

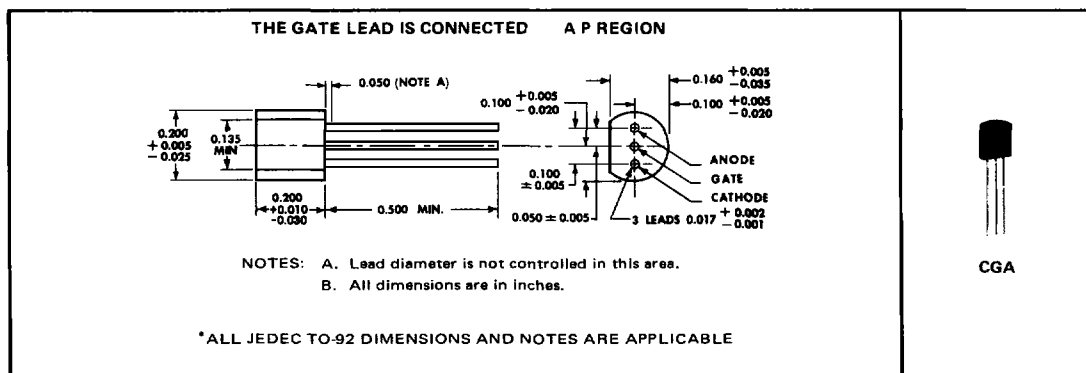
TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64 P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

SILECT[†] THYRISTORS[‡]
800 mA DC • 30 thru 200 VOLTS

mechanical data

These thyristors are encapsulated in a plastic compound specifically designed for this purpose, using a highly mechanized process developed by Texas Instruments. The case will withstand soldering temperatures without deformation. These devices exhibit stable characteristics under high-humidity conditions and are capable of meeting MIL-STD-202C method 106B. The thyristors are insensitive to light.

TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64
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absolute maximum ratings at specified case temperature

		2N5060	2N5061	2N5062	2N5063	2N5064	UNIT
		TIC60	TIC61	TIC62	TIC63	TIC64	
* Repetitive Peak Off-State Voltage, V_{DRM} (See Note 1)	-65°C to 125°C	30	60	100	150	200	V
* Repetitive Peak Reverse Voltage, V_{RRM}	-65°C to 125°C	30	60	100	150	200	V
* Nonrepetitive Peak Reverse Voltage, V_{RSM} (Pulse Width ≤ 5 ms)	-65°C to 125°C	45	80	125	180	230	V
Continuous On-State Current (See Note 2)	-65°C to 50°C	800					mA
* Average On-State Current (180° Conduction Angle, See Note 3)	-65°C to 67°C	510					mA
* Surge On-State Current (See Note 4)	25°C	6					A
* Peak Positive Gate Current (Pulse Width ≤ 300 μ s, $f \leq 120$ pps)	25°C	1					A
* Peak Gate Reverse Voltage	-65°C to 125°C	5					V
* Average Gate Power Dissipation (See Note 5)	25°C	10					mW
* Peak Gate Power Dissipation (Pulse Width ≤ 300 μ s)	25°C	100					mW
* Operating Case Temperature Range		-65 to 125					°C
* Storage Temperature Range		-65 to 150					°C
* Lead Temperature 1/16 Inch from Case for 10 Seconds		230					°C

- NOTES: 1. These values apply when the gate-cathode resistance $R_{GK} = 1$ k Ω .
2. These values apply for continuous d-c operation with resistive load. Above 50°C derate according to Figure 1.
3. This value may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 67°C derate according to Figure 1.
4. This value applies for one 60-Hz half sine wave when the device is operating at (or below) rated values of peak reverse voltage and on-state current. Surge may be repeated after the device has returned to original thermal equilibrium.
5. This value applies for a maximum averaging time of 16.6 ms.

*JEDEC registered data. The asterisk identifies JEDEC registered data for the 2N5060 through 2N5064 only. This data sheet contains all applicable registered data in effect at the time of publication.

[†] Trademark of Texas Instruments

[‡] U.S. Patent No. 3,439,238

TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64

P-N-P-N SILICON REVERSE-BLOCKING TRIODE THYRISTORS

electrical characteristics at specified case temperature

PARAMETER	TEST CONDITIONS	2N5060 THRU 2N5064		TIC60 THRU TIC64		UNIT
		MIN	MAX	MIN	MAX	
I_{ORM} Repetitive Peak Off-State Current	$V_D = \text{Rated } V_{ORM}, R_{GK} = 1 \text{ k}\Omega, 125^\circ\text{C}$		50*		50	μA
I_{RRM} Repetitive Peak Reverse Current	$V_R = \text{Rated } V_{RRM}, R_{GK} = 1 \text{ k}\Omega, 125^\circ\text{C}$		50*		50	μA
I_{GT} Gate Trigger Current	$V_{AA} = 7 \text{ V}, R_L = 100 \Omega, -65^\circ\text{C}$ $R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 1 \text{ ms}, 25^\circ\text{C}$		350*		200	μA
V_{GT} Gate Trigger Voltage	$V_{AA} = 7 \text{ V}, R_L = 100 \Omega, -65^\circ\text{C}$ $R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 1 \text{ ms}, 25^\circ\text{C}$		1.2*		0.8	V
	$V_D = \text{Rated } V_{DRM}, R_L = 100 \Omega, 125^\circ\text{C}$ $R_{GK} = 1 \text{ k}\Omega, t_{p(g)} \geq 1 \text{ ms}$	0.1*		0.1		
I_H Holding Current	$V_{AA} = 7 \text{ V}, R_{GK} = 1 \text{ k}\Omega, -65^\circ\text{C}$ Initiating $I_T = 20 \text{ mA}, 25^\circ\text{C}$		10*		5	mA
V_{TM} Peak On-State Voltage	$I_{TM} = 1.2 \text{ A}, \text{ See Note 6}, 25^\circ\text{C}$		1.7*		1.7	V

*thermal characteristics

PARAMETER	MAX	UNIT
$R_{\theta JC}$ Junction-to-Case Thermal Resistance	75	$^\circ\text{C/W}$

NOTE 6: This parameter must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 1\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

*JEDEC registered data

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THERMAL INFORMATION

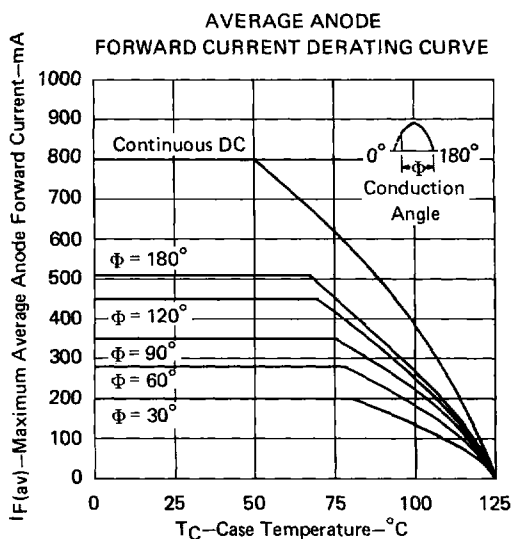


FIGURE 1

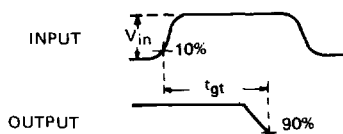
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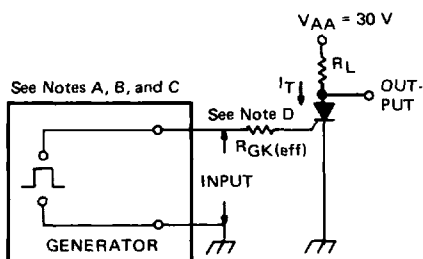
switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	TYP	UNIT
t_{gt} Gate-Controlled Turn-On-Time	$V_{AA} = 30\text{ V}$, $R_L = 39\ \Omega$, $R_{GK}(\text{eff}) = 20\text{ k}\Omega$, $V_{in} = 20\text{ V}$, See Figure 2	3	μs
t_q Circuit-Commutated Turn-Off Time	$V_{AA} = 30\text{ V}$, $R_L = 30\ \Omega$, $I_{RM} \approx 7\text{ A}$, See Figure 3	7	μs

PARAMETER MEASUREMENT INFORMATION

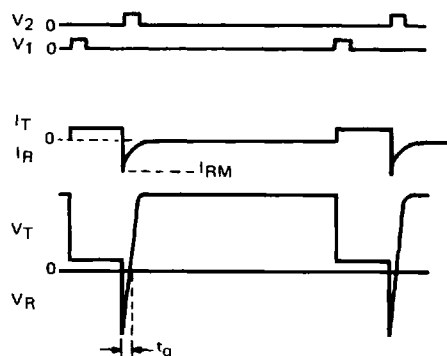


VOLTAGE WAVEFORMS

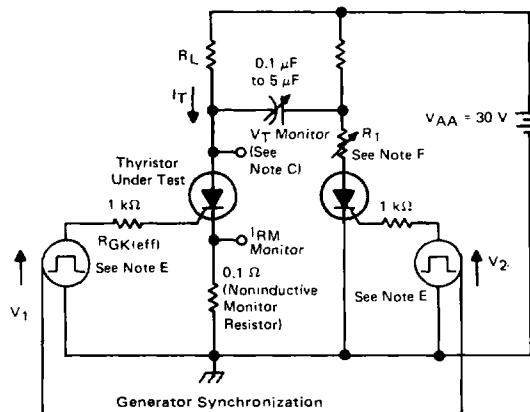


TEST CIRCUIT

FIGURE 2—GATE-CONTROLLED TURN-ON TIME



WAVEFORMS



TEST CIRCUIT

FIGURE 3—CIRCUIT-COMMUTATED TURN-OFF TIME

- NOTES:
- V_{in} is measured with gate and cathode terminals open.
 - The input waveform of Figure 2 has the following characteristics: $t_r \leq 40\text{ ns}$, $t_w \geq 20\ \mu\text{s}$.
 - Waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 14\text{ ns}$, $R_{in} \geq 10\text{ M}\Omega$, $C_{in} \leq 12\text{ pF}$.
 - $R_{GK}(\text{eff})$ includes the total resistance of the generator and the external resistor.
 - Pulse generators for V_1 and V_2 are synchronized to provide an anode current waveform with the following characteristics: $t_w = 50$ to $300\ \mu\text{s}$, duty cycle = 1%. The pulse widths of V_1 and V_2 are $\geq 10\ \mu\text{s}$.
 - Resistor R_1 is adjusted for $I_{RM} \approx 7\text{ A}$.

TYPES 2N5060 THRU 2N5064, TIC60 THRU TIC64

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TYPICAL CHARACTERISTICS

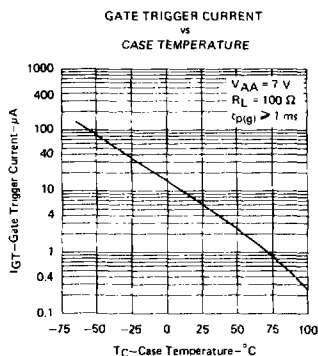


FIGURE 4

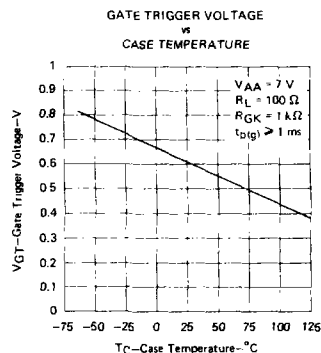


FIGURE 5

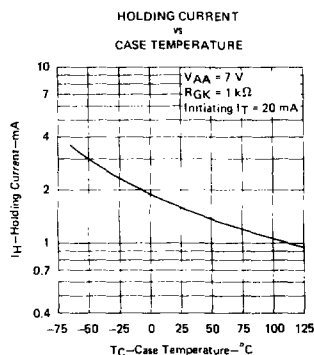


FIGURE 6

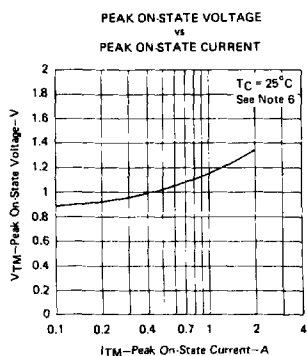


FIGURE 7

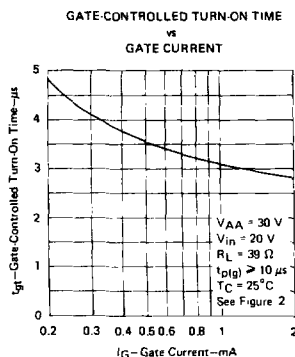


FIGURE 8

NOTE 6: This parameter must be measured using pulse techniques. $t_W = 300 \mu\text{s}$, duty cycle $\leq 2\%$. Voltage-sensing contacts, separate from the current-carrying contacts, are located within 0.125 inch from the device body.

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