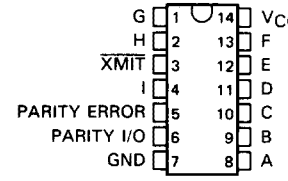
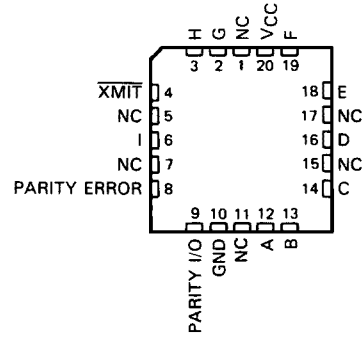
- **Generates Either Odd or Even Parity for Nine Data Lines**
- **Cascadable for n-Bits Parity**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54F286 . . . J PACKAGE
SN74F286 . . . D OR N PACKAGE
(TOP VIEW)



SN54F286 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

The SN54F286 and SN74F286 universal nine-bit parity generators/checkers feature a local output for parity checking and a bus-driving parity I/O port for parity generation/checking. The word-length capability is easily expanded by cascading.

The $\overline{\text{XMIT}}$ control input is implemented specifically to accommodate cascading. When $\overline{\text{XMIT}}$ is low, the parity tree is disabled and the Parity Error output will remain at a high logic level regardless of the input levels. When $\overline{\text{XMIT}}$ is high, the parity tree is enabled. The Parity Error output will indicate a parity error when either an even number of inputs (A through I) are high and Parity I/O is forced to a low logic level, or when an odd number of inputs are high and Parity I/O is forced to a high logic level.

The I/O control circuitry was designed so that the I/O port will remain in the high-impedance state during power-up or power-down to prevent bus glitches.

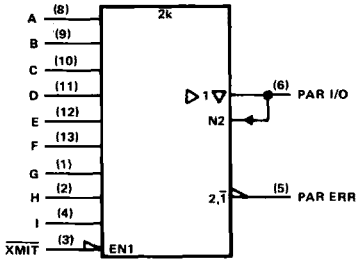
The SN54F286 is characterized for operation over the full military range of −55°C to 125°C. The SN74F286 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

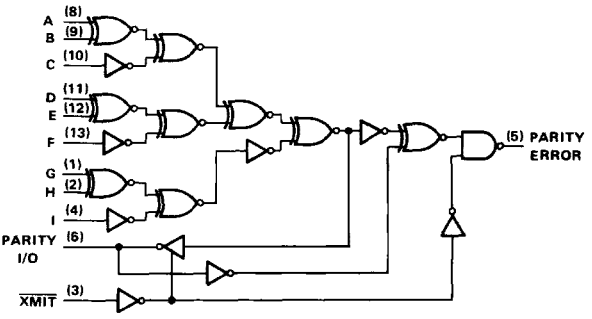
NUMBER OF INPUTS (A THRU I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h = high input level l = low input level
H = high output level L = low output level

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage‡ . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to Parity I/O in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to either output in the high state . . . . . −0.5 V to V_{CC}
Current into either output in the low state: SN54F286 (Parity Error) . . . . . 40 mA
SN54F286 (Parity I/O) . . . . . 96 mA
SN74F286 (Parity Error) . . . . . 40 mA
SN74F286 (Parity I/O) . . . . . 128 mA
Operating free-air temperature range: SN54F286 . . . . . −55°C to 125°C
SN74F286 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

‡ The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

			SN54F286			SN74F286			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	High-level output current	Parity Error			−1			−1	mA
		Parity I/O			−12			−15	
I_{OL}	Low-level output current	Parity Error			20			20	mA
		Parity I/O			48			64	
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F286			SN74F286			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	Parity Error	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
	Parity I/O		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
	Any output	V_{CC} = 4.75 V	I_{OH} = −1 mA to −3 mA				2.7			
V_{OL}	Parity Error	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
	Parity I/O		I_{OL} = 48 mA		0.38	0.55				
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}‡	Parity I/O	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	μA
	Any other input					20			20	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	Parity I/O	V_{CC} = 5.5 V,	V_I = 0.5 V	−100		−225	−100		−225	mA
	Parity Error			−60		−150	−60		−150	
I_{CCH}		V_{CC} = 5.5 V,			27			27	44	mA
I_{CCL}		V_{CC} = 5.5 V			28			28	45	mA
I_{CCZ}		V_{CC} = 5.5 V			27			27	44	mA

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX¶				UNIT
			'F286			SN54F286		SN74F286		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Any A thru I	Parity I/O		8.3						ns
t_{PHL}				8.6						
t_{PLH}	Any A thru I	Parity Error		10.8						ns
t_{PHL}				10						
t_{PLH}	Parity I/O	Parity Error		4.9						ns
t_{PHL}				5						
t_{PZH}	$\overline{XMIT}$	Parity I/O		3.8						ns
t_{PZL}				5.8						
t_{PHZ}	$\overline{XMIT}$	Parity I/O		3.8						ns
t_{PLZ}				3.3						

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, parameters I_{IH} and I_{IL} include the off-state output current.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
¶For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 1: Load circuits and waveforms are shown in Section 1.