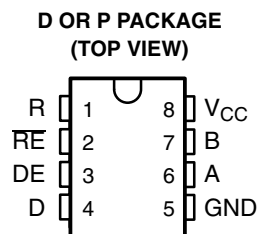


- **Bidirectional Transceiver**
- **Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Skew . . . 6 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply-Current Requirements . . . 30 mA Max**
- **Wide Positive and Negative Input/Output Bus-Voltage Ranges**
- **Driver Output Capacity . . .  $\pm 60$  mA**
- **Thermal-Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 k $\Omega$  Min**
- **Receiver Input Sensitivity . . .  $\pm 200$  mV Max**
- **Receiver Input Hysteresis . . . 120 mV Typ**
- **Fail Safe . . . High Receiver Output With Inputs Open**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Interchangeable With National DS3695 and DS3695A**



## description

The TL3695 differential bus transceiver is designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

The TL3695 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a directional control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or  $V_{CC} = 0$ . This port features wide positive and negative common-mode voltage ranges, making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# TL3695 DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TL3695D	TL3695P

The D package is available taped and reeled. Add the suffix R to device type (e.g., TL3695DR).

### Function Tables

#### DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

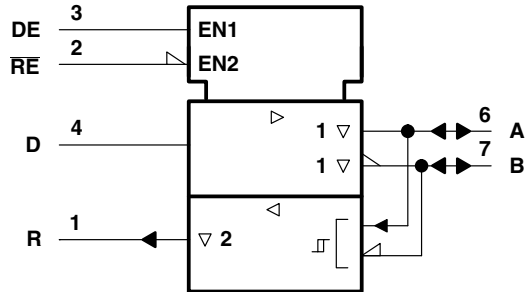
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

#### RECEIVER

DIFFERENTIAL INPUTS A – B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Inputs open	L	H

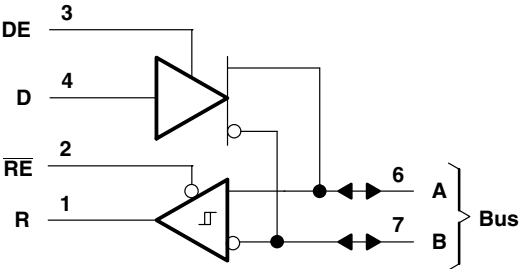
H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

### logic symbol†

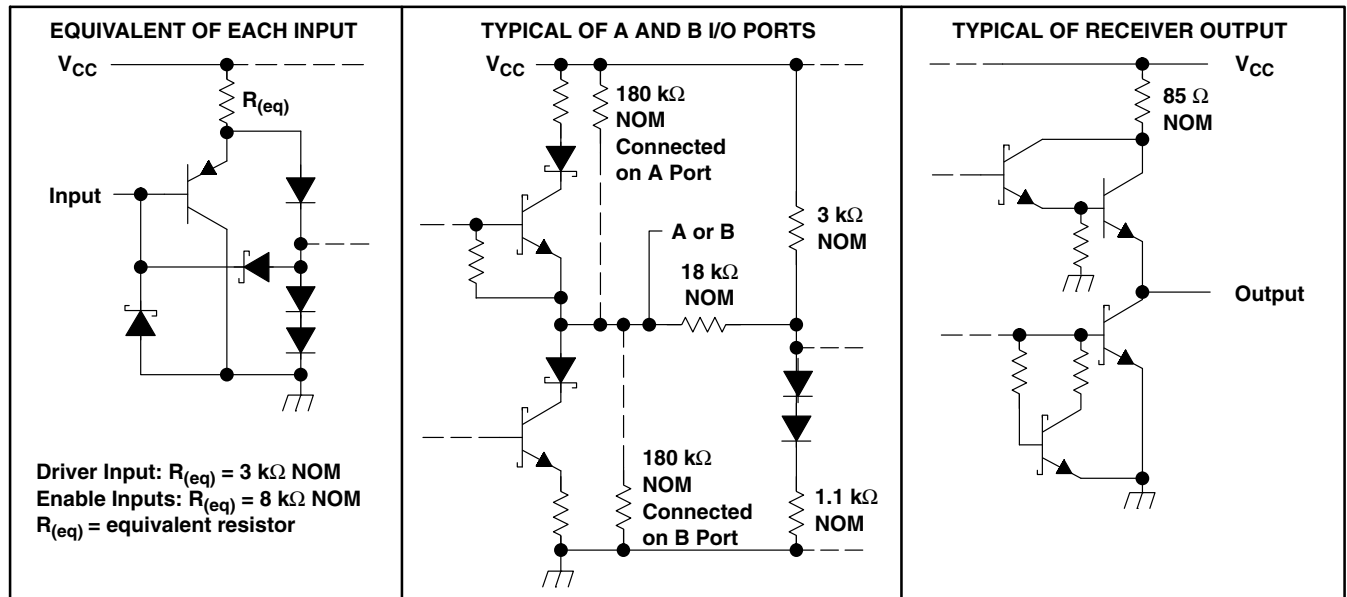


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### logic diagram (positive logic)



## schematic of inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	–10 V to 15 V
Enable input voltage, $V_I$	5.5 V
Operating free-air temperature range, $T_A$	0°C to 70°C
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	97°C/W
PW package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.  
 2. The package thermal impedance is calculated in accordance with JESD 51.

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

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### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V <sub>I</sub> or V <sub>IC</sub>		12			V
		−7			
High-level Input voltage, V <sub>IH</sub>	D, DE, and RE	2			V
Low-level Input voltage, V <sub>IL</sub>	D, DE, and RE	0.8			V
Differential input voltage, V <sub>ID</sub> (see Note 3)		±12			V
High-level output current, I <sub>OH</sub>	Driver	− 60			mA
	Receiver	− 400			μA
Low-level output current, I <sub>OL</sub>	Driver	60			mA
	Receiver	8			
Operating free-air temperature, T <sub>A</sub>		0		70	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

## DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{IK}$ Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$V_O$ Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		5	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$ , See Figure 1	$1/2 V_{OD1}$ or 2§			V
	$R_L = 54 \Omega$ , See Figure 1	1.5	2.5	5	V
$V_{OD3}$ Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$ , See Figure 2	1.5		5	V
$\Delta  V_{OD} $ Change in magnitude of differential output voltage¶	$R_L = 54 \Omega$ , See Figure 1			$\pm 0.2$	V
$V_{OC}$ Common-mode output voltage				3	V
$\Delta  V_{OC} $ Change in magnitude of common-mode output voltage¶				$\pm 0.2$	V
$I_O$ Output current	Output disabled, See Note 4	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
$I_{IH}$ High-level input current	$V_I = 2.4 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$ Low-level input current	$V_I = 0.4 \text{ V}$			-200	$\mu\text{A}$
$I_{OS}$ Short-circuit output current#	$V_O = -6 \text{ V}$			-250	mA
	$V_O = 0$			-150	
	$V_O = V_{CC}$			250	
	$V_O = 8 \text{ V}$			250	
$I_{CC}$ Supply current	No load	Outputs enabled	23	50	mA
		Outputs disabled	19	35	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

§ The minimum  $V_{OD2}$  with a 100- $\Omega$  load is either  $1/2 V_{OD1}$  or 2 V, whichever is greater.

¶  $\Delta |V_{OD}|$  and  $\Delta |V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

# Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature**

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{d(OD)}$ Differential-output delay time	$C_{L1} = C_{L2} = 100 \text{ pF}$ , $R_L = 60 \Omega$ , See Figure 3		8	22	ns
Skew ( $ t_{d(ODH)} - t_{d(ODL)} $ )			1	8	ns
$t_{f(OD)}$ Differential output transition time			8	18	ns
$t_{PZH}$ Output enable time to high level	$C_L = 100 \text{ pF}$ , $R_L = 500 \Omega$ , See Figure 4			50	ns
$t_{PZL}$ Output enable time to low level	$C_L = 100 \text{ pF}$ , $R_L = 500 \Omega$ , See Figure 5			50	ns
$t_{PHZ}$ Output disable time from high level	$C_L = 15 \text{ pF}$ , $R_L = 500 \Omega$ , See Figure 4		8	30	ns
$t_{PLZ}$ Output disable time from low level	$C_L = 15 \text{ pF}$ , $R_L = 500 \Omega$ , See Figure 5		8	30	ns

‡ All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

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### SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
$V_O$	$V_{oa}, V_{ob}$	$V_{oa}, V_{ob}$
$ V_{OD1} $	$V_o$	$V_o$
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $		$V_t$ (test termination measurement 2)
$V_{test}$		$V_{tst}$
$\Delta  V_{OD} $	$   V_t  -  \bar{V}_t   $	$   V_t  -  \bar{V}_t   $
$V_{OC}$	$ V_{os} $	$ V_{os} $
$\Delta  V_{OC} $	$  V_{os} - \bar{V}_{os}  $	$  V_{os} - \bar{V}_{os}  $
$I_{OS}$	$  I_{sa}  ,   I_{sb}  $	
$I_O$	$  I_{xa}  ,   I_{xb}  $	$I_{ia}, I_{ib}$

### RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT+}$ Positive-going input threshold voltage	$V_O = 2.7 \text{ V}$ , $I_O = -0.4 \text{ mA}$			0.2	V
$V_{IT-}$ Negative-going input threshold voltage	$V_O = 0.5 \text{ V}$ , $I_O = 8 \text{ mA}$	$-0.2^\ddagger$			V
$V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )	$V_{OC} = 0$		70		mV
$V_{IK}$ Enable-input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
$V_{OH}$ High-level output voltage	$V_{ID} = 200 \text{ mV}$ or inputs open, $I_{OH} = -400 \mu\text{A}$ , See Figure 6	2.4			V
$V_{OL}$ Low-level output voltage	$V_{ID} = -200 \text{ mV}$ , See Figure 6	$I_{OL} = 16 \text{ mA}$		0.5	V
		$I_{OL} = 8 \text{ mA}$		0.45	
$I_{OZ}$ High-impedance-state output current	$V_O = 0.4 \text{ V}$ to $2.4 \text{ V}$			$\pm 20$	$\mu\text{A}$
$I_I$ Line input current	Other input = 0, See Note 5	$V_I = 12 \text{ V}$		1	mA
		$V_I = -7 \text{ V}$		-0.8	
$I_{IH}$ High-level enable-input current	$V_{IH} = 2.7 \text{ V}$			20	$\mu\text{A}$
$I_{IL}$ Low-level enable-input current	$V_{IL} = 0.4 \text{ V}$			-100	$\mu\text{A}$
$r_I$ Input resistance		12			k $\Omega$
$I_{OS}$ Short-circuit output current§	$V_O = 0$	-15		-85	mA
$I_{CC}$ Supply current	No load	Outputs enabled	23	50	mA
		Outputs disabled	19	35	

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§ Duration of the short circuit should not exceed one second for this test.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.



switching characteristics over recommended ranges of supply voltage and operating free-air temperature range,  $C_L = 15 \text{ pF}$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH}$ Propagation delay time, low- to high-level output	$V_{ID} = -1.5 \text{ V to } 1.5 \text{ V}$ , See Figure 7		14	37	ns
$t_{PHL}$ Propagation delay time, high- to low-level output			14	37	ns
$t_{PZH}$ Output enable time to high level	See Figure 8		7	20	ns
$t_{PZL}$ Output enable time to low level			7	20	ns
$t_{PHZ}$ Output disable time from high level	See Figure 8		7	16	ns
$t_{PLZ}$ Output disable time from low level			8	16	ns

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

### PARAMETER MEASUREMENT INFORMATION

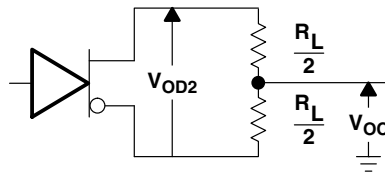


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

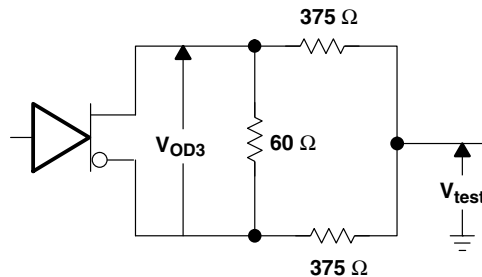
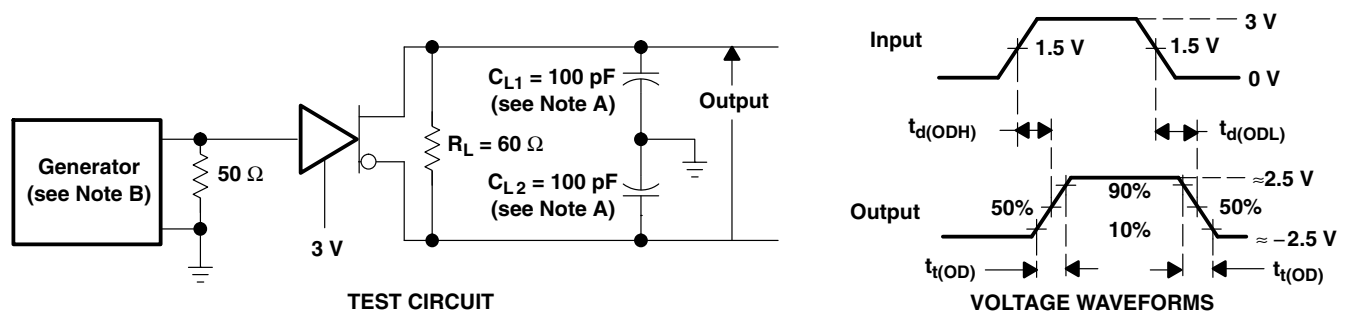


Figure 2. Driver  $V_{OD3}$



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , 50% duty cycle,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$ ,  $Z_O = 50 \Omega$ .

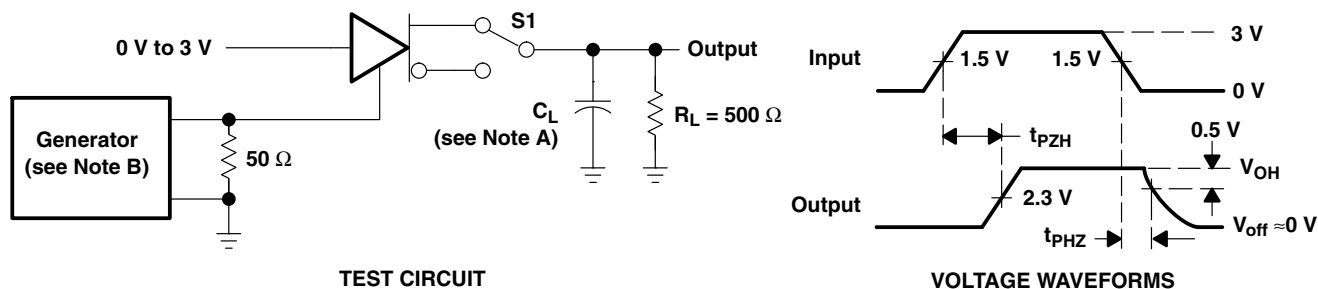
Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

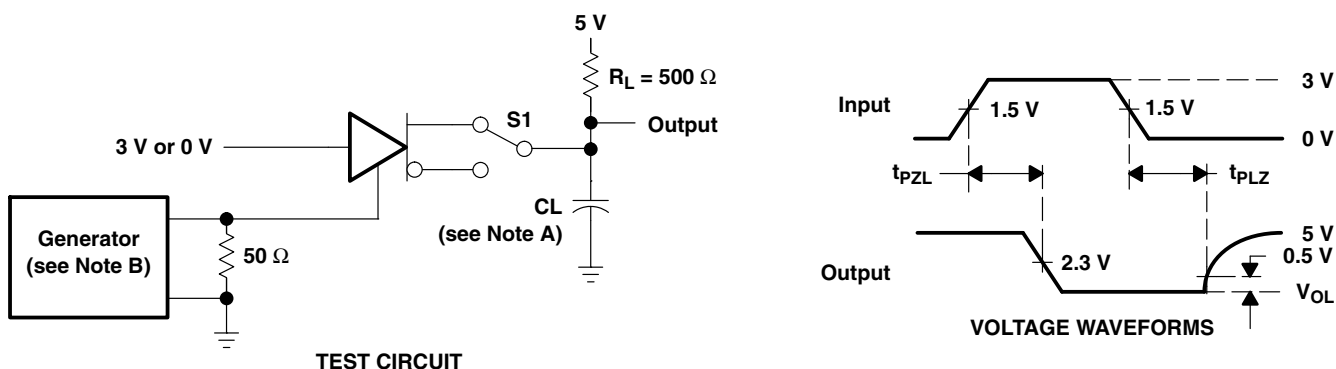
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### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

Figure 4. Driver Test Circuit and Voltage Waveforms



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

Figure 5. Driver Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION

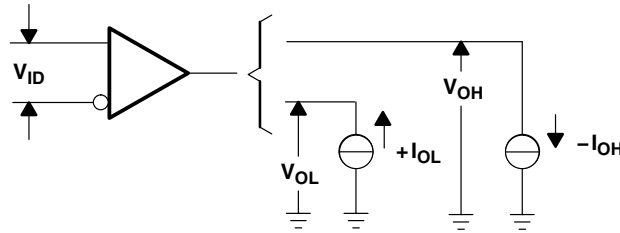
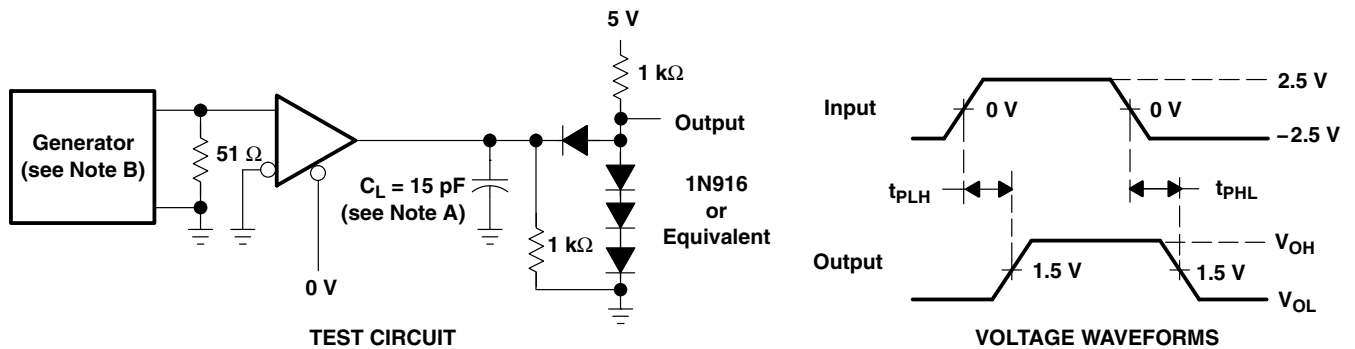


Figure 6. Receiver  $V_{OH}$  and  $V_{OL}$



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

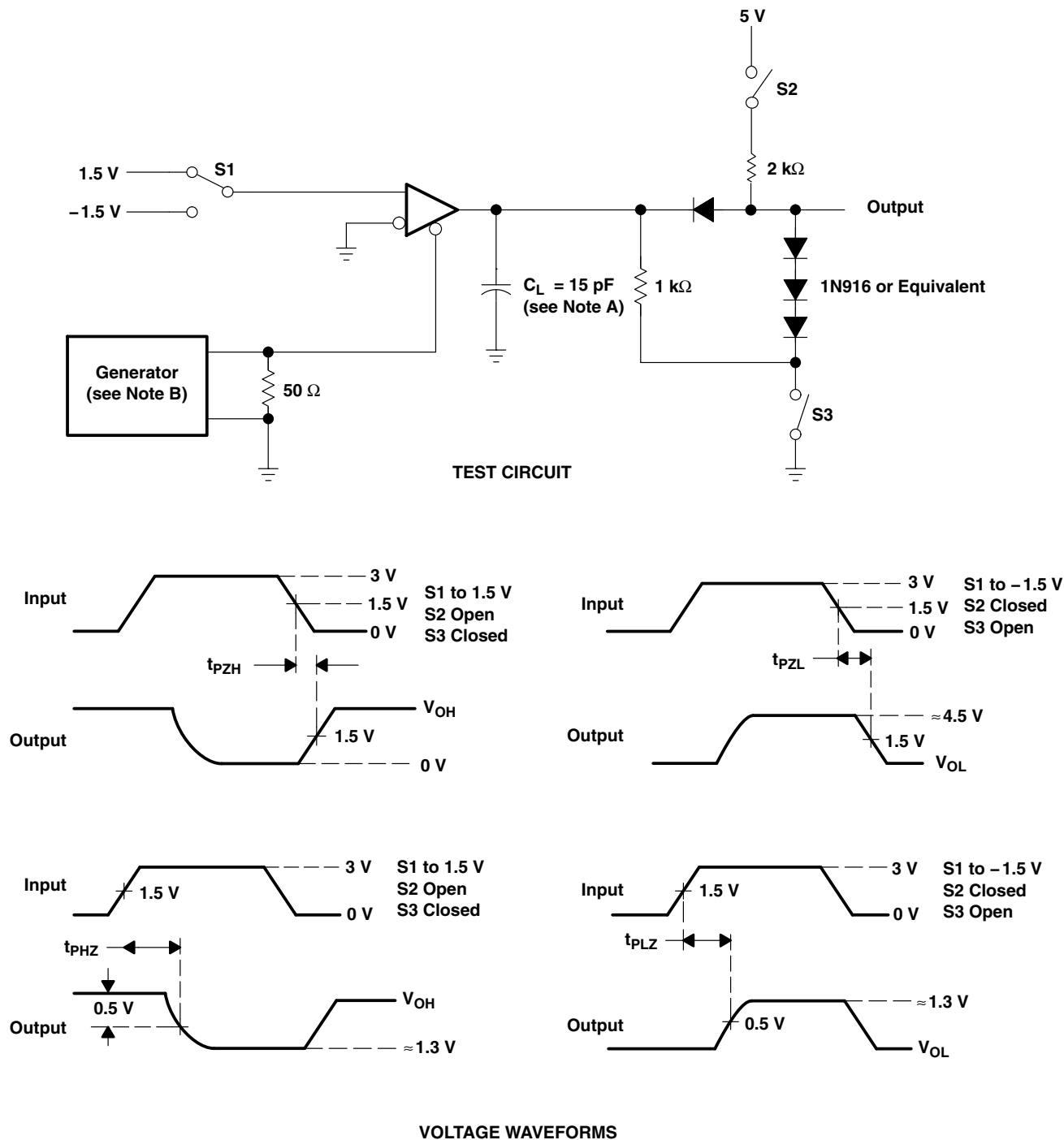
Figure 7. Receiver Test Circuit and Voltage Waveforms

# TL3695

## DIFFERENTIAL BUS TRANSCEIVER

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### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 1$  MHz, 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns,  $Z_O = 50 \Omega$ .

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

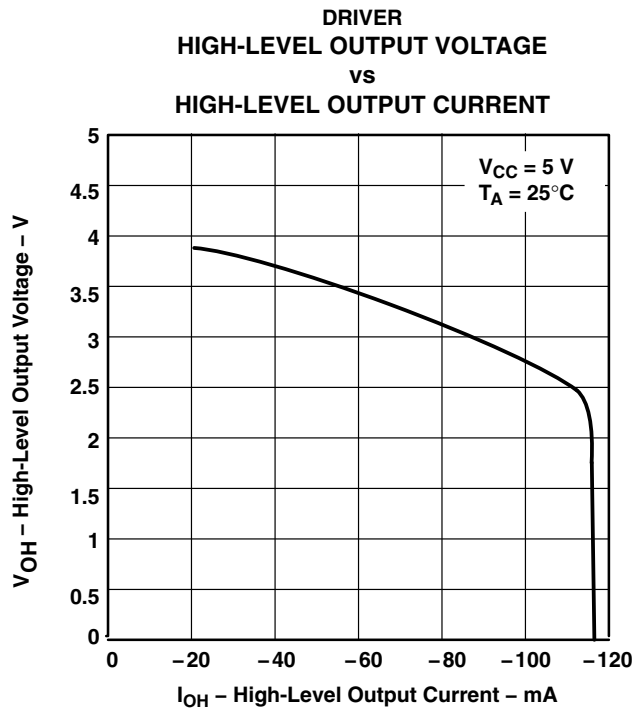


Figure 9

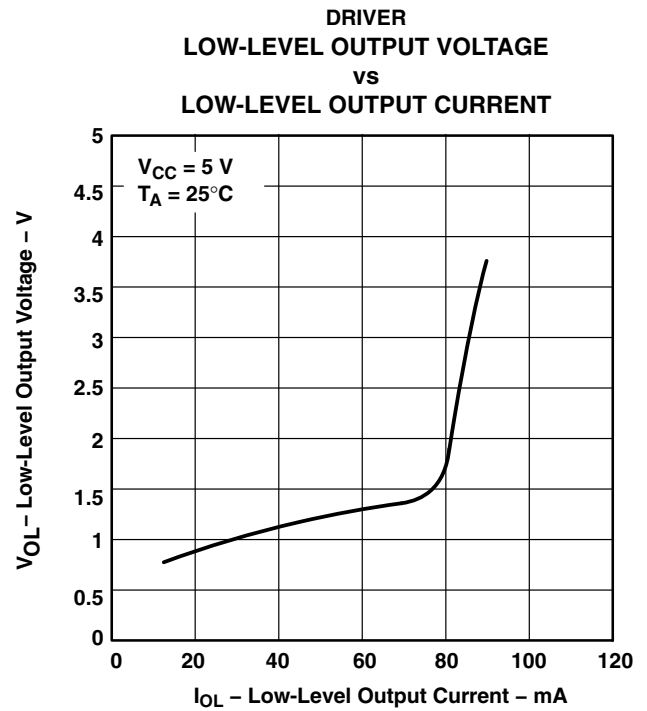


Figure 10

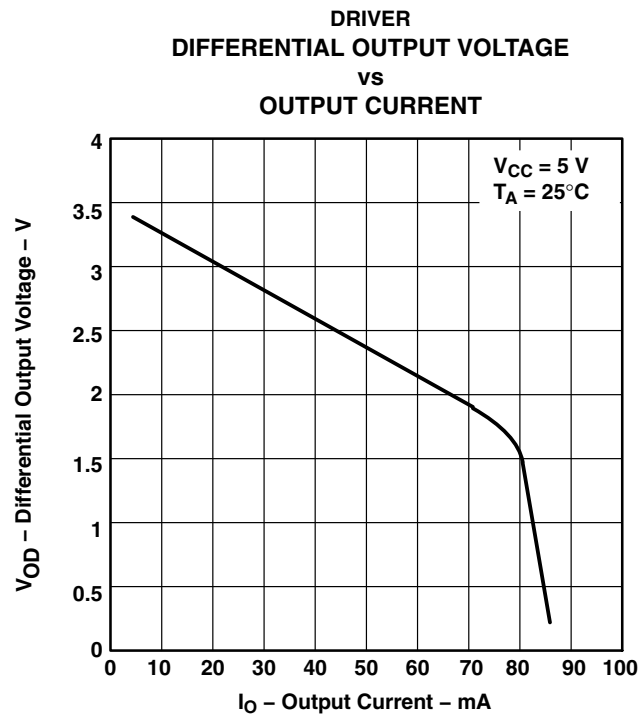


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

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TYPICAL CHARACTERISTICS†

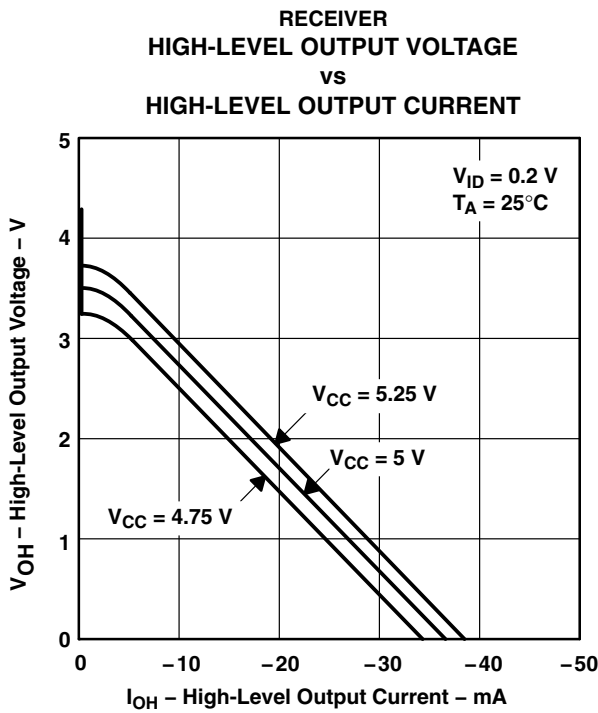


Figure 12

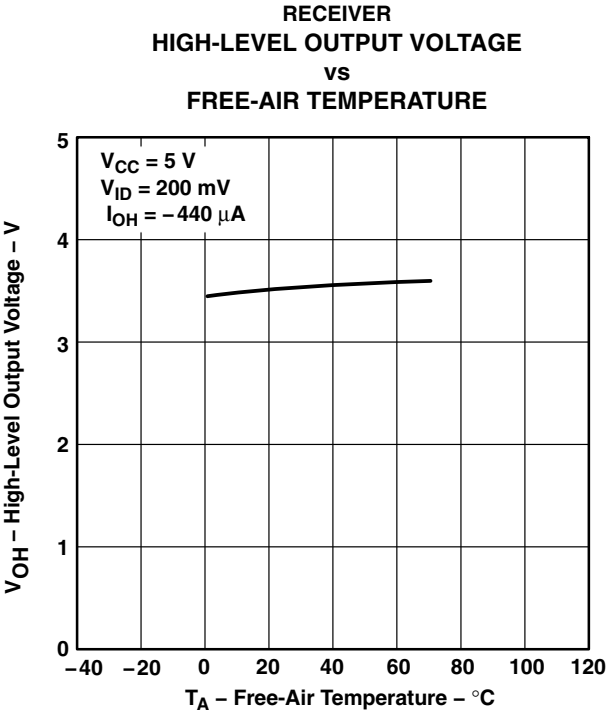


Figure 13

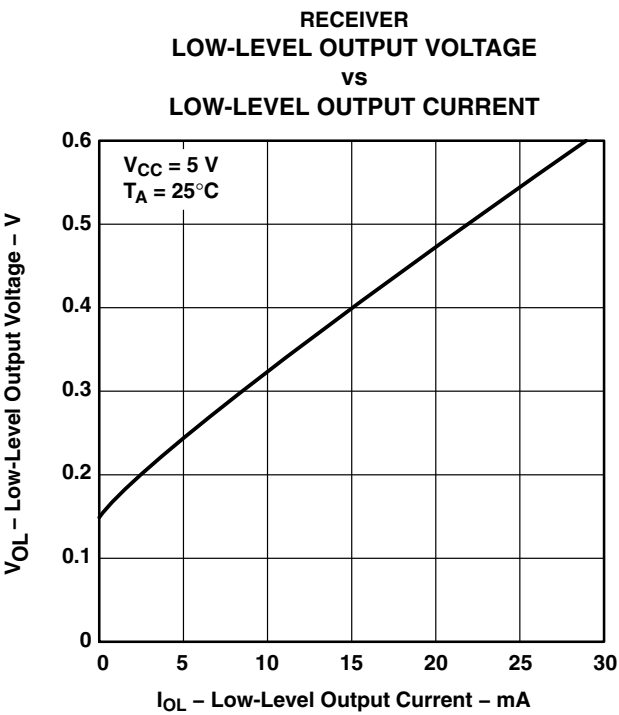


Figure 14

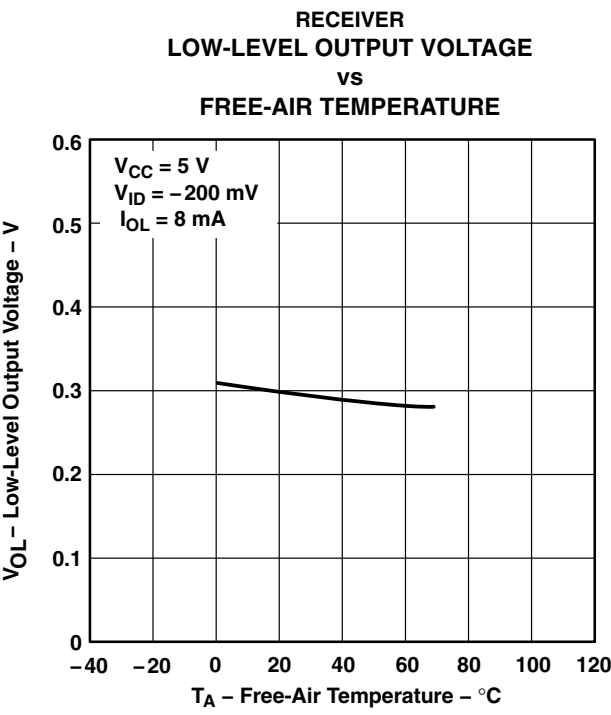
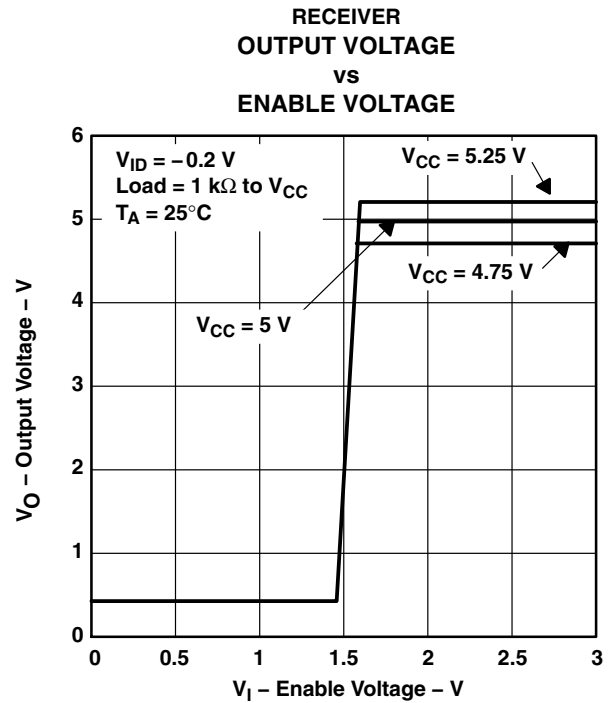
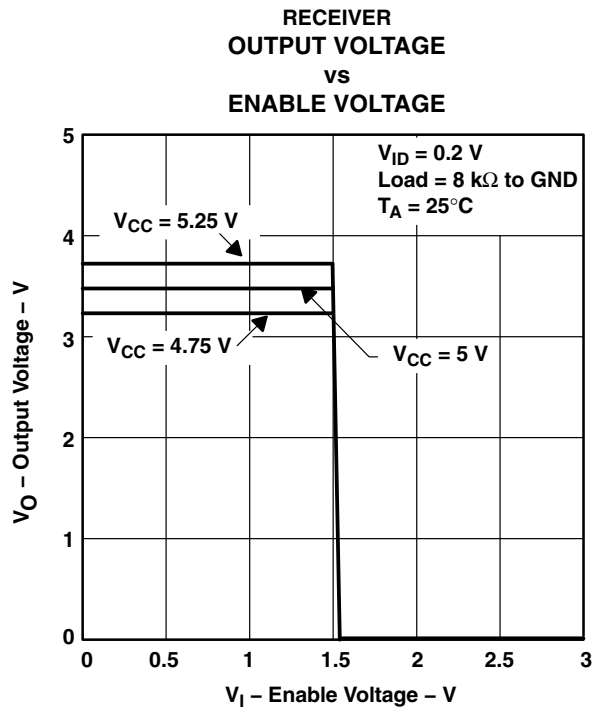


Figure 15

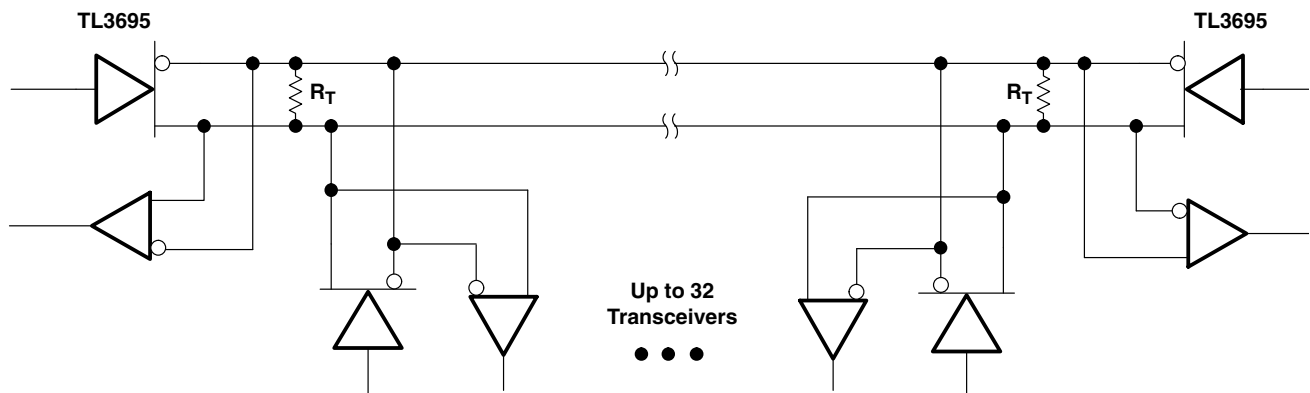
† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

### TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

### APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

**Figure 18. Typical Application Circuit**

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL3695D	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695
TL3695D.A	Active	Production	SOIC (D)   8	75   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695
<a href="#">TL3695DR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695
TL3695DR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695
TL3695DRG4	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695
TL3695P	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3695P
TL3695P.A	Active	Production	PDIP (P)   8	50   TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL3695P

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

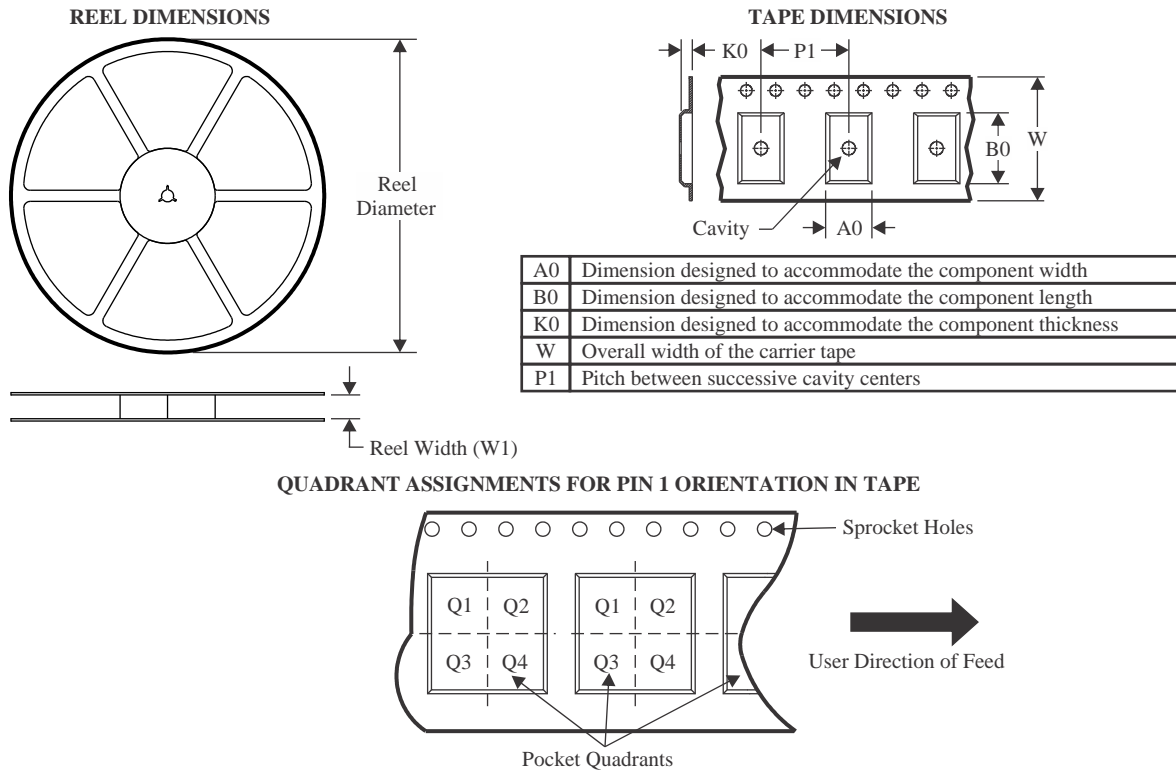
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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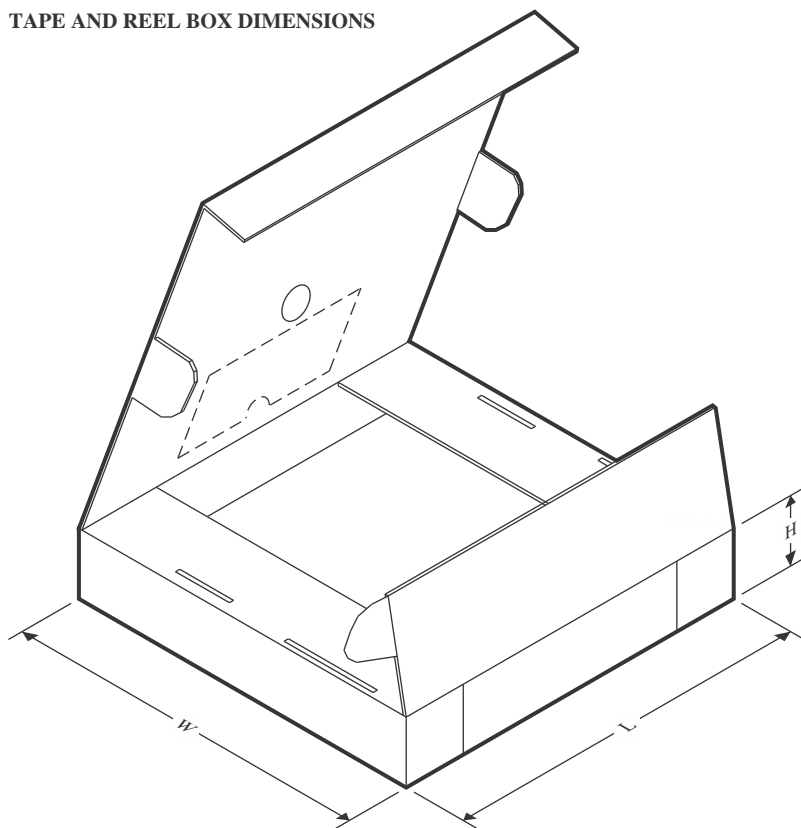
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3695DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

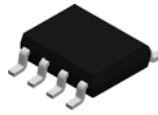
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3695DR	SOIC	D	8	2500	353.0	353.0	32.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TL3695D	D	SOIC	8	75	507	8	3940	4.32
TL3695D.A	D	SOIC	8	75	507	8	3940	4.32
TL3695P	P	PDIP	8	50	506	13.97	11230	4.32
TL3695P.A	P	PDIP	8	50	506	13.97	11230	4.32

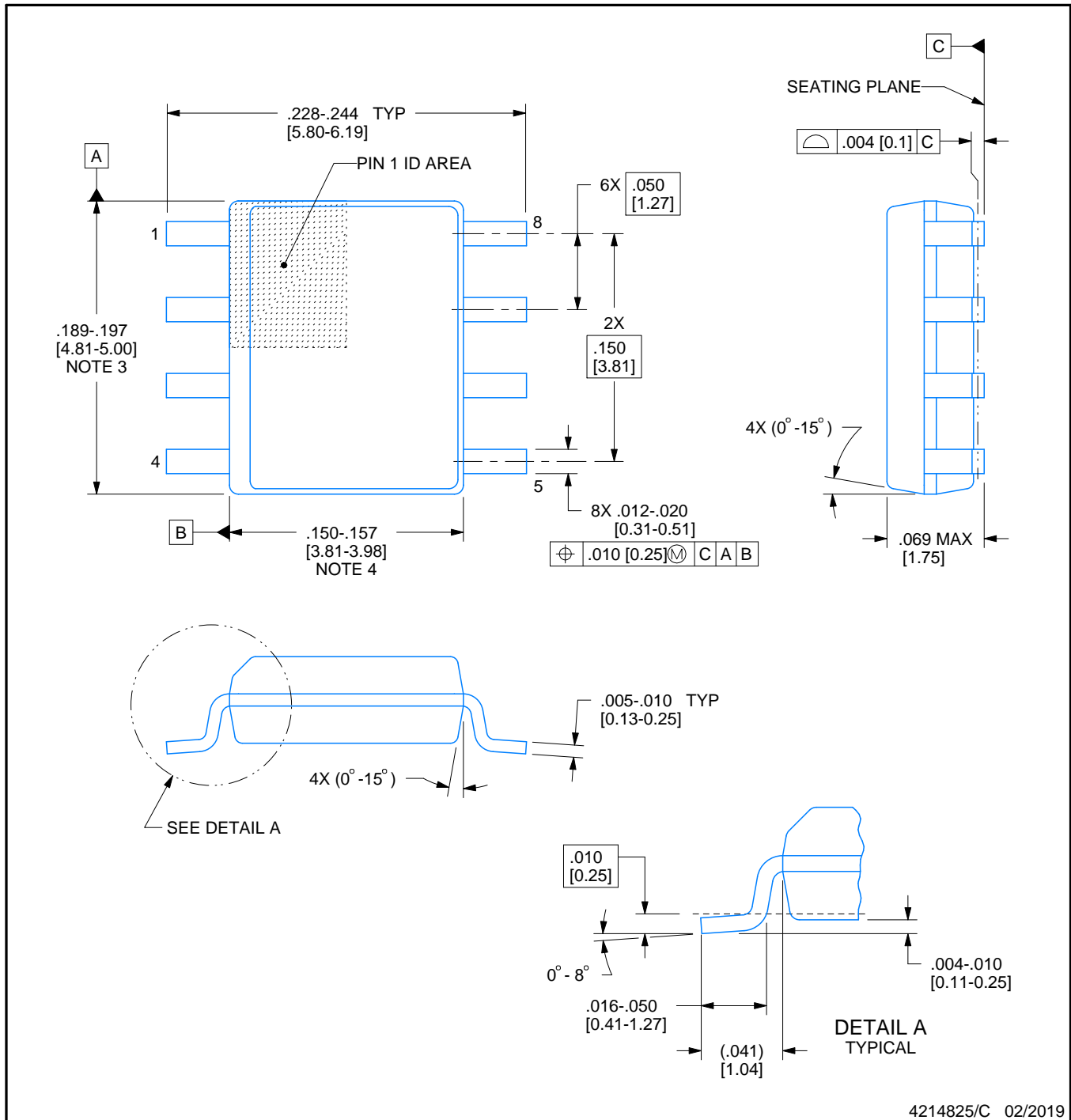


**D0008A**

# PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

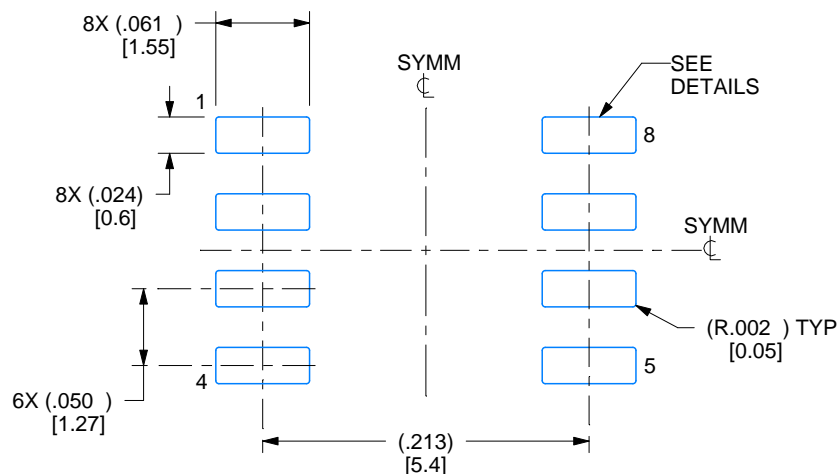
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

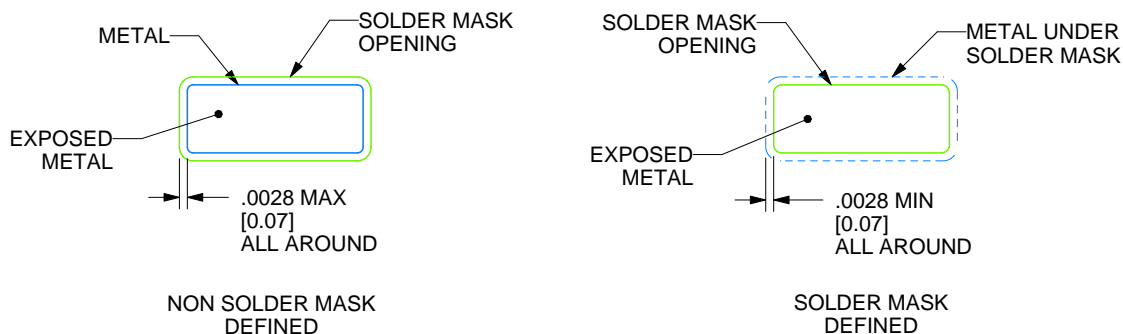
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

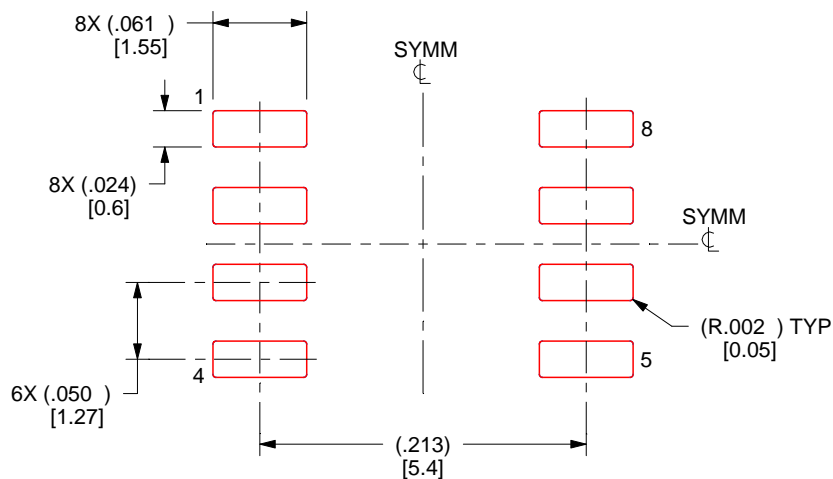
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

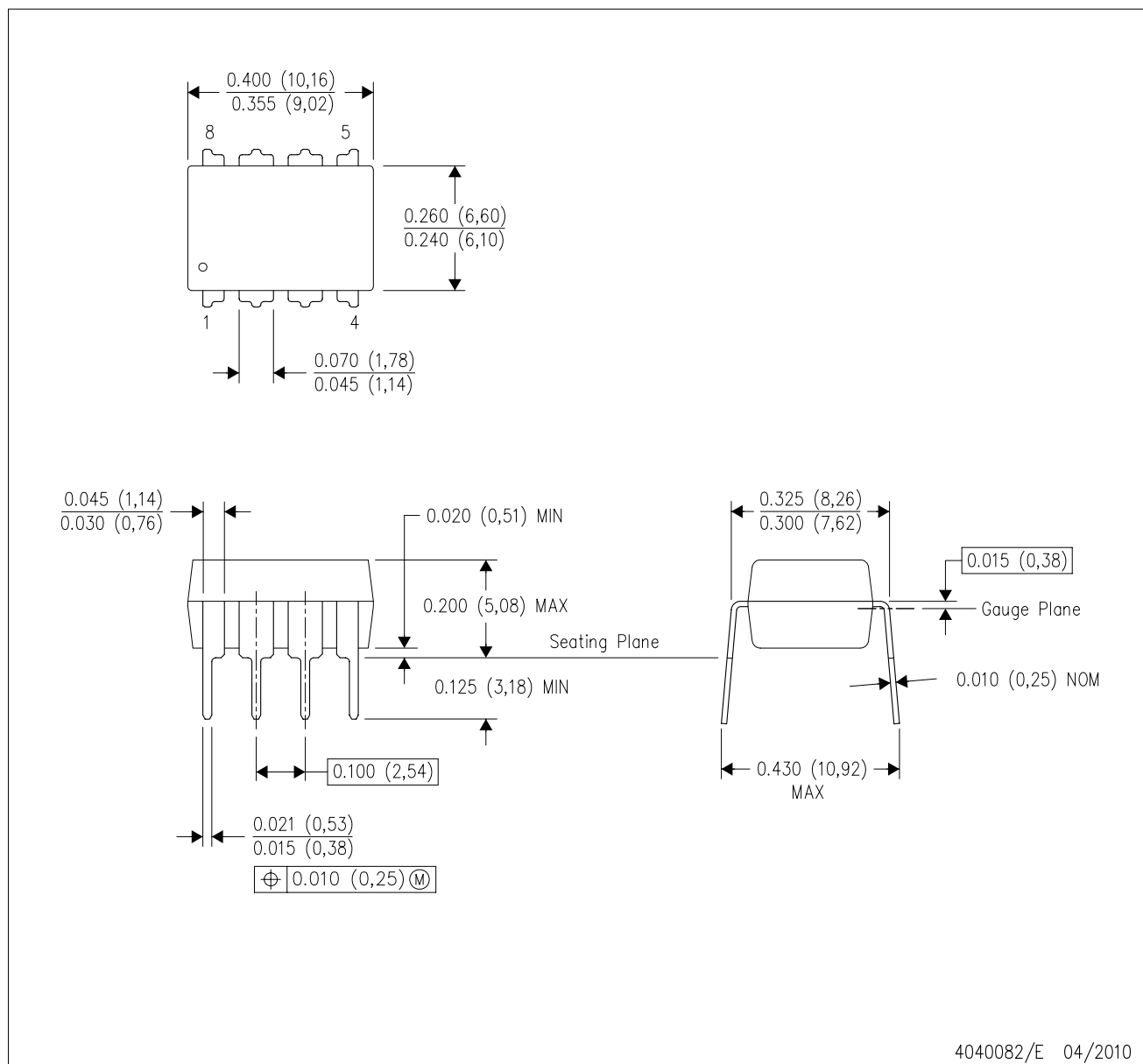
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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