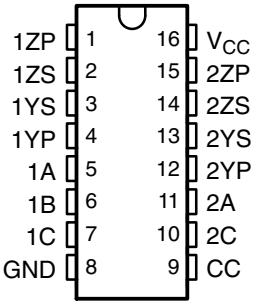
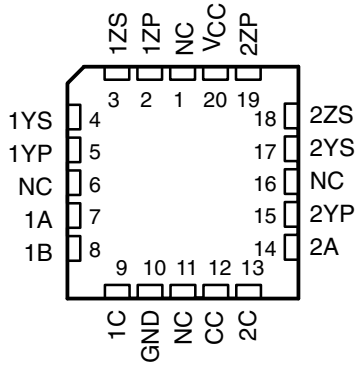
SLLS070C – SEPTEMBER 1973 – REVISED MARCH 1997

- **Choice of Open-Collector, Open-Emitter, or 3-State Outputs**
- **High-Impedance Output State for Party-Line Applications**
- **Single-Ended or Differential AND/NAND Outputs**
- **Single 5-V Supply**
- **Dual Channel Operation**
- **Compatible With TTL**
- **Short-Circuit Protection**
- **High-Current Outputs**
- **Common and Individual Output Controls**
- **Clamp Diodes at Inputs and Outputs**
- **Easily Adaptable to SN55114 and SN75114 Applications**
- **Designed for Use With SN55115 and SN75115**

**SN55113 . . . J OR W PACKAGE**
**SN75113 . . . N PACKAGE**
**(TOP VIEW)**




**SN55113 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The SN55113 and SN75113 dual differential line drivers with 3-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. Individual controls are provided for each output pair, as well as a common control for both output pairs. If any output is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pullup terminals, YP and ZP, available on adjacent package pins.

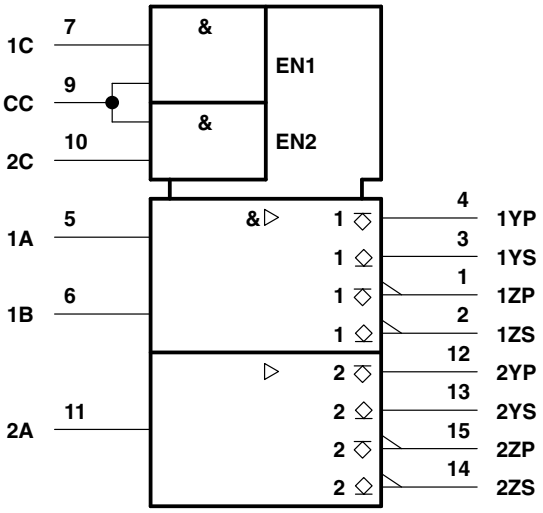
The SN55113 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN75113 is characterized for operation over the temperature range of 0°C to 70°C.

**FUNCTION TABLE**

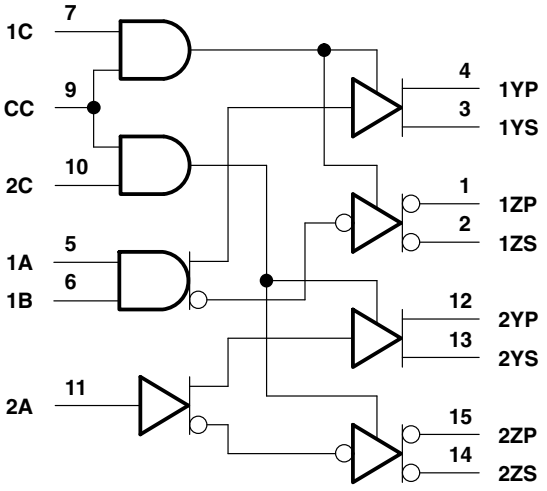
| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| OUTPUT C | CONTROL CC | DATA A | DATA B† | AND Y | NAND Z |
| L | X | X | X | Z | Z |
| X | L | X | X | Z | Z |
| H | H | L | X | L | H |
| H | H | X | L | L | H |
| H | H | H | H | H | L |

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)
† B input and 4th line of function table are applicable only to driver number 1.

## logic symbol‡

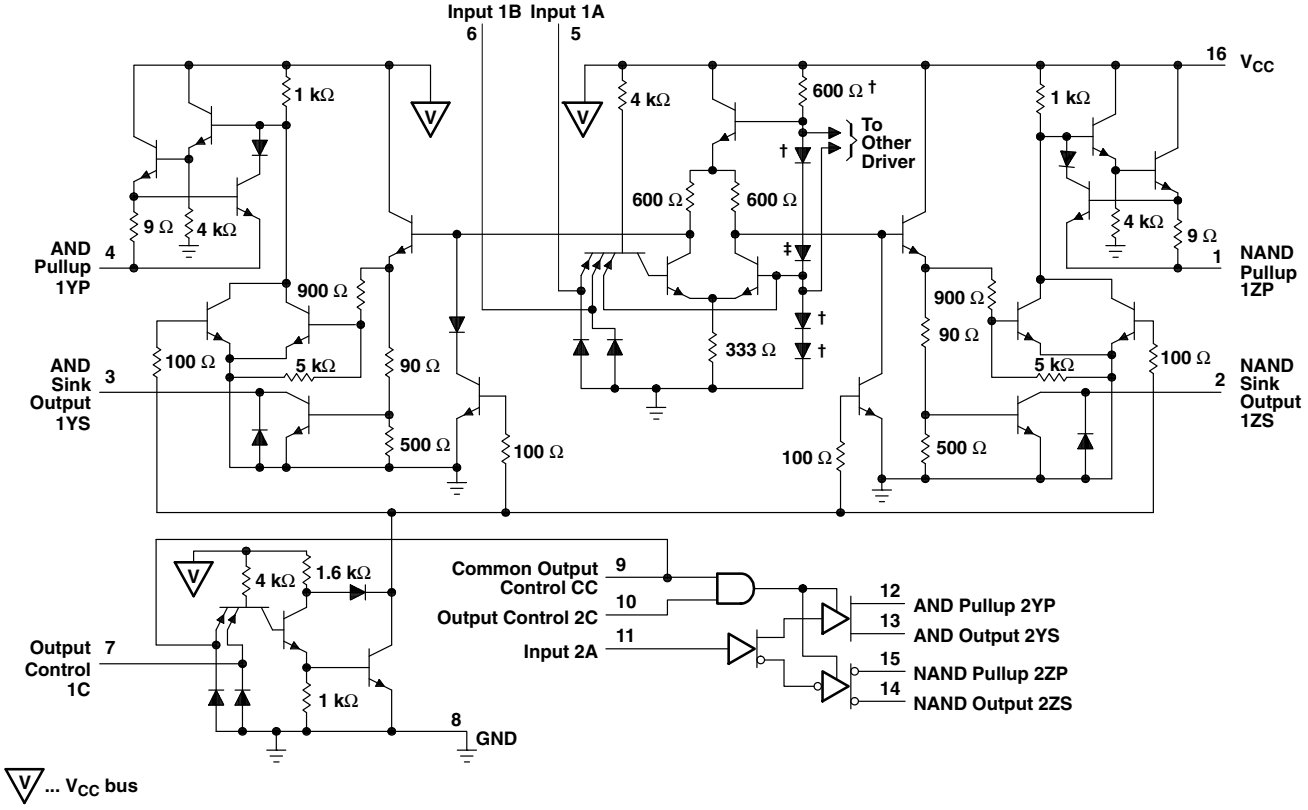



## logic diagram (positive logic)




‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the J, N, and W packages.

## schematic




† These components are common to both drivers. Resistor values shown are nominal and in ohms.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage, $V_I$ . . . . . 5.5 V
Off-state voltage applied to open-collector outputs . . . . . 12 V
Continuous total power dissipation (see Note 2) . . . . . See Dissipation Rating Table
Operating free-air temperature range, $T_A$: SN55113 . . . . . −55°C to 125°C
SN75113 . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package . . . . . 260°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package . . . . . 300°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW | 275 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | N/A |
| W | 1000 mW | 8.0 mW/°C | 640 mW | 200 mW |

## recommended operating conditions

| | SN55113 | | | SN75113 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | 2 | | | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | 0.8 | | | 0.8 | V |
| High-level output current, $I_{OH}$ | | | – 40 | | | – 40 | mA |
| Low-level output current, $I_{OL}$ | | | 40 | | | 40 | mA |
| Operating free-air temperature, $T_A$ | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | | SN55113 | | | SN75113 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = –12 mA | | | | –0.9 | –1.5 | | –0.9 | –1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = 0.8 V, $V_{IH}$ = 2 V, | | $I_{OH}$ = –10 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | | | $I_{OH}$ = –40 mA | 2 | 3.0 | | 2 | 3.0 | | |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $I_{OL}$ = 40 mA, $V_{IH}$ = 2 V, | | $V_{IL}$ = 0.8 V, | | 0.23 | 0.4 | | 0.23 | 0.4 | V |
| $V_{OK}$ | Output clamp voltage | | $V_{CC}$ = MAX, $I_O$ = – 40 mA | | | | –1.1 | –1.5 | | –1.1 | –1.5 | V |
| $I_{O(off)}$ | Off-state open-collector output current | | $V_{CC}$ = MAX | $V_{OH}$ = 12 V | $T_A$ = 25°C | | 1 | 10 | | | | μA |
| | | | | | $T_A$ = 125°C | | | 200 | | | | |
| | | | | $V_{OH}$ = 5.25 V | $T_A$ = 25°C | | | | | 1 | 10 | |
| | | | | | $T_A$ = 70°C | | | | | | 20 | |
| $I_{OZ}$ | Off-state (high-impedance-state) output current | | $V_{CC}$ = MAX, Output controls at 0.8 V | $T_A$ = 25°C, $V_O$ = 0 to $V_{CC}$ | | | | ±10 | | | ±10 | μA |
| | | | | $T_A$ = MAX | $V_O$ = 0 | | | –150 | | | –20 | |
| | | | | | $V_O$ = 0.4 V | | | ±80 | | | ±20 | |
| | | | | | $V_O$ = 2.4 V | | | ±80 | | | ±20 | |
| | | | | | $V_O$ = $V_{CC}$ | | | 80 | | | 20 | |
| $I_I$ | Input current at maximum input voltage | A, B, C | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | | 1 | | | 1 | mA |
| | | CC | | | | | | 2 | | | 2 | |
| $I_{IH}$ | High-level input current | A, B, C | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | | 40 | | | 40 | μA |
| | | CC | | | | | | 80 | | | 80 | |
| $I_{IL}$ | Low-level input current | A, B, C | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | | –1.6 | | | –1.6 | mA |
| | | CC | | | | | | –3.2 | | | –3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX, $V_O$ = 0, | | $T_A$ = 25°C | –40 | –90 | –120 | –40 | –90 | –120 | mA |
| $I_{CC}$ | Supply current (both drivers) | | All inputs at 0 V, No load, $T_A$ = 25°C | | $V_{CC}$ = MAX | | 47 | 65 | | 47 | 65 | mA |
| | | | | | $V_{CC}$ = 7 V | | 65 | 85 | | 65 | 85 | |

† All parameters with the exception of off-state open-collector output current are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

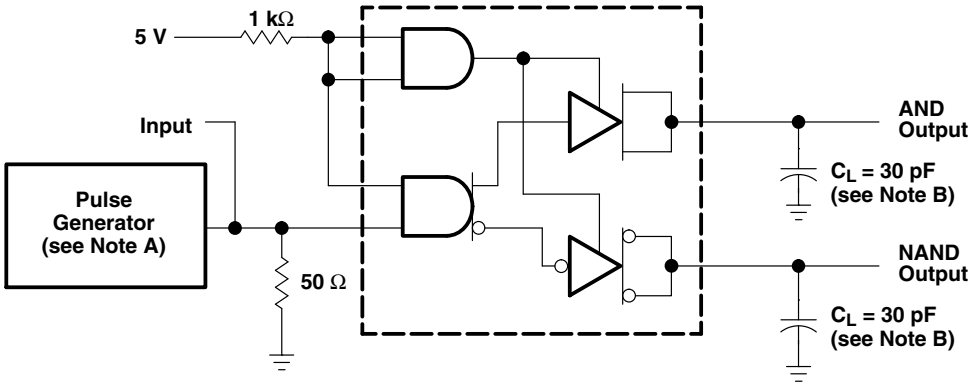
‡ All typical values are at $T_A$ = 25°C and $V_{CC}$ = 5 V, with the exception of $V_{CC}$ at 7 V.

§ Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

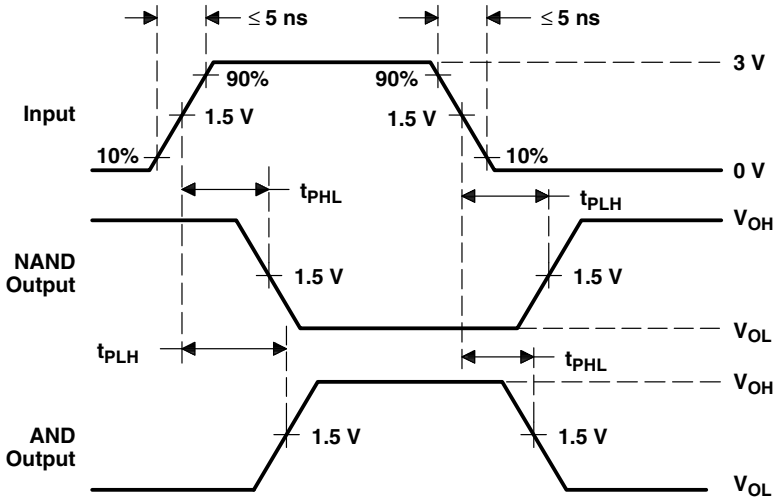
## switching characteristics, $V_{CC}$ = 5 V, $C_L$ = 30 pF, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | SN55113 | | | SN75113 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | Propagation delay time, low-to-high level output | See Figure 1 | | 13 | 20 | | 13 | 30 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 12 | 20 | | 12 | 30 | ns |
| $t_{PZH}$ | Output enable time to high level | $R_L$ = 180 Ω, See Figure 2 | | 7 | 15 | | 7 | 20 | ns |
| $t_{PZL}$ | Output enable time to low level | $R_L$ = 250 Ω, See Figure 3 | | 14 | 30 | | 14 | 40 | ns |
| $t_{PHZ}$ | Output disable time from high level | $R_L$ = 180 Ω, See Figure 2 | | 10 | 20 | | 10 | 30 | ns |
| $t_{PLZ}$ | Output disable time from low level | $R_L$ = 250 Ω, See Figure 3 | | 17 | 35 | | 17 | 35 | ns |

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

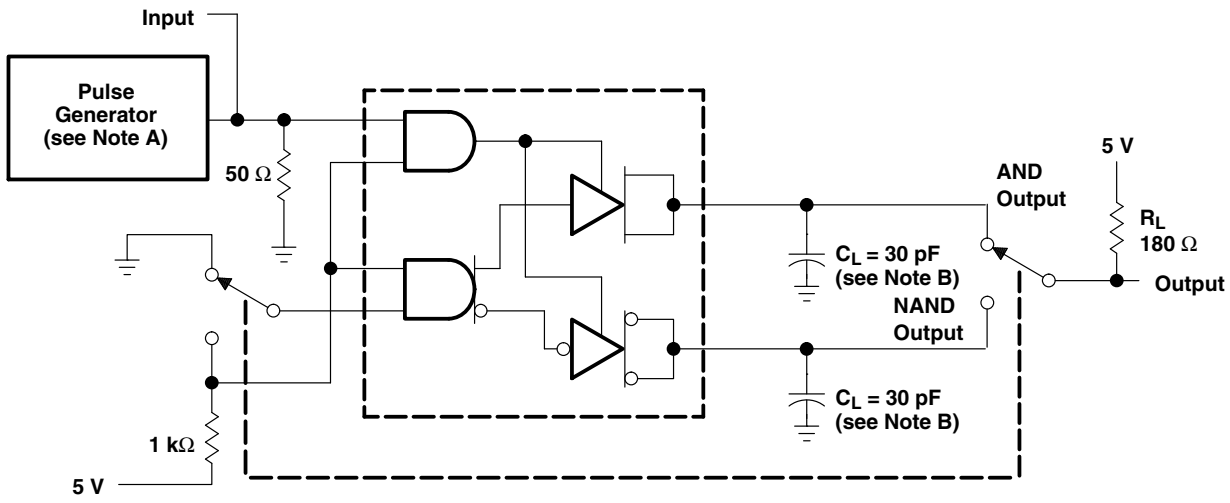



VOLTAGE WAVEFORMS

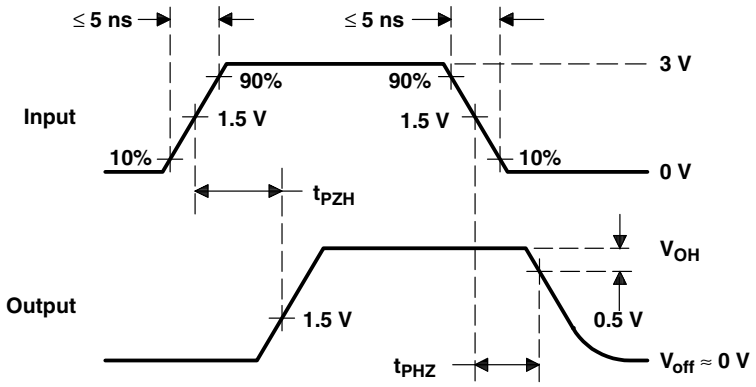
NOTES: A. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, PRR ≤ 500 kHz, $t_w$ = 100 ns.
B. $C_L$ includes probe and jig capacitance.

**Figure 1. Test Circuit and Voltage Waveforms $t_{PLH}$ and $t_{PHL}$**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT

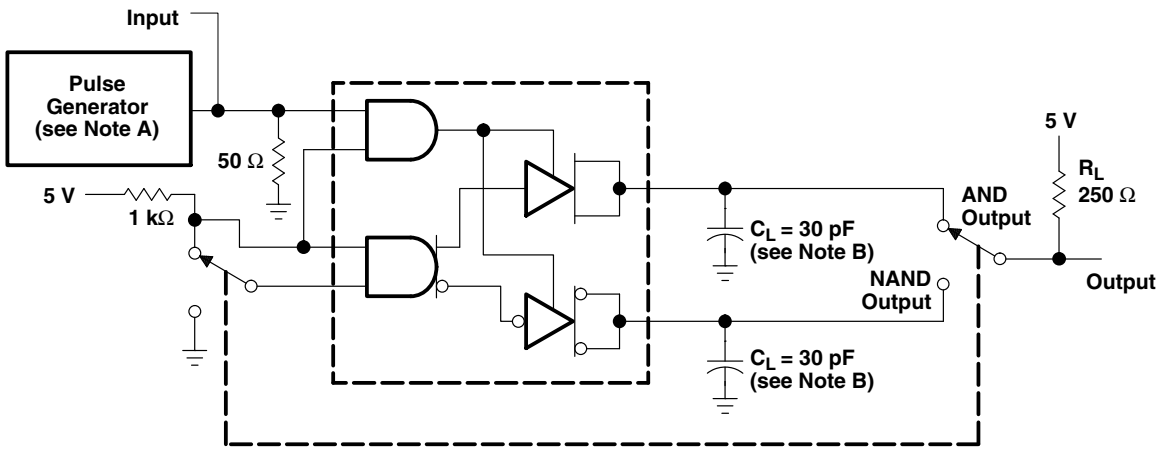



VOLTAGE WAVEFORMS

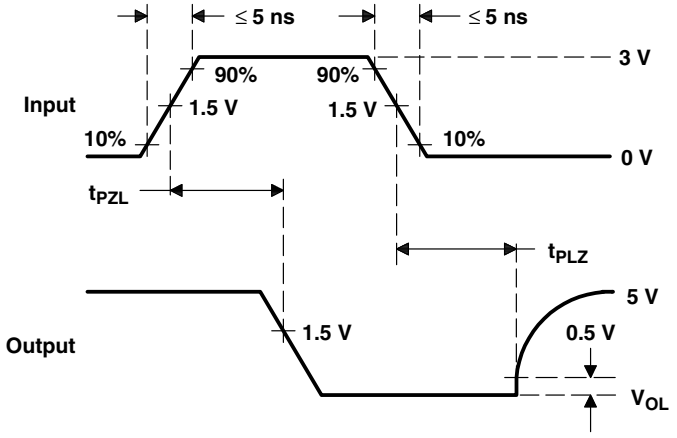
NOTES: A. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, PRR ≤ 500 kHz, $t_w$ = 100 ns.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Test Circuit and Voltage Waveforms $t_{PZH}$ and $t_{PHZ}$**

## PARAMETER MEASUREMENT INFORMATION




TEST CIRCUIT




VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_O$ = 50 Ω, PRR ≤ 500 kHz, $t_w$ = 100 ns.
B. $C_L$ includes probe and jig capacitance.

**Figure 3. Test Circuit and Voltage Waveforms, $t_{PZL}$ and $t_{PLZ}$**

## TYPICAL CHARACTERISTICS†

**OUTPUT VOLTAGE vs DATA INPUT VOLTAGE**

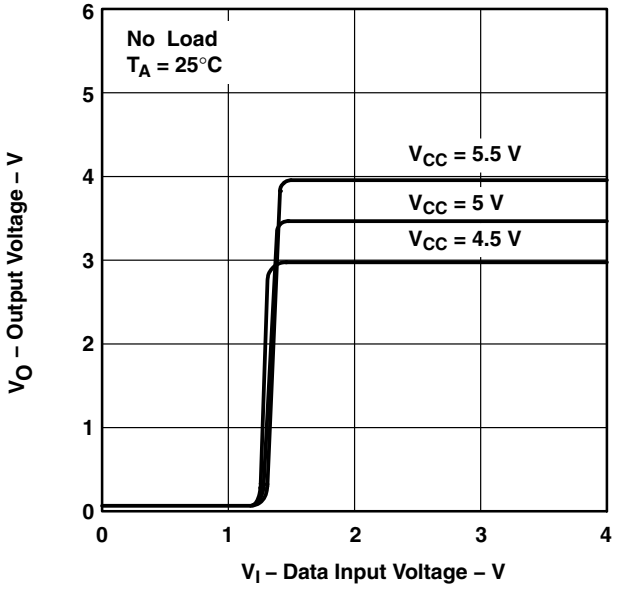



Figure 4

**OUTPUT VOLTAGE vs DATA INPUT VOLTAGE**

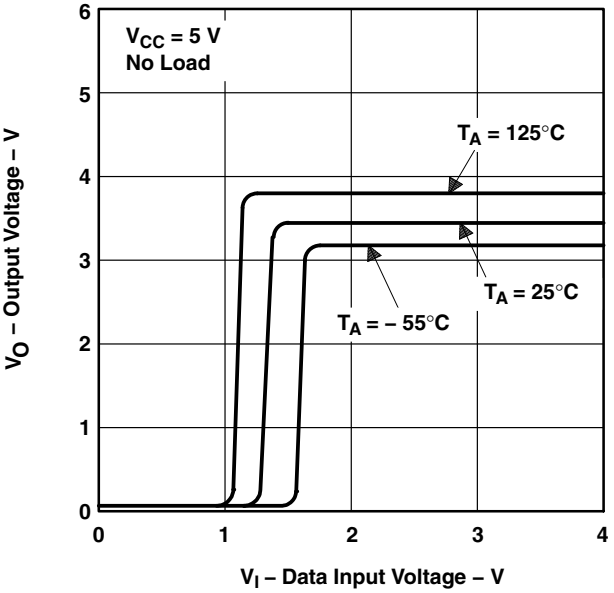



Figure 5

**OUTPUT VOLTAGE vs INPUT VOLTAGE (OUTPUT CONTROL)**

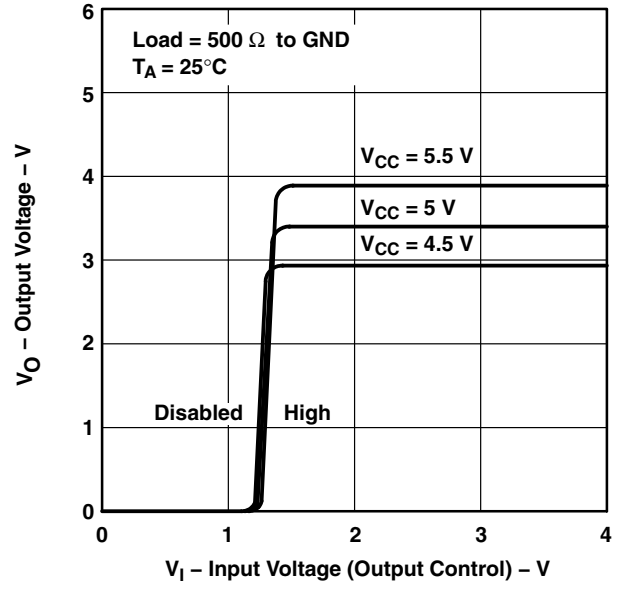



Figure 6

**OUTPUT VOLTAGE vs INPUT VOLTAGE (OUTPUT CONTROL)**

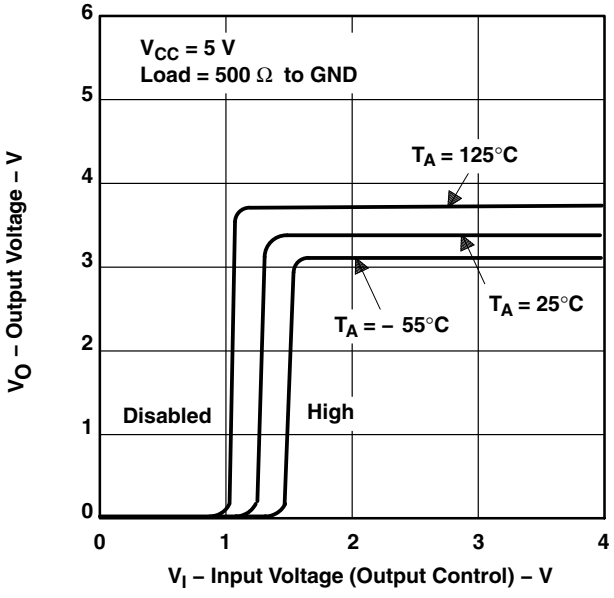



Figure 7

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

## TYPICAL CHARACTERISTICS†

**OUTPUT VOLTAGE vs INPUT VOLTAGE (OUTPUT CONTROL)**

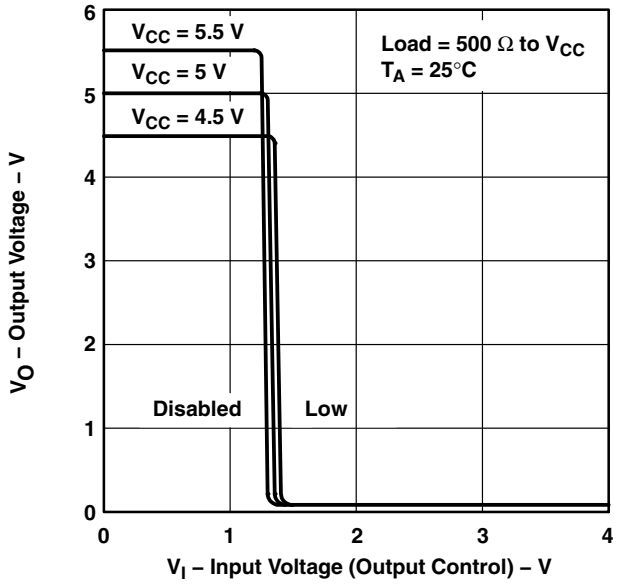



Figure 8

**OUTPUT VOLTAGE vs INPUT VOLTAGE (OUTPUT CONTROL)**

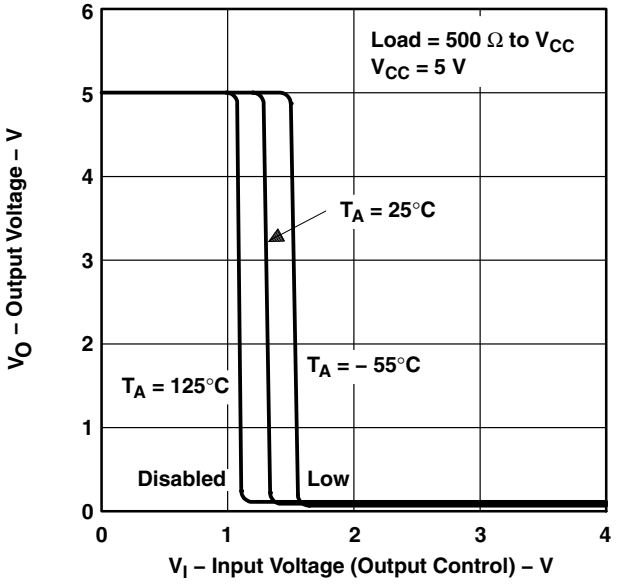



Figure 9

**OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

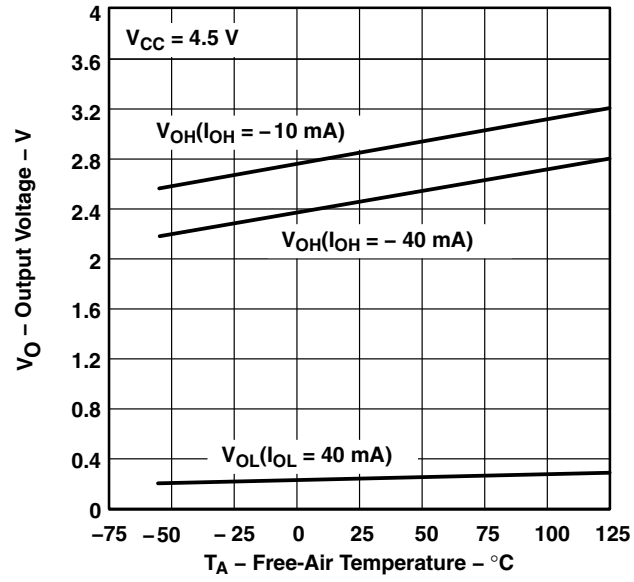



Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT**

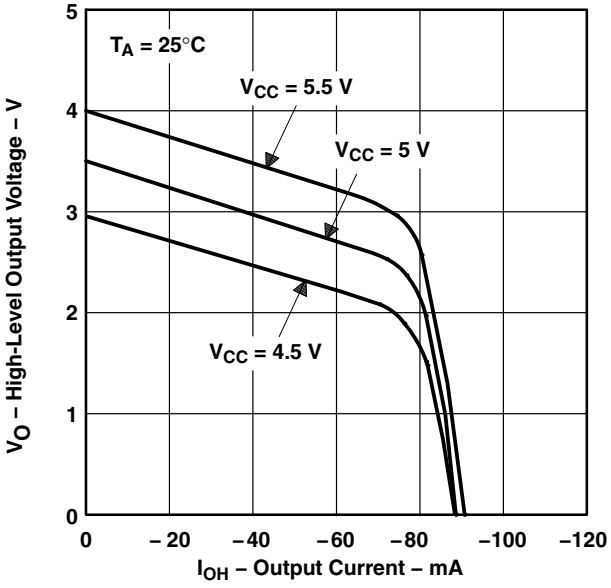



Figure 11

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

## TYPICAL CHARACTERISTICS†

**LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT**

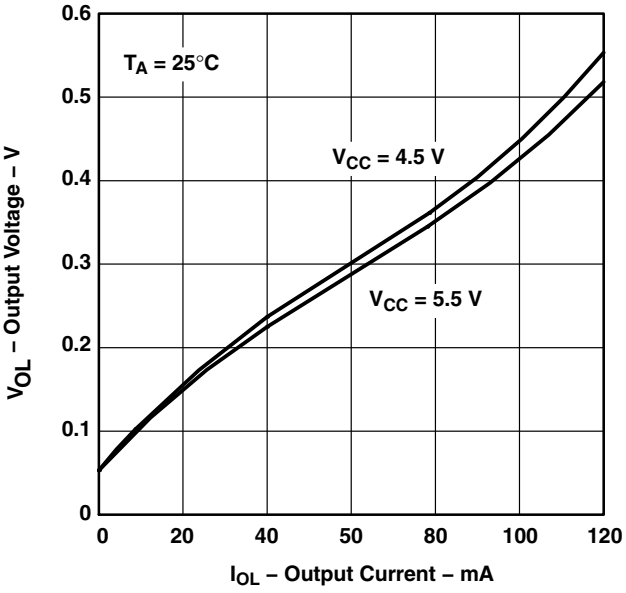



Figure 12

**SUPPLY CURRENT (BOTH DRIVERS) vs SUPPLY VOLTAGE**

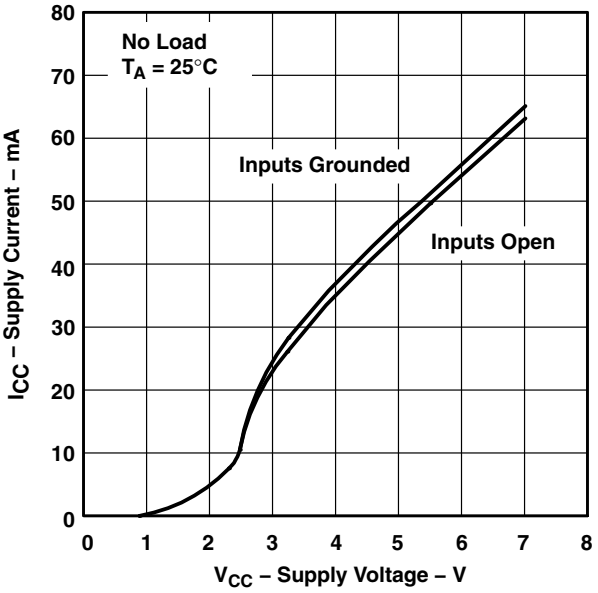



Figure 13

**SUPPLY CURRENT (BOTH DRIVERS) vs OUTPUT CURRENT**

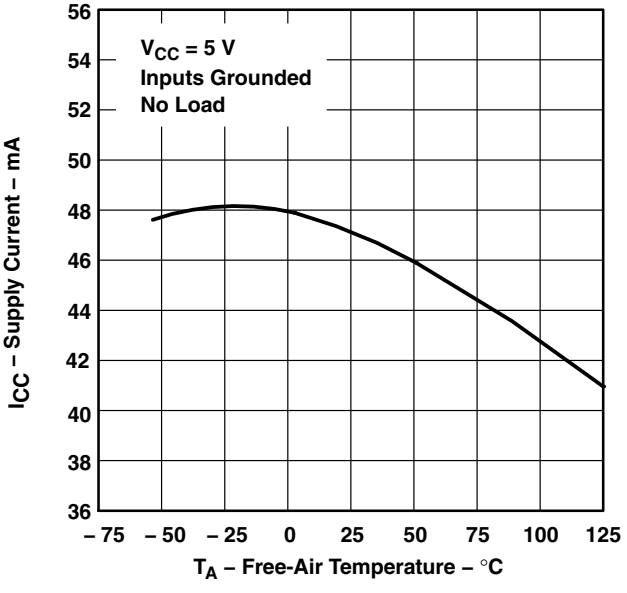



Figure 14

**SUPPLY CURRENT (BOTH DRIVERS) vs SUPPLY VOLTAGE**

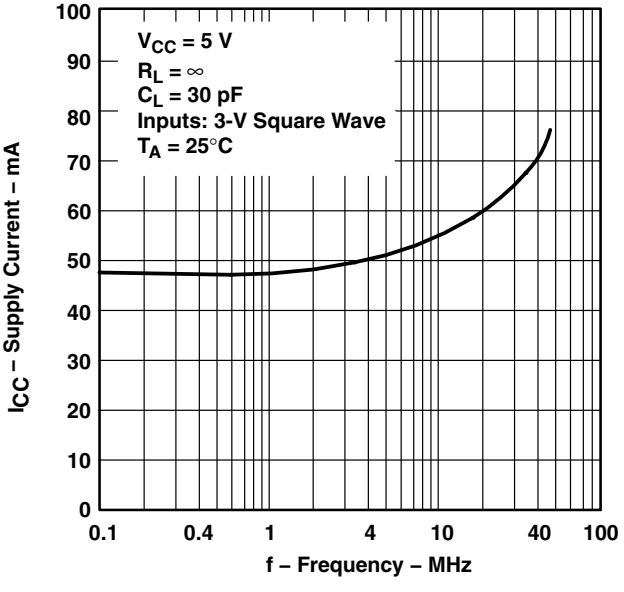



Figure 15

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

## TYPICAL CHARACTERISTICS†

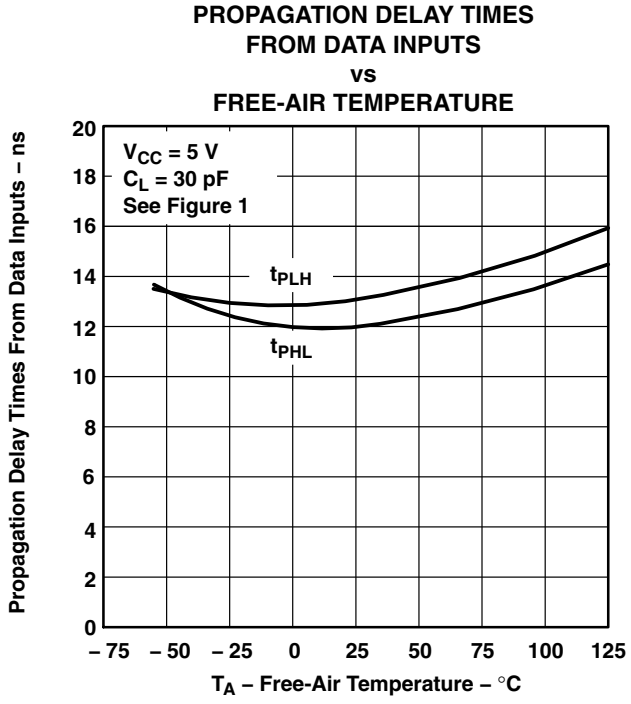



Figure 16

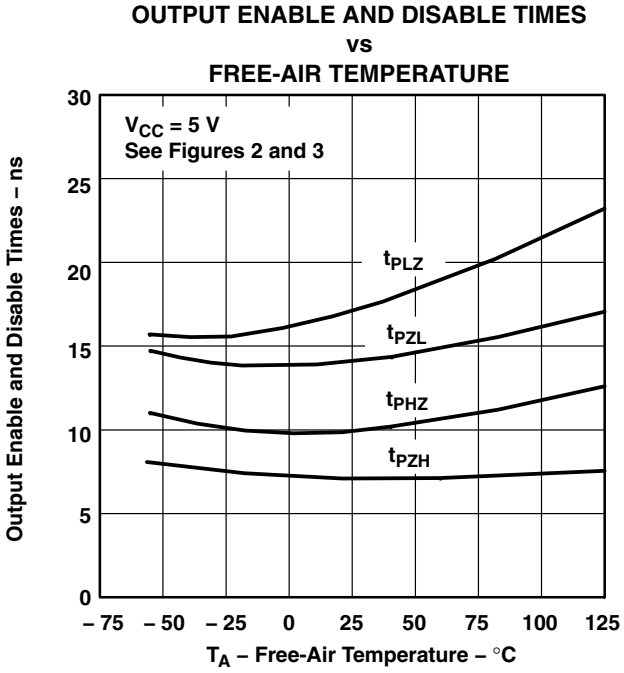
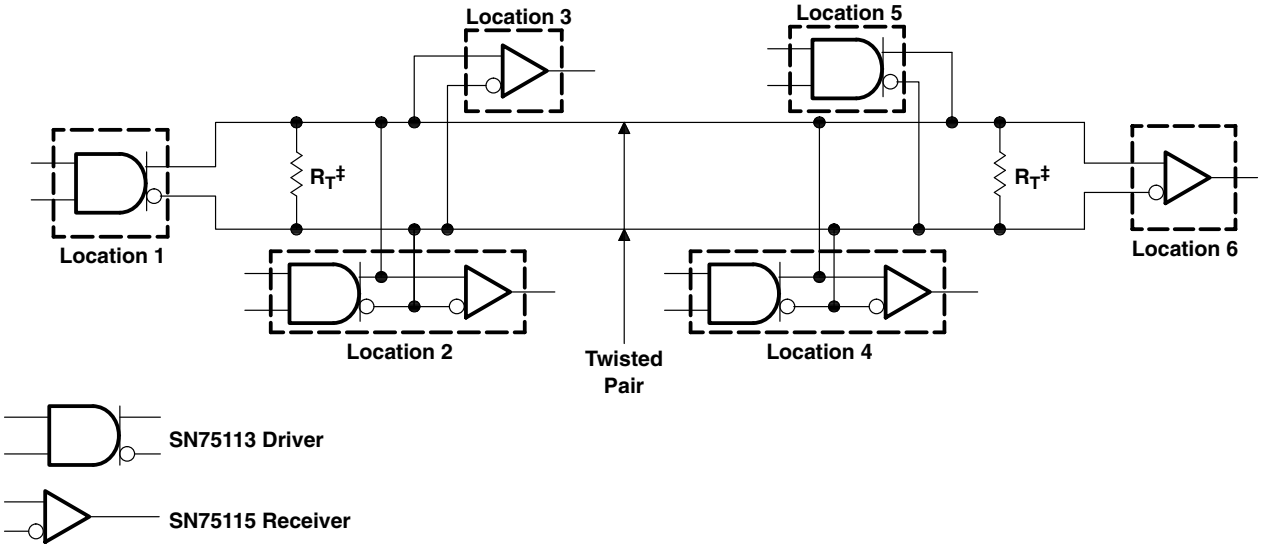



Figure 17

† Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pullup connected to the sink output.

## APPLICATION INFORMATION




‡ $R_T = Z_O$. A capacitor may be connected in series with $R_T$ to reduce power dissipation.

**Figure 18. Basic Party-Line or Data-Bus Differential Data Transmission**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-88744012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-88744012A SNJ55 113FK |
| 5962-8874401EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874401EA SNJ55113J |
| 5962-8874401FA | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874401FA SNJ55113W |
| JM38510/10405BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510 /10405BEA |
| SN55113J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN55113J |
| SN75113N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN75113N |
| SN75113NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75113 |
| SNJ55113FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-88744012A SNJ55 113FK |
| SNJ55113J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874401EA SNJ55113J |
| SNJ55113W | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8874401FA SNJ55113W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN55113, SN75113 :**

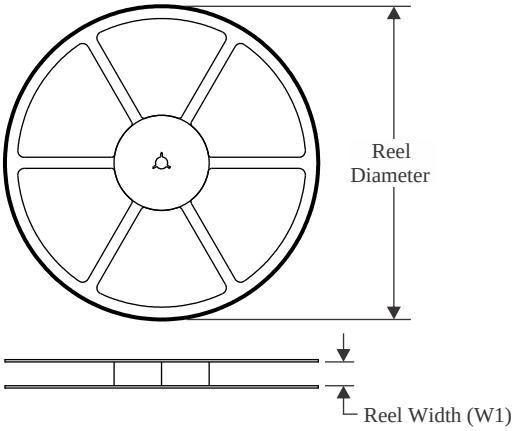
- Catalog : SN75113
- Military : SN55113

NOTE: Qualified Version Definitions:

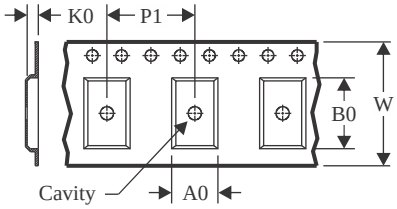
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

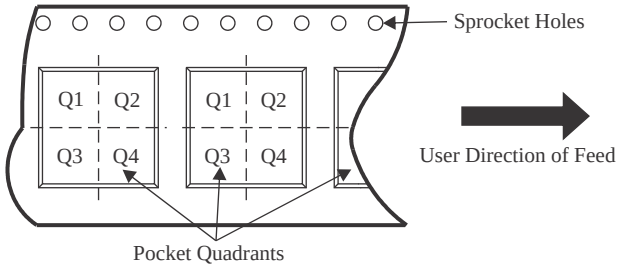



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

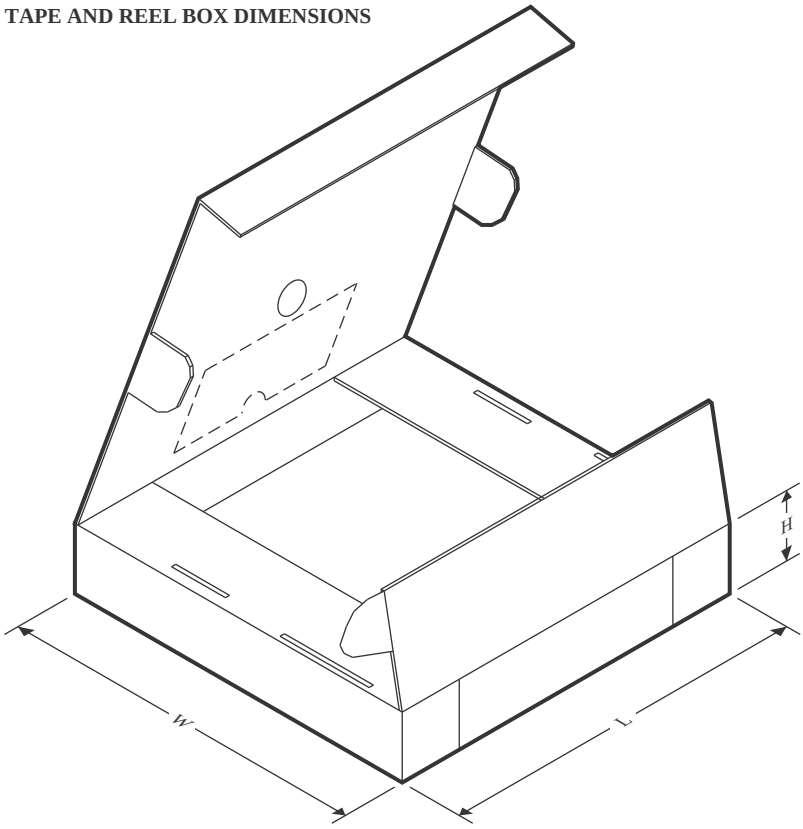
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75113NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

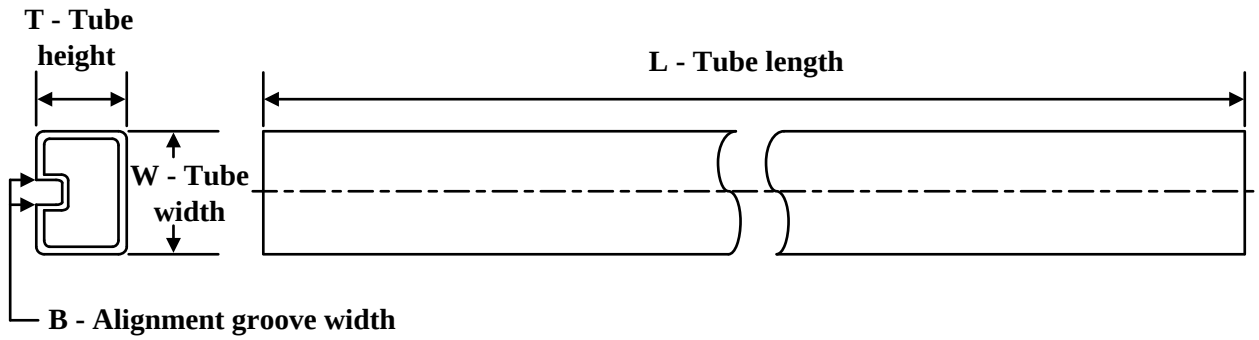
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75113NSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |

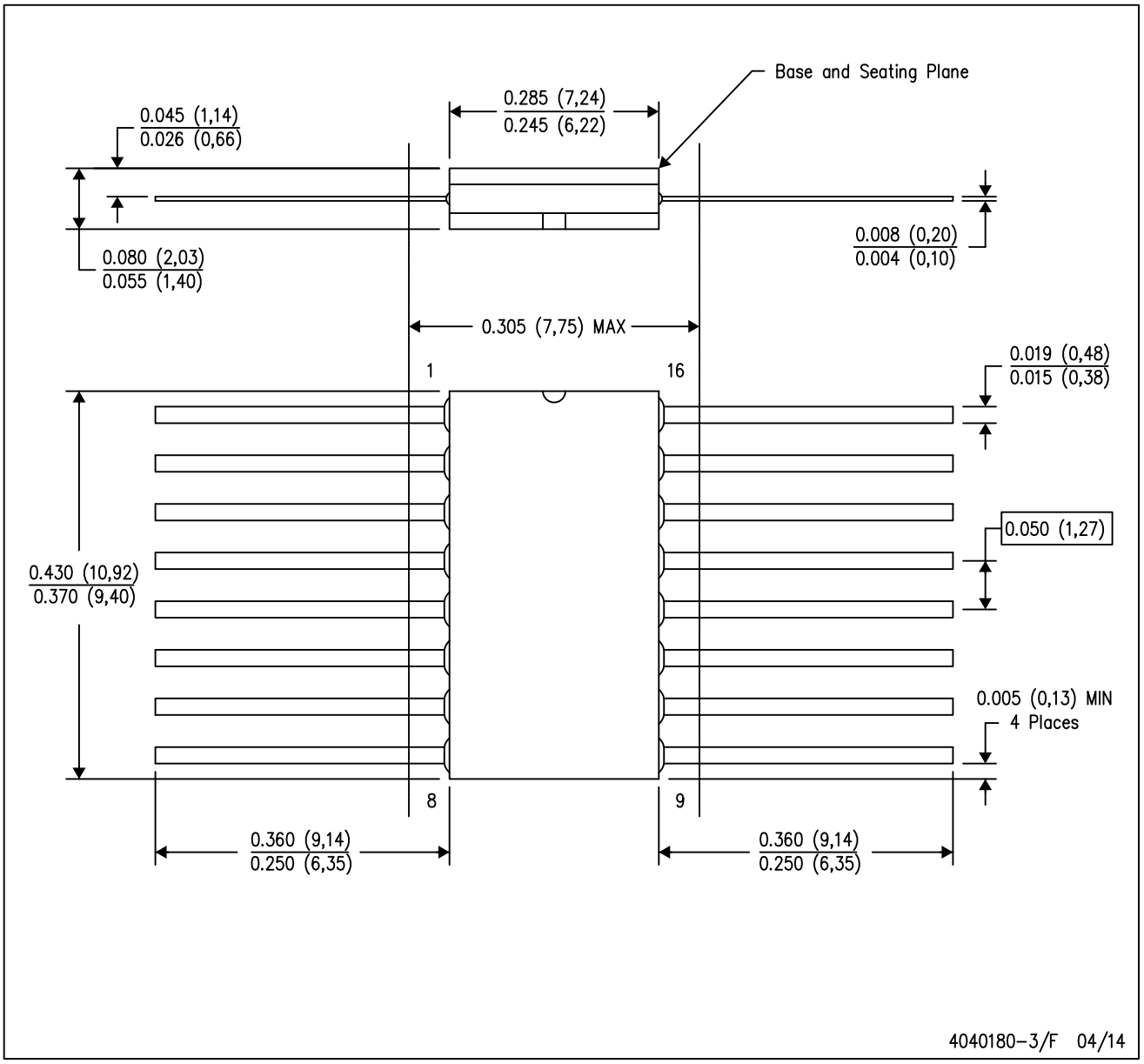
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-88744012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8874401FA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN75113N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75113NE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ55113FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ55113W | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F16) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

# GENERIC PACKAGE VIEW

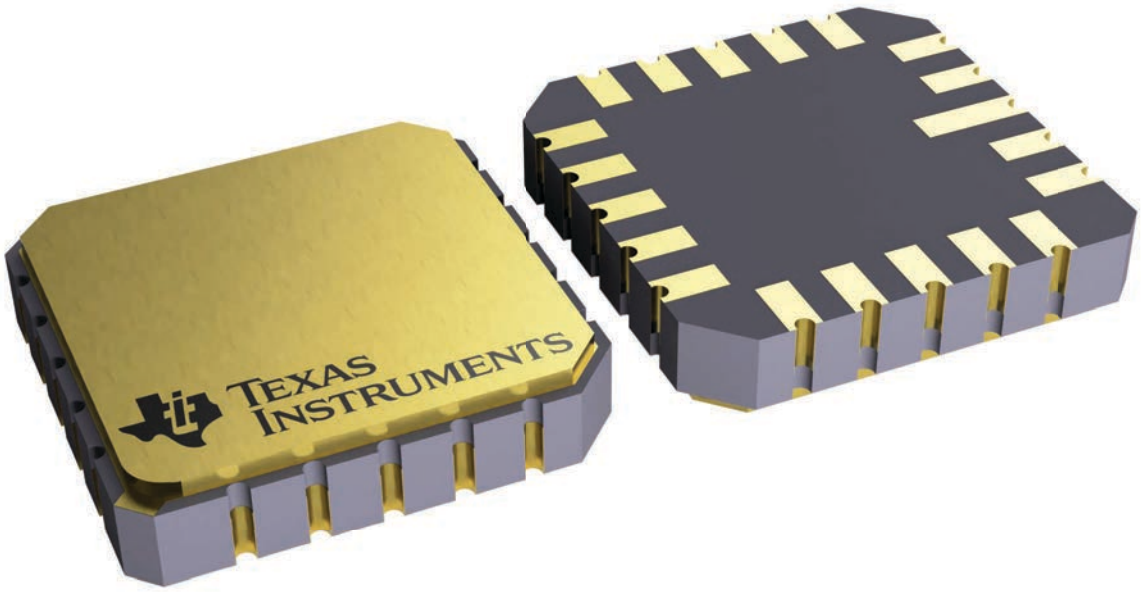
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

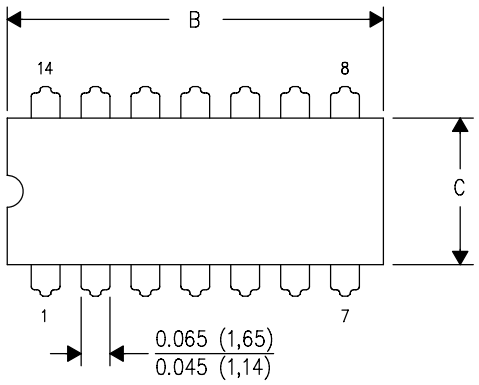



4229370VA\

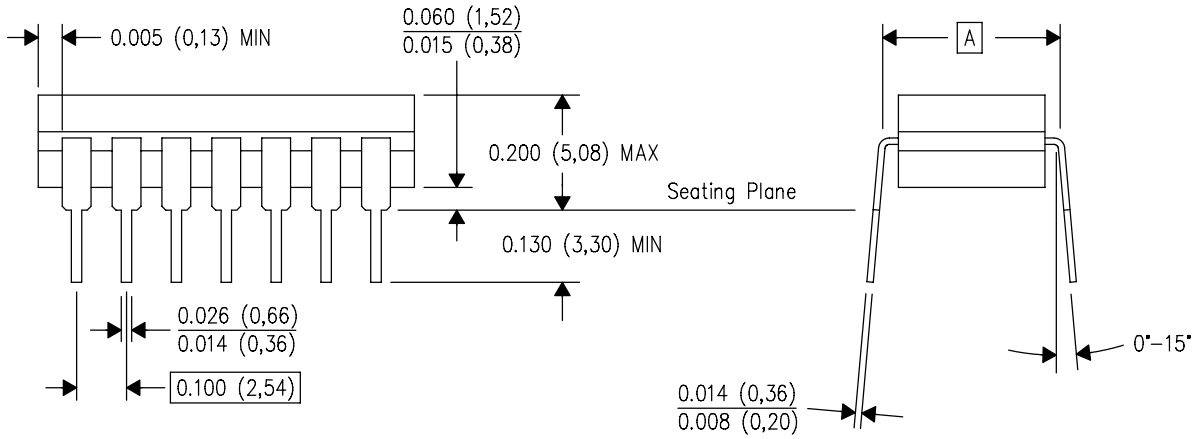
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



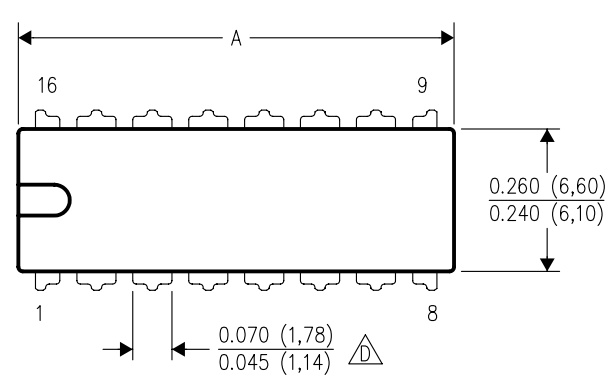

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

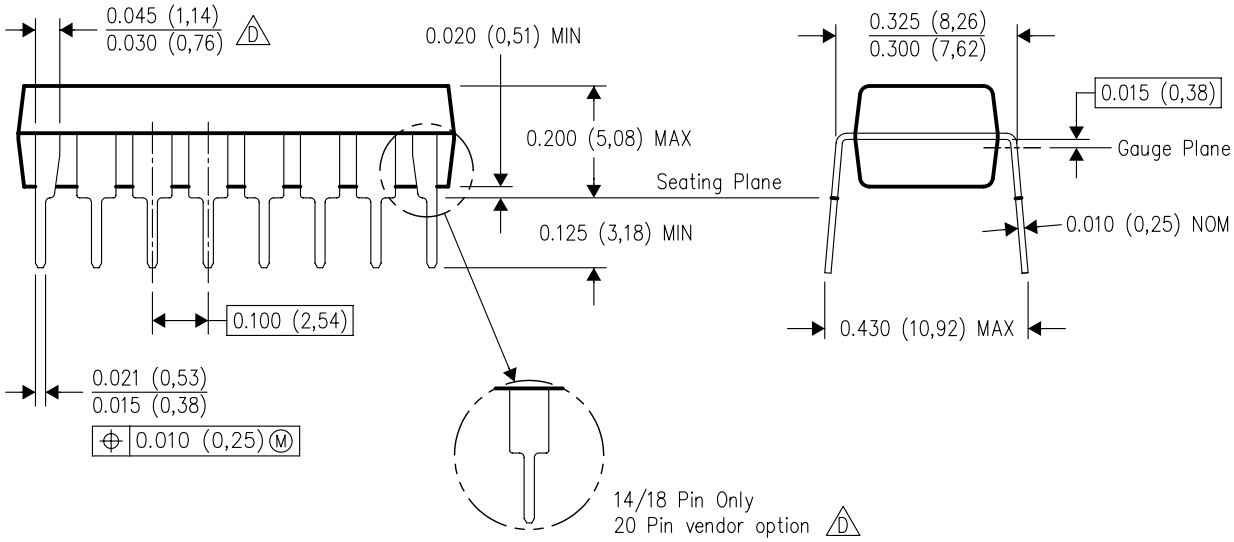
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

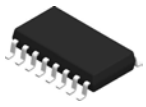



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

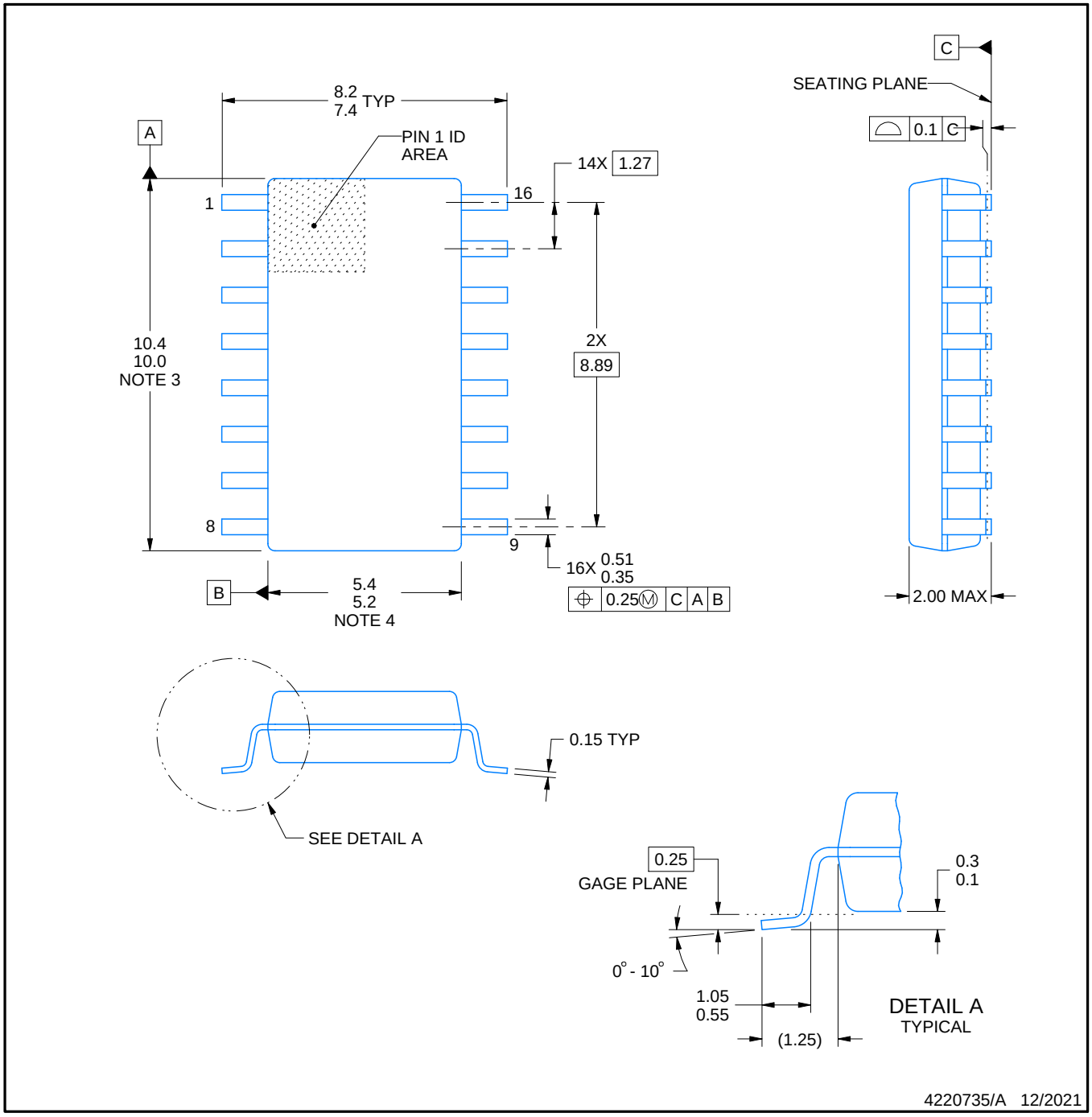


# PACKAGE OUTLINE

## NS0016A

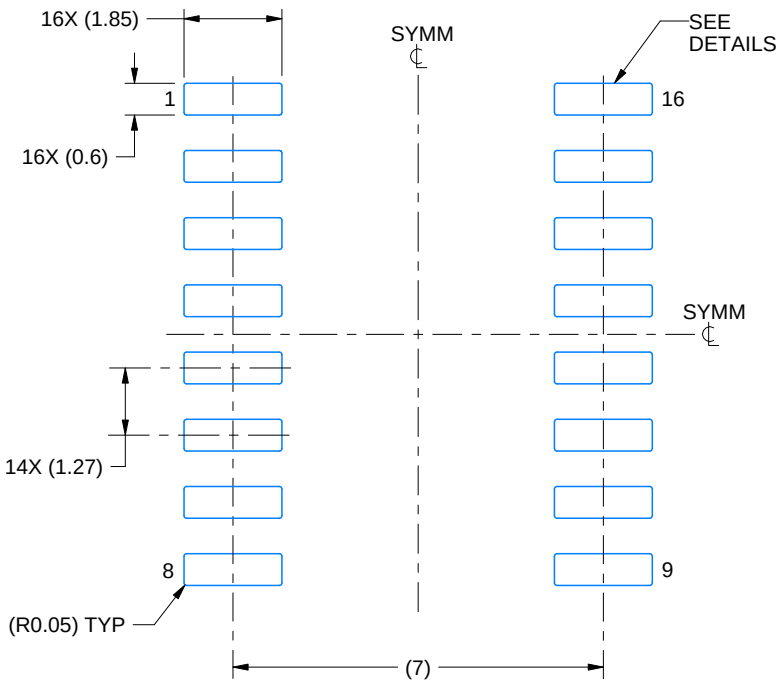
## SOP - 2.00 mm max height

SOP

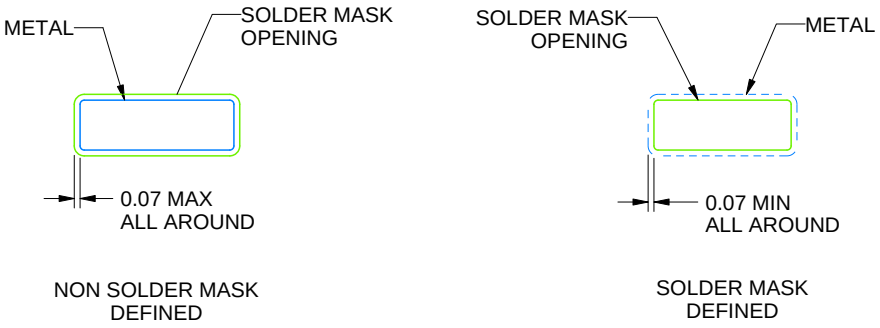



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

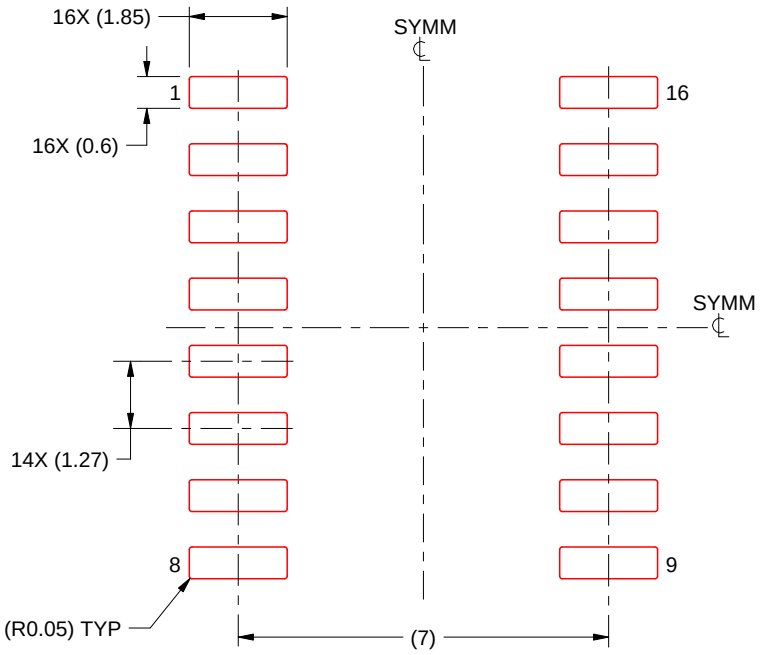
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

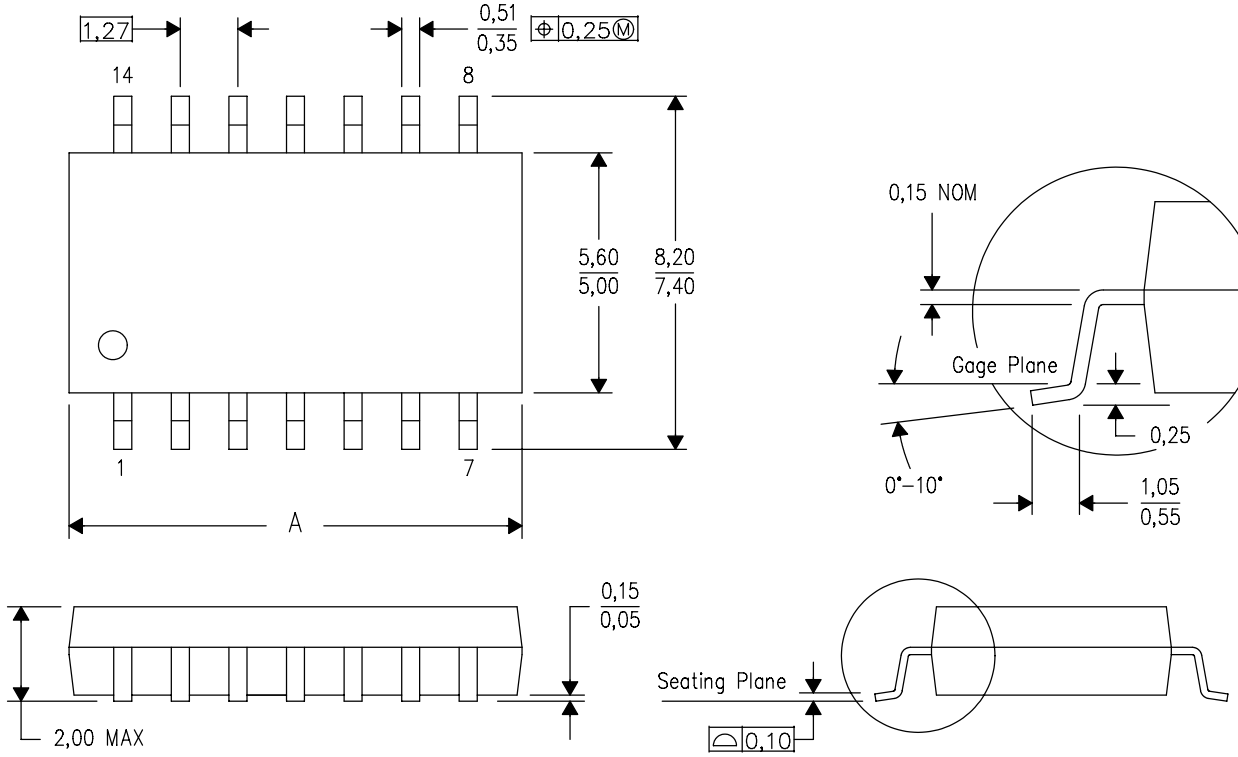
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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