

SILICON GATE CMOS

32,768 WORD x 8 BIT STATIC RAM

Description

The TC55257DPI is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (typ.) and a minimum cycle time of 70ns.

When \overline{CE} is a logical high, the device is placed in a low power standby mode in which the standby current is 0.3 μ A typically. The TC55257DPI has two control inputs. Chip Enable (\overline{CE}) allows for device selection and data retention control, and an Output Enable input (\overline{OE}) provides fast memory access. The TC55257DPI is suitable for use in microprocessor application systems where high speed, low power, and battery backup are required. The TC55257DPI is guaranteed over an operating temperature range of -40 ~ 85°C so the TC55257DPI is suitable for use in wide operating temperature systems.

The TC55257DPI is offered in a standard dual-in-line 28-pin plastic package (0.6 inch width), a small outline plastic package, and a thin small outline plastic package (forward type).

Features

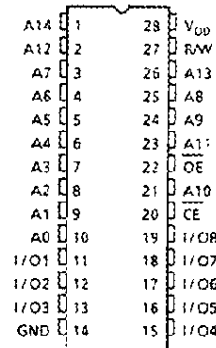
- Low power dissipation: 27.5mW/MHz (typ.)
- Standby current: 2 μ A (max.) at Ta = 25°C
- 5V single power supply
- Access time (max.)

	TC55257DPI/DFI/DFTI	
	-70L	-85L
Access Time	70ns	85ns
\overline{CE} Access Time	70ns	85ns
\overline{OE} Access Time	35ns	45ns

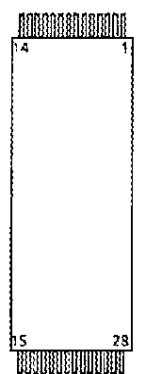
- Power down feature: \overline{CE}
- Data retention supply voltage: 2.0 ~ 5.5V
- Inputs and outputs directly TTL compatible
- Wide operating temperature: -40 ~ 85°C
- Package
 - TC55257DPI : DIP28-P-600
 - TC55257DFI : SOP28-P-450
 - TC55257DFTI : TSOP28-P

Pin Connection (Top View)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP (forward type)



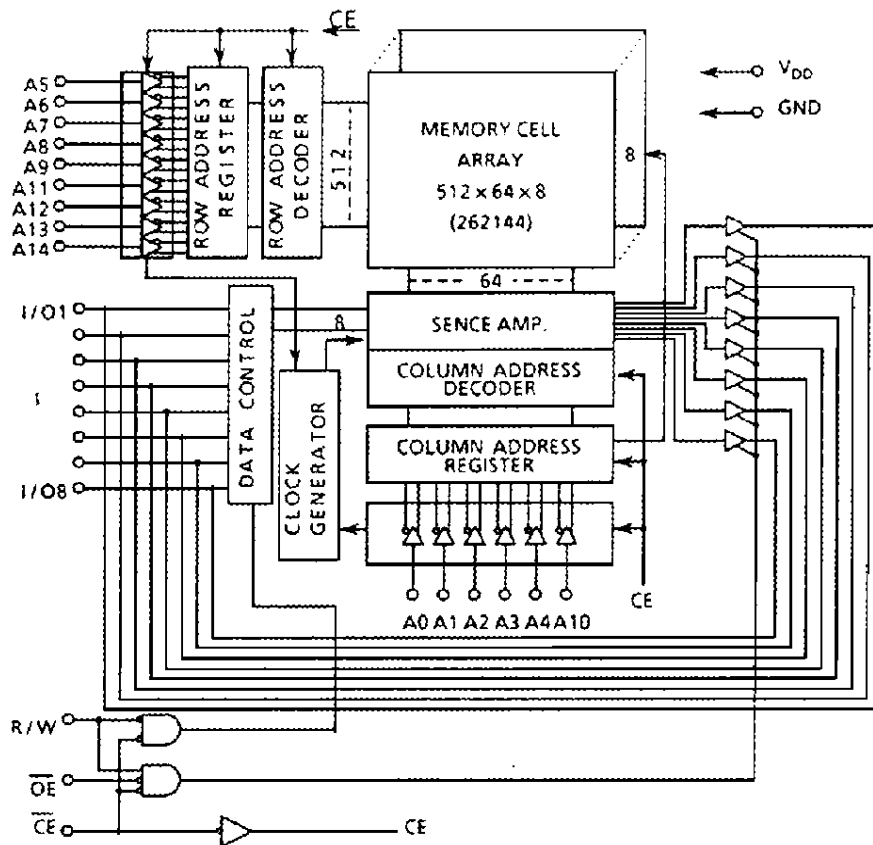
Pin Names

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
\overline{OE}	Output Enable Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Input/Output
V _{DD}	Power (+5V)
GND	Ground

TSOP Pinout

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	\overline{OE}	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V _{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	\overline{CE}	A ₁₀

Block Diagram



Operating Mode

OPERATION MODE	\overline{CE}	\overline{OE}	R/W	I/O1 ~ I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	High-Z	I _{DDO}
Standby	H	*	*	High-Z	I _{DDs}

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V _{IN}	Input Voltage	-0.3* ~ 7.0	V
V _{IO}	Input and Output Voltage	-0.5* ~ V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{SOLDER}	Soldering Temperature (10 s)	260	°C
T _{STRG}	Storage Temperature	-55 ~ 150	°C
T _{OPR}	Operating Temperature	-40 ~ 85	°C

* -3.0V at pulse width 50ns

** SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0V at pulse width 50ns

DC and Operating Characteristics ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	± 1.0	μA	
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$	–	–	± 1.0	μA	
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	–	–	mA	
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	4.0	–	–	mA	
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$ Other Input = V_{IH}/V_{IL} $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	–	10	–	mA
			$t_{\text{cycle}} = \text{Min. cycle}$	–	–	70	
I_{DDO2}	Operating Current	$\overline{CE} = 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$ Other Input = $V_{DD} - 0.2\text{V}/0.2\text{V}$ $I_{OUT} = 0\text{mA}$	$t_{\text{cycle}} = 1\mu\text{s}$	–	5	–	
			$t_{\text{cycle}} = \text{Min. cycle}$	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$	–	–	3	mA	
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2\text{V}$ $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$	$T_a = -40 \sim 85^\circ\text{C}$	–	–	30	μA
			$T_a = 25^\circ\text{C}$	–	0.3	2	

Capacitance* ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	μF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±10%)**Read Cycle**

SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	–	85	–	ns
t _{ACC}	Address Access Time	–	70	–	85	
t _{CO}	$\overline{\text{CE}}$ Access Time	–	70	–	85	
t _{OE}	Output Enable to Output in Valid	–	35	–	45	
t _{COE}	Chip Enable ($\overline{\text{CE}}$) to Output in Low-Z	5	–	5	–	
t _{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t _{OD}	Chip Enable ($\overline{\text{CE}}$) to Output in High-Z	–	25	–	30	
t _{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t _{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

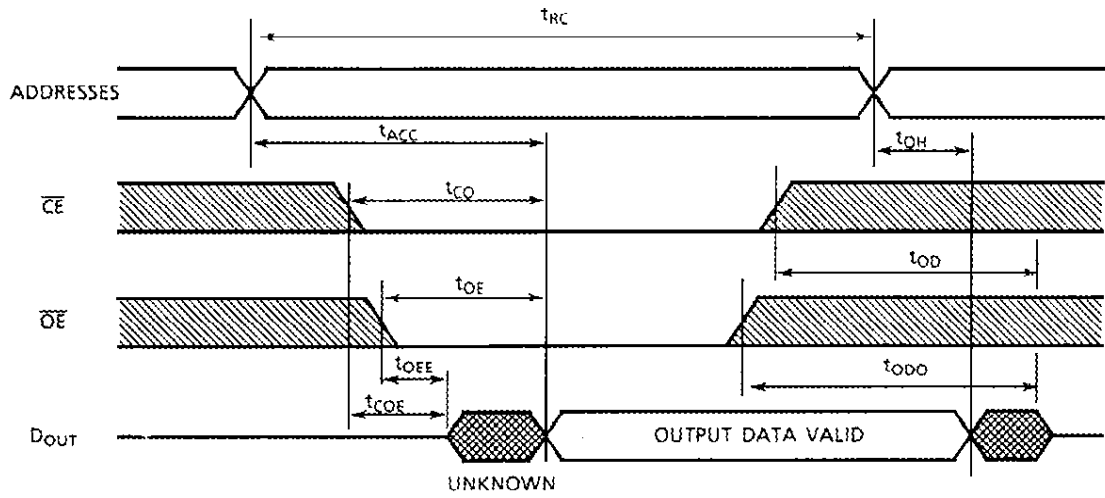
SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI				UNIT
		-70L		-85L		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	–	85	–	ns
t _{WP}	Write Pulse Width	50	–	60	–	
t _{CW}	Chip Selection to End of Write	60	–	65	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W to Output in High-Z	–	25	–	30	
t _{OEW}	R/W to Output in Low-Z	0	–	0	–	
t _{DS}	Data Setup Time	30	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC Test Conditions

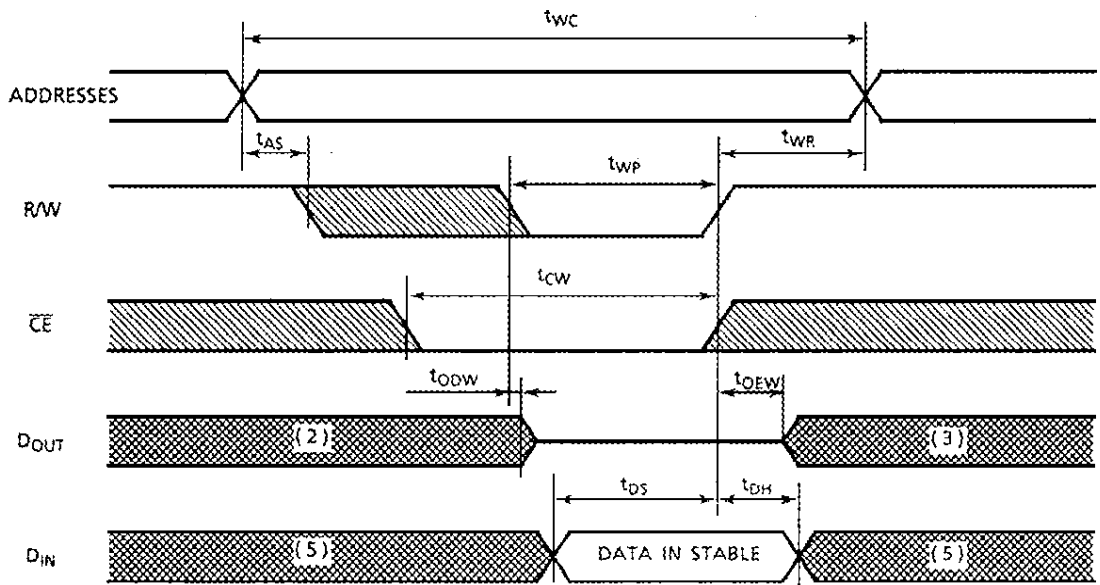
Input Pulse Levels	2.6V/0.4V
Input Pulse Rise and Fall Time	5ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	1 TTL Gate and C _L = 100pF

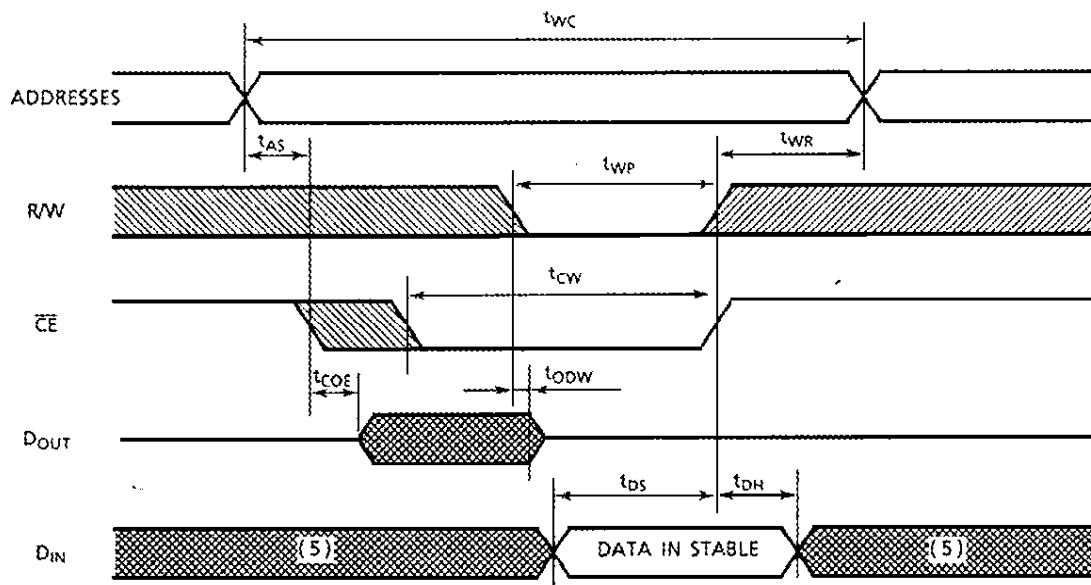
Timing Waveforms

Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 ⁽⁴⁾ ($\overline{\text{CE}}$ Controlled Write)

Notes:

1. R/W is High for read cycle.
2. Assuming that $\overline{\text{CE}}$ Low transition occurs coincident with or after the R/W low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{\text{CE}}$ High transition occurs coincident with or prior to the R/W high transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{\text{OE}}$ is High for a write cycle, the Outputs are in a high impedance state during this period.
5. The I/O may be in the output state during this time; input signals of opposite phase must not be applied.

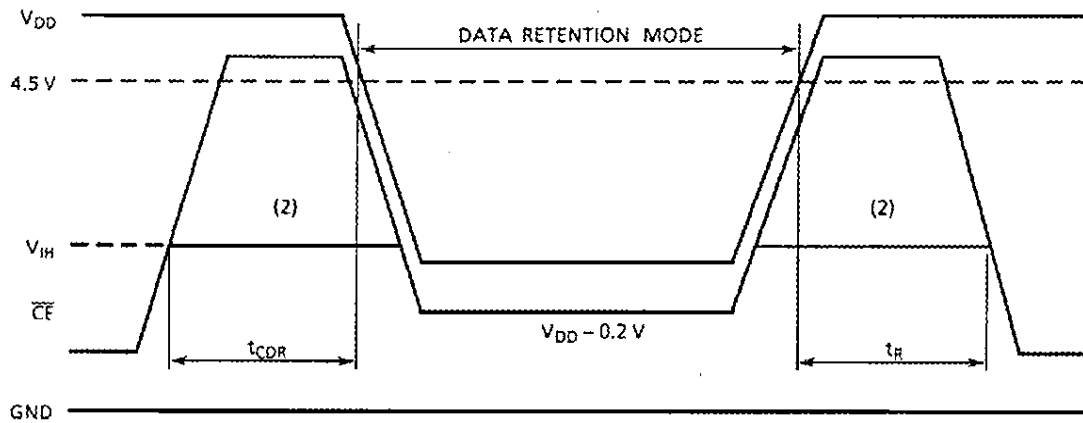
Data Retention Characteristics (Ta = -40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	–	5.5	V
I _{DDs2}	Standby Current	V _{DH} = 3.0V	–	15*	μA
		V _{DH} = 5.5V	–	30	
t _{CDR}	Chip Deselect to Data Retention Mode	0	–	–	ns
t _R	Recovery Time	t _{RC(1)}	–	–	

Note (1): Read Cycle Time

*2μA (max.) Ta = 0 ~ 40°C

\overline{CE} Controlled Data Retention Mode

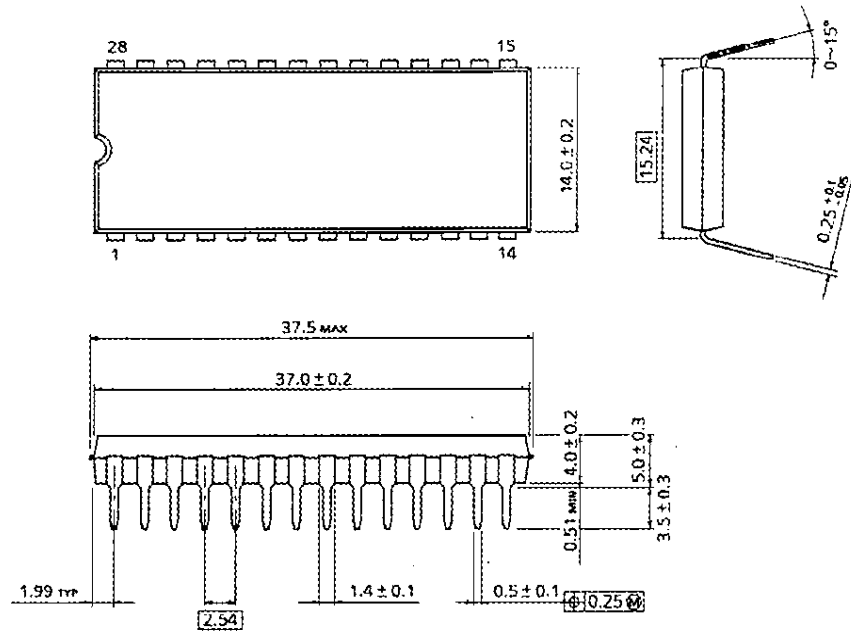


Note (2): If the V_{IH} of \overline{CE} is 2.4V in operation, I_{DDs1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.6V.

Outline Drawing

DIP28-P-600

Unit in mm

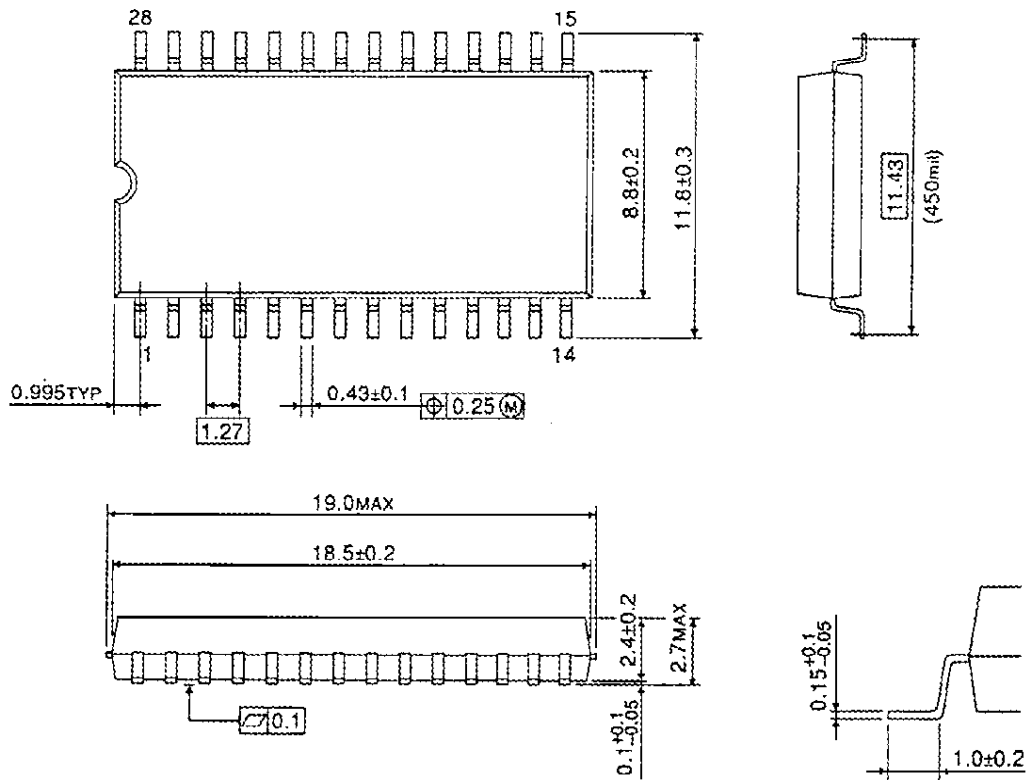


Weight : 4.42g (Typ.)

Outline Drawing

SOP28-P-450

Unit in mm

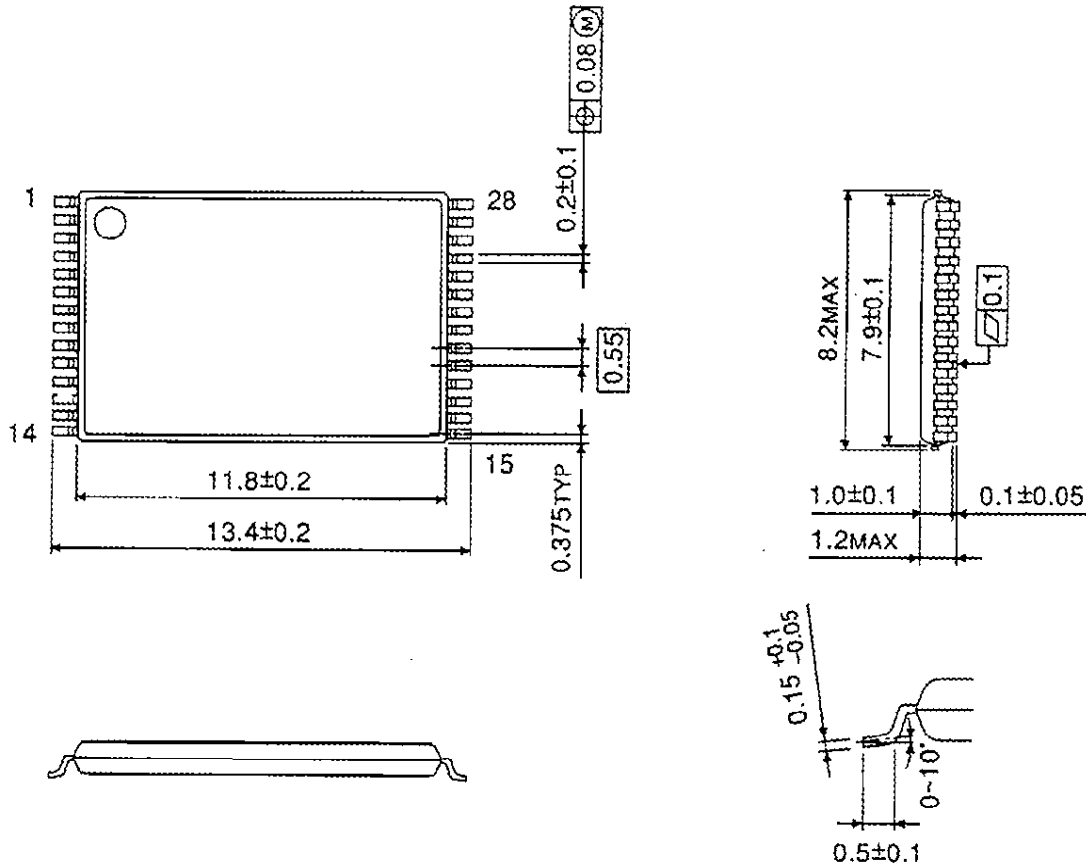


Weight : 0.79g (Typ.)

Outline Drawing

TSOP28-P

Unit in mm



Weight : 0.22g (Typ.)

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