

SILICON STACKED GATE CMOS

1,048,576 WORD x 16 BIT/2,097,152 WORD x 8 BIT CMOS MASK ROM

Description

The TC5316200BP/BF is a 16,777,216 bit read only memory organized as 1,048,576 words by 16 bits when **BYTE** is logical high, and organized as 2,097,152 words by 8 bits when **BYTE** is logical low.

The TC5316200BP/BF is suitable for use as program memory, data memory, or as a character generator.

The TC5316200BP/BF is packaged in a standard 600mil 42-pin DIP or 600mil 44-pin SOP.

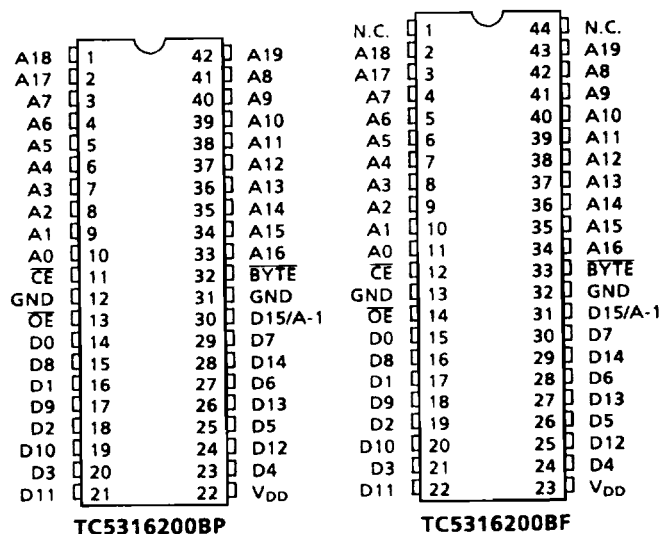
Features

- Single 5V power supply
- Access time : 200ns (max.)
- Power dissipation
 - Operating current : 50mA (max.)
 - Standby current : 100 μ A (max.)
- Fully static operation
- All inputs and outputs TTL compatible
- Three state outputs
- Package
 - TC5316200BP : DIP42-P-600
 - TC5316200BF : SOP44-P-600

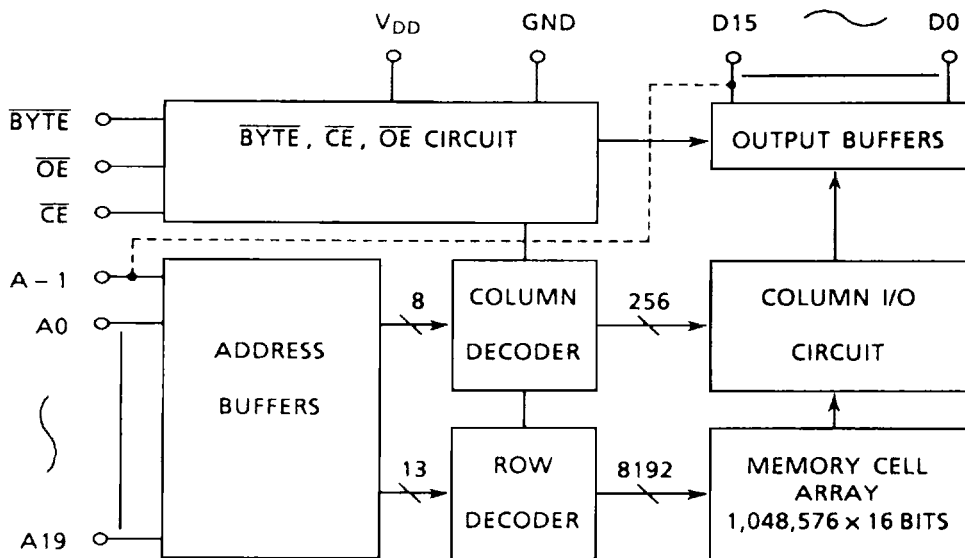
Pin Names

A0 ~ A19	Address Inputs
D0 ~ D14	Data Outputs
\overline{CE}	Chip Enable Input
\overline{OE}	Output Enable Input
D15/A - 1	Data Output/Address Input
BYTE	Word, Byte Selection Input
V _{DD}	Power Supply Voltage (+5V)
GND	Ground
NC	No Connection

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	CE	OE	BYTE	D0 ~ D7	D8 ~ D14	D15/A - 1	POWER
Read (16 Bits)	L	L	H	Data Out			Active
Read (Lower 8 Bits)	L	L	L	Data Out (Lower 8 Bits)	High Impedance	L	
Read (Upper 8 Bits)	L	L	L	Data Out (Upper 8 Bits)	High Impedance	H	
Output Deselect	L	H	*	High Impedance			Standby
Standby	H	*	*	High Impedance			

H = V_{IH} , L = V_{IL} , * = V_{IH} or V_{IL}

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.5 ~ 7.0	V
V_{IN}	Input Voltage	-0.5 ~ V_{DD}	
V_{OUT}	Output Voltage	0 ~ V_{DD}	
P_D	Power Dissipation	1.0/0.6*	W
T_{STRG}	Storage Temperature	-55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

* SOP

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.2	–	V _{DD} + 0.3	
V _{IL}	Input Low Voltage	-0.3	–	0.8	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
I _{LI}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}	–	±5.0	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0 ~ V _{DD}	–	±5.0	
I _{OH}	Output High Current	V _{OH} = 2.4V	-1.0	–	mA
I _{OL}	Output Low Current	V _{OL} = 0.4V	2.0	–	
I _{DDS1}	Standby Current	CE = V _{IH}	–	2	μA
I _{DDS2}		CE = V _{DD} - 0.2V	–	100	
I _{DDO1}	Operating Current	V _{IN} = V _{IH} /V _{IL} , t _{cycle} = 200ns, I _{OUT} = 0mA	–	60	mA
I _{DDO2}		V _{IN} = V _{DD} - 0.2V/0.2V, t _{cycle} = 200ns, I _{OUT} = 0mA	–	50	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t _{CYC}	Cycle Time	200	–	ns
t _{ACC}	Address Access Time	–	200	
t _{CE}	Chip Enable Access Time	–	200	
t _{BT}	BYTE Access Time	–	200	
t _{OE}	Output Enable Access Time	–	70	
t _{CED}	Output Disable Time from CE	–	60	
t _{OED}	Output Disable Time from OE	–	60	
t _{BSD}	Output Disable Time from BYTE	–	60	
t _{OH}	Output Hold Time	5	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.6V
Input Pulse Rise and Fall Times	5ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C _L = 100 pF

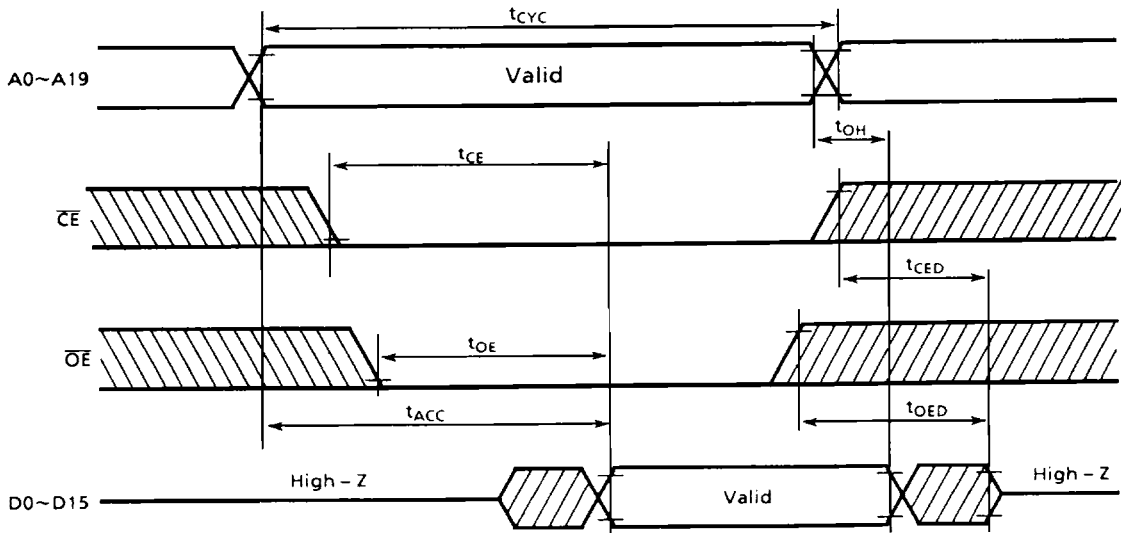
Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	–	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	–	12	

*This parameter is periodically sampled and is not 100% tested.

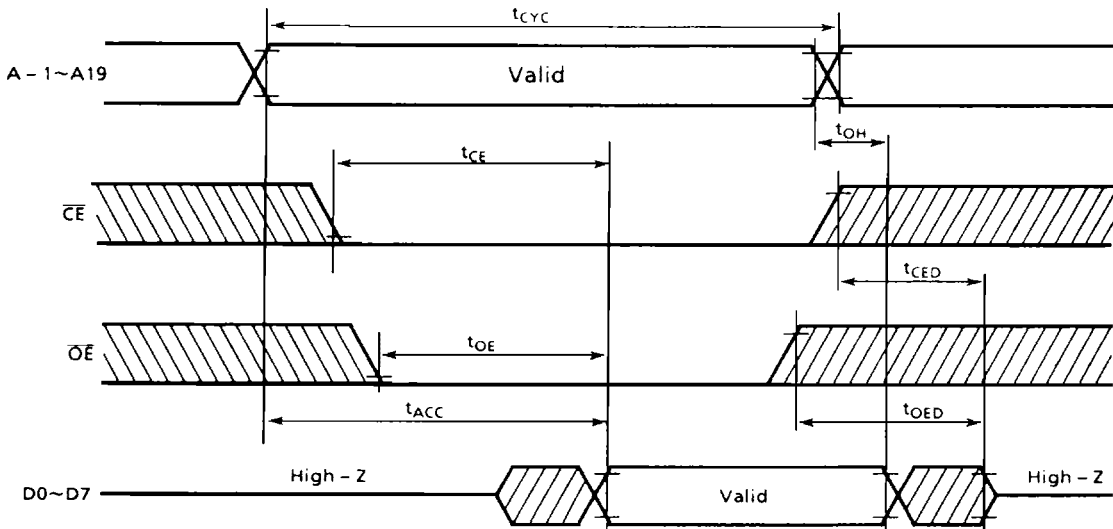
Timing Waveforms

Word-Wide (16 Bit) Read Mode



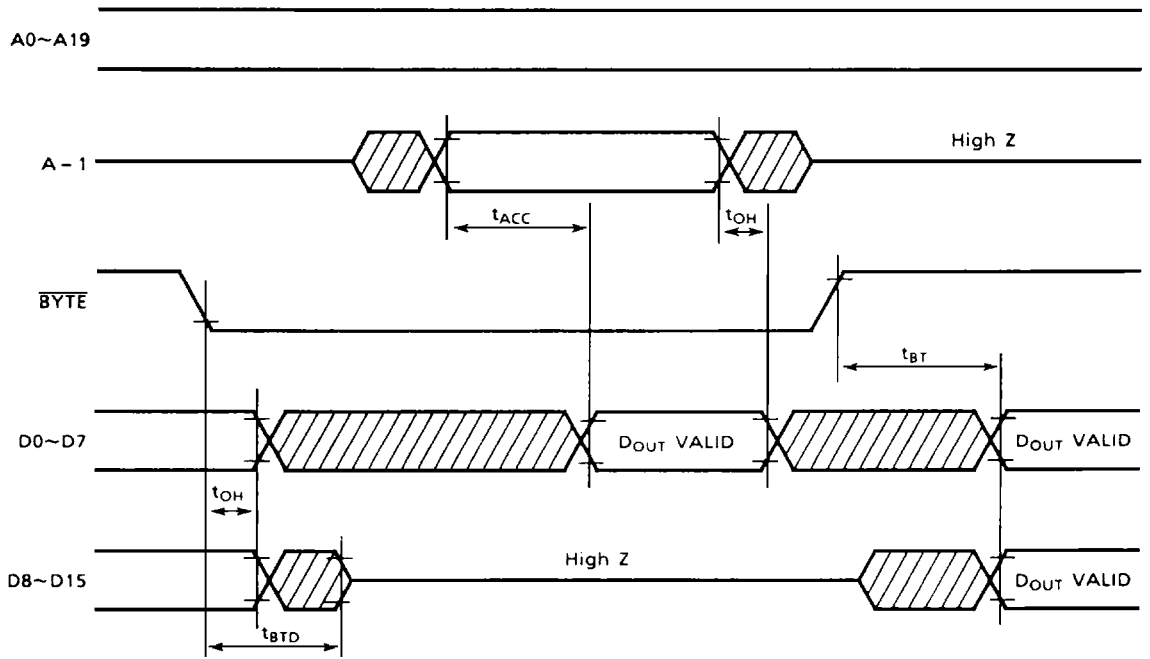
Note: $\overline{\text{BYTE}} = V_{IH}$

Byte-Wide (8 Bit) Read Mode



Note: $\overline{\text{BYTE}} = V_{IL}$

BYTE Transition



Note: $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$

