

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LVX4245FS

Dual Supply Octal Bus Transceiver

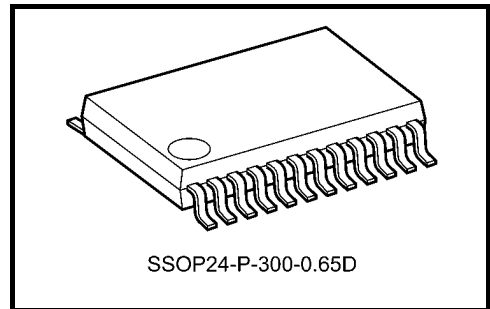
The TC74LVX4245FS is a dual supply, advanced high-speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology.

Designed for use as an interface between a 5V bus and a 3.3V bus in mixed 5V/3.3V supply systems' it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is intended for 2 way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\bar{G}$) can be used to disable the device so that the busses are effectively isolated. The A-port interfaces with the 5V bus, the B-port with the 3.3V bus.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight: 0.14 g (typ.)

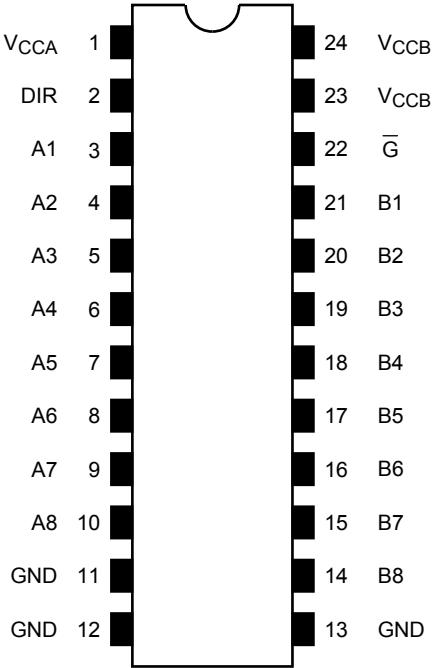
Features

- Bi-directional interface between 5 V and 3 V buses
- High-speed: $t_{pd} = 6.0 \text{ ns}$ (typ.)
($V_{CCA} = 5.0 \text{ V}$, $V_{CCB} = 3.3 \text{ V}$)
- Low power dissipation: $I_{CC} = 8 \mu\text{A}$ (max) ($T_a = 25^\circ\text{C}$)
- Symmetrical output impedance: $I_{OUTA} = \pm 24 \text{ mA}$ (min)
 $I_{OUTB} = \pm 12 \text{ mA}$ (min)
($V_{CCA} = 4.5 \text{ V}$, $V_{CCB} = 3.0 \text{ V}$)
- Low noise: $V_{OLP} = 1.5 \text{ V}$ (max)
- Package: SSOP (shrink small outline package)

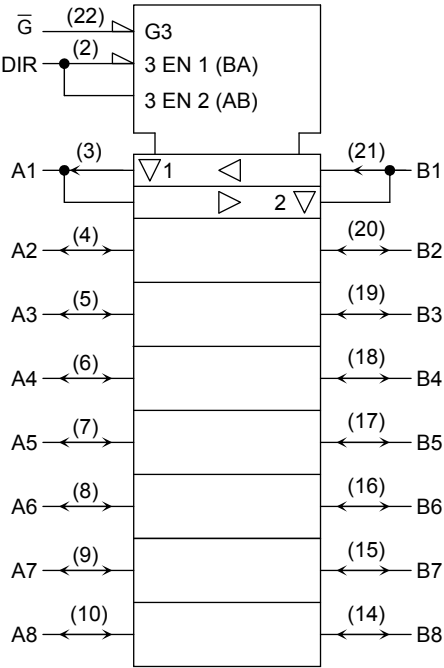
Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.

All floating (high impedance) bus pin must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment (top view)



IEC Logic Symbol



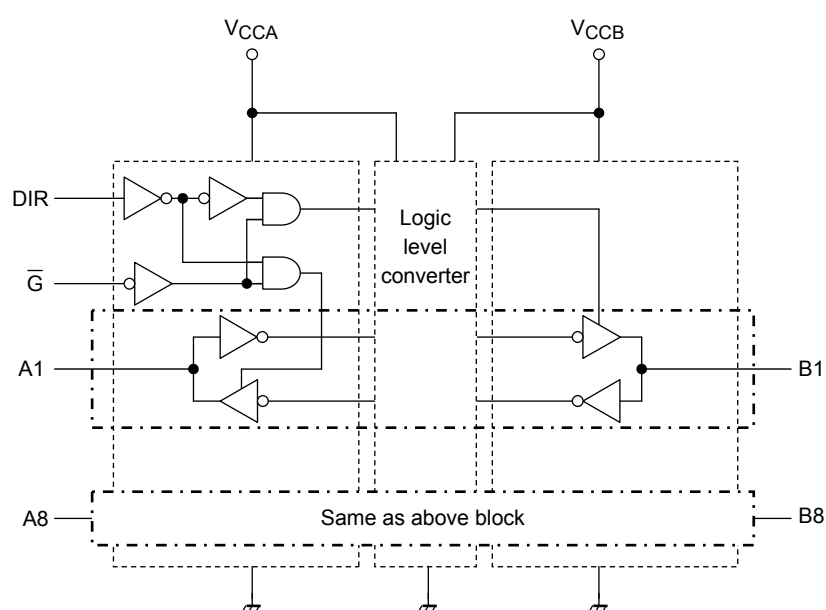
Truth Table

Inputs		Outputs	Function	
G-bar	DIR		A-Bus	B-Bus
L	L	A = B	Output	Input
L	H	B = A	Input	Output
H	X	Z	High impedance	

X: Don't care

Z: High impedance

Block Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range (Note 2)	V_{CCA}	-0.5 to 7.0	V
	V_{CCB}	-0.5 to $V_{CCA} + 0.5$	
DC input voltage	V_{IN}	-0.5 to $V_{CCA} + 0.5$	V
DC bus I/O voltage	$V_{I/OA}$	-0.5 to $V_{CCA} + 0.5$	V
	$V_{I/OB}$	-0.5 to $V_{CCB} + 0.5$	
Input diode current	I_{IK}	-20	mA
Output diode current	$I_{I/OK}$	±50	mA
DC output current	I_{OUTA}	±50	mA
	I_{OUTB}	±50	
DC V_{CC} /ground current	I_{CCA}	±200	mA
	I_{CCB}	±100	
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Don't supply a voltage to V_{CCB} terminal when V_{CCA} is in the off-state.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CCA}	4.5 to 5.5	V
	V _{CCB}	2.7 to 3.6	
Input voltage	V _{IN}	0 to V _{CCA}	V
Bus I/O voltage	V _{I/OA}	0 to V _{CCA}	V
	V _{I/OB}	0 to V _{CCB}	
Operating temperature	T _{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 8	ns/V
		(V _{CCA} = 4.5 to 5.5 V)	
		0 to 8	
		(V _{CCB} = 2.7 to 3.6 V)	

Note: The operating ranges are required to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either VCC or GND. Please connect both bus inputs and the bus outputs with VCC or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Electrical Characteristics

DC Characteristics (V_{CCB} = 2.7 to 3.6 V)

Characteristics		Symbol	Test Condition	V _{CCA} (V)	Ta = 25°C			Ta = −40 to 85°C		Unit
					Min	Typ.	Max	Min	Max	
Input voltage	H-level	V _{IHA}	DIR, $\overline{G}$, An	4.5 to 5.5	2.0	—	—	2.0	—	V
	L-level	V _{ILA}	DIR, $\overline{G}$, An	4.5 to 5.5	—	—	0.8	—	0.8	
Output voltage	H-level	V _{OHA}	V _{INA} = V _{IHA} or V _{ILA} I _{OH} = −100 μA	4.5	4.4	4.5	—	4.4	—	V
			V _{INB} = V _{IHB} or V _{ILB} I _{OH} = −24 mA	4.5	3.86	—	—	3.76	—	
	L-level	V _{OLA}	V _{INA} = V _{IHA} or V _{ILA} I _{OL} = 100 μA	4.5	—	0	0.1	—	0.1	
			V _{INB} = V _{IHB} or V _{ILB} I _{OL} = 24 mA	4.5	—	—	0.36	—	0.44	
3-state output Off-state current		I _{OZA}	V _{INA} = V _{IHA} or V _{ILA} V _{INB} = V _{IHB} or V _{ILB} V _{I/OA} = V _{CCA} or GND	5.5	—	—	±0.5	—	±5.0	μA
Input leakage current		I _{INA}	V _{IN} (DIR, $\overline{G}$) = V _{CCA} or GND	5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I _{CCA}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	5.5	—	—	8.0	—	80.0	μA
		I _{CCTA}	V _{INA} = 3.4 V (per input) V _{CCA} or GND (other input)	5.5	—	—	2.3	—	2.5	mA

DC Characteristics ($V_{CCA} = 5.0 \pm 0.5$ V)

Characteristics		Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
					V _{CCB} (V)	Min	Typ.	Max	Min		Max
Input voltage	H-level	V _{IHB}	Bn	2.7	2.0	—	—	2.0	—	V	
				3.6	2.2	—	—	2.2	—		
	L-level	V _{ILB}	Bn	2.7	—	—	0.8	—	0.8		
				3.6	—	—	0.8	—	0.8		
Output voltage	H-level	V _{OHB}	V _{INA} = V _{IHA} or V _{ILA}	I _{OH} = -100 μA	3.0	2.9	3.0	—	2.9	—	V
				I _{OH} = -8 mA	2.7	2.26	—	—	2.20	—	
				I _{OH} = -12 mA	3.0	2.48	—	—	2.40	—	
	L-level	V _{OLB}	V _{INA} = V _{IHA} or V _{ILA}	I _{OL} = 100 μA	3.0	—	0	0.1	—	0.1	
				I _{OL} = 8 mA	2.7	—	—	0.31	—	0.40	
				I _{OL} = 12 mA	3.0	—	—	0.31	—	0.40	
3-state output Off-state current		I _{OZB}	V _{INA} = V _{IHA} or V _{ILA} V _{I/OB} = V _{CCB} or GND	3.6	—	—	±0.5	—	±5.0	μA	
Quiescent supply current		I _{CCB}	V _{INA} = V _{CCA} or GND V _{INB} = V _{CCB} or GND	3.6	—	—	5.0	—	50.0	μA	
		I _{CCTB}	V _{INA} = 3.0 V (per input) V _{CCB} or GND (other input)	3.6	—	—	0.35	—	0.50	mA	

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, $V_{CCA} = 5.0 \pm 0.5 \text{ V}$)

Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = -40 to 85°C		Unit
			VCC (V)	Min	Typ.	Max	Min	Max	
Propagation delay time (An⇒Bn)	t _{pLH} t _{pHL}	Input: An Output: Bn (DIR = "H")	2.7	—	7.1	9.5	1.0	10.5	ns
			3.3 ± 0.3	—	6.5	8.6	1.0	9.5	
3-state output enable time ($\overline{G}$ ⇒ Bn)	t _{pZL} t _{pZH}		2.7	—	9.5	12.5	1.0	13.8	ns
			3.3 ± 0.3	—	8.6	11.4	1.0	12.5	
3-state output disable time ($\overline{G}$ ⇒ Bn)	t _{pLZ} t _{pHZ}		2.7	—	5.3	9.1	1.0	10.0	ns
			3.3 ± 0.3	—	5.3	9.1	1.0	10.0	
Propagation delay time (Bn⇒An)	t _{pLH} t _{pHL}	Input: Bn Output: An (DIR = "L")	2.7	—	7.0	9.5	1.0	10.5	ns
			3.3 ± 0.3	—	6.4	8.6	1.0	9.5	
3-state output enable time ($\overline{G}$ ⇒ An)	t _{pZL} t _{pZH}		2.7	—	8.5	11.6	1.0	12.7	ns
			3.3 ± 0.3	—	7.7	10.5	1.0	11.5	
3-state output disable time ($\overline{G}$ ⇒ An)	t _{pLZ} t _{pHZ}		2.7	—	5.1	6.8	1.0	7.5	ns
			3.3 ± 0.3	—	5.1	6.8	1.0	7.5	
Output to output skew	t _{osLH} t _{osHL}	(Note 1)	2.7 3.3 ± 0.3	— —	— —	1.5 1.5	— —	1.5 1.5	ns
Input capacitance	C _{INA}	DIR, $\overline{G}$	3.3 ± 0.3	—	5	10	—	10	
Bus input capacitance	C _{I/O}	An, Bn	3.3 ± 0.3	—	13	—	—	—	pF
Power dissipation capacitance (Note 2)	C _{PDA}	A⇒B (DIR = "H")	3.3 ± 0.3	—	17	—	—	—	pF
		B⇒A (DIR = "L")	3.3 ± 0.3	—	25	—	—	—	
	C _{PDB}	A⇒B (DIR = "H")	3.3 ± 0.3	—	4	—	—	—	
		B⇒A (DIR = "L")	3.3 ± 0.3	—	4	—	—	—	

Note 1: Parameter guaranteed by design.

($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

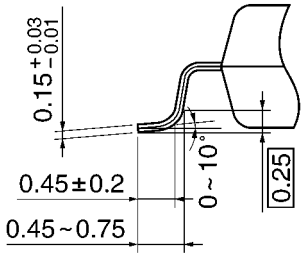
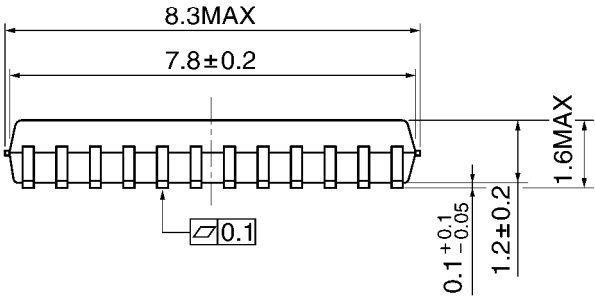
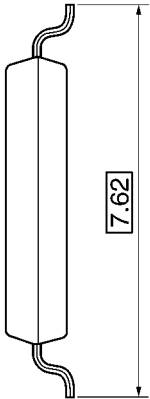
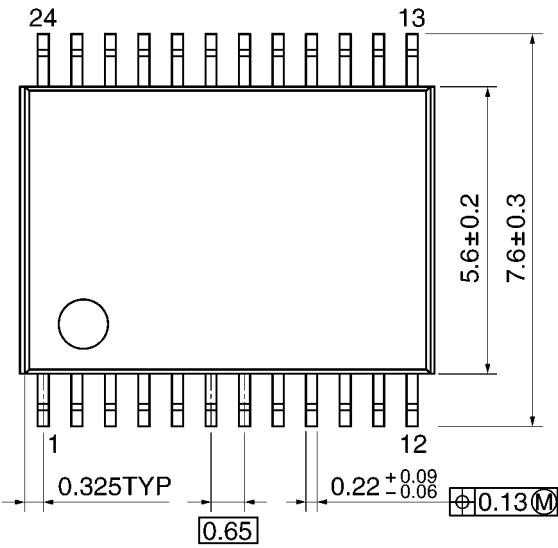
Noise Characteristics (Ta = 25°C, input: tr = tf = 3 ns, CL = 50 pF, RL = 500 Ω)

Characteristics		Symbol	Test Condition			Typ.	Limit	Unit
				V _{CCA} (V)	V _{CCB} (V)			
Quiet output maximum dynamic	V _{OL} (A)	V _{OLPA}	Input: Bn	5.0	3.3	1.0	1.5	V
Quiet output minimum dynamic	V _{OL} (A)	V _{OLVA}	Output: An (DIR = “L”)	5.0	3.3	−0.6	−1.2	V
Quiet output maximum dynamic	V _{OL} (B)	V _{OLPB}	Input: An	5.0	3.3	0.8	1.2	V
Quiet output minimum dynamic	V _{OL} (B)	V _{OLVB}	Output: Bn (DIR = “H”)	5.0	3.3	−0.5	−0.8	V
Minimum high level dynamic input voltage	V _{IH} (A)	V _{IHDA}	Input: An	5.0	3.3	—	2.0	V
Maximum low level dynamic input voltage	V _{IL} (A)	V _{ILDA}	Input: An	5.0	3.3	—	0.8	V
Minimum high level dynamic input voltage	V _{IH} (B)	V _{IHDB}	Input: Bn	5.0	3.3	—	2.0	V
Maximum low level dynamic input voltage	V _{IL} (B)	V _{ILDB}	Input: Bn	5.0	3.3	—	0.8	V

Package Dimensions

SSOP24-P-300-0.65D

Unit: mm



Weight: 0.14 g (typ.)

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