

swissbit®

Product Data Sheet

Industrial PCIe BGA SSD (M.2 1620 BGA)

E2000 Series

PCIe Gen3, 16x20mm BGA

Industrial Temperature Grade

Date: November 19, 2025
Revision: 1.11



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E2000 Series – Industrial PCIe Solid State Drive 60 GBytes up to 480 GBytes (PCI Express™ M.2 BGA)

1. Product Summary

- **Capacities:** 60 GBytes, 120 GBytes, 240 GBytes, 480 GBytes
- **Form Factor:** PCI Express® M.2 BGA (1620) (16mm x 20mm x 1.8mm)
- **Compliance:** PCI Express (PCIe) Specification Revision 3.1
- **Interface:** Gen3 x 4 Lanes
- **Command Sets:** Supports NVMe 1.3
- **Performance:**
 - Read Performance: Sequential Read up to 1,753 MBytes/s, Random Read 4K up to 140,000 IOPS
 - Write Performance: Sequential Write up to 864 MBytes/s, Random Write 4K up to 134,000 IOPS
- **Operating Temperature Range²:**
 - Industrial: -40 °C to 85 °C (T_{ambient})
 - Industrial: -40 °C up to 95 °C (T_{case})³
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 3.3, 1.8 and 0.9V supply voltages
- **Low Power Consumption**
- **Power:**
 - Power States PS0, PS1, PS2, PS3 and PS4
 - Thermal Throttling supported
- **Data Retention⁴:** 10 Years @ Life Begin; 1 Year @ Life End
- **High-Performance Processor with Integrated, Parallel Flash Interface Engines:**
 - 3D NAND Flash
 - LDPC Code ECC (up to 120bit corrections per 1KByte page)
 - End-to-end data path protection
 - Increased Overprovisioning for improved performance and endurance
 - Page RAID feature
- **High Reliability**

¹ To check the compatibility of the customer system and the storage device is part of the customer's responsibility. Swissbit can provide guidance and support on request.

² Adequate airflow is required to ensure the drive temperature, as reported in the S.M.A.R.T. data, does not exceed CCTEMP (Critical Composite Temperature Threshold) reported in the "Identify Controller Data Structure"

³ T_{case} is the case surface temperature at the center of the top side of the device.

⁴ NAND Flash suppliers refer to JEDEC JESD47 and JESD22 for Data Retention testing. Based on the information provided by the NAND Flash suppliers, Data Retention is targeted as shown in the table for reference.

2. Product Features

- Dynamic and Static Wear Leveling
- Subpage Mode Flash Translation Layer (FTL)
- Data Care Management
 - Active: Adaptive Read Refresh
 - Passive: Background Media Scan
- Lifetime Enhancements
 - Dynamic Bad Block Remapping
 - Write Amplification Reduction
- Power Fail Data Loss Protection
- In-Field Firmware Update
- Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)⁵
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM
- AES256 Encryption (on request)
- TCG Opal 2.0 (on request)
- Life Cycle Management
- Controlled "Locked" BOM
- RoHS / REACH Compliant



⁵ Refer to the JEDEC JESD218A and JESD291A standard for SSD device life and endurance measurement techniques.

3. Ordering Information

Table 1: Standard Product List

Capacity	Part Number
60 GBytes	SE2000BC060Gt-xTB1-yCB-STD
120 GBytes	SE2000BC120Gt-xTB2-yCB-STD
240 GBytes	SE2000BC240Gt-xTB4-yCB-STD
480 GBytes	SE2000BC480Gt-xTB8-yCB-STD

t = temperature; x = product generation; y= firmware revision

Table 2: Available Part Numbers

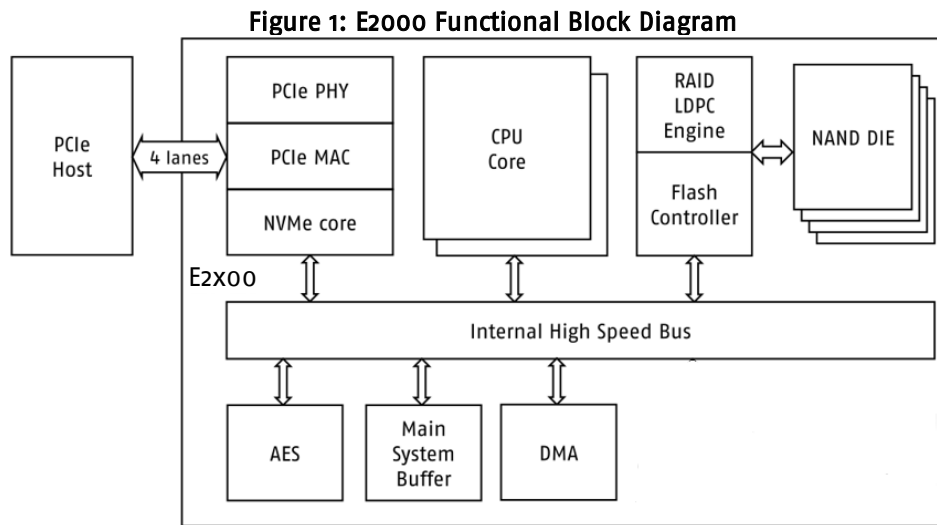
Capacity	FW ECR50001
60 GBytes	SE2000BC060GI-1TB1-1CB-STD
120 GBytes	SE2000BC120GI-1TB2-1CB-STD
240 GBytes	SE2000BC240GI-1TB4-1CB-STD
480 GBytes	SE2000BC480GI-1TB8-1CB-STD

Table 3: Available Part Numbers

Capacity	FW ECR50002
60 GBytes	SE2000BC060GI-1TB1-2CB-STD
120 GBytes	SE2000BC120GI-1TB2-2CB-STD
240 GBytes	SE2000BC240GI-1TB4-2CB-STD
480 GBytes	SE2000BC480GI-1TB8-2CB-STD

4. Product Description

The Swissbit® E2000 Solid State Drive (SSD) leverages the M.2 BGA standard and NVMe standard to support a PCIe electrical interface. The NVMe controller and the newest 3D NAND flash technology provide a robust, non-volatile storage solution for today's embedded computing applications. A functional block diagram of the E2000 SSD is provided below in Figure 1.



The E2000 SSD combines a high performance NVMe controller and several 3D NAND flash devices into a 16 x 20mm BGA package.

The on-board NVMe controller manages the interface between the host and the non-volatile NAND flash memory array. The controller is designed to support PCIe interface speeds and utilizes a dual processing core, providing an optimum balance between read/write performance, Data Care Management, and power fail protection.

Swissbit E2000 SSDs deliver a high IOPS rate and high endurance by combining latest 3D NAND flash technology with a high-end controller architecture, firmware, and an optimized configuration. The SSDs are designed for applications requiring high data transfer rates (See section 4-1, Table 3). This performance is achieved through a 4-channel flash controller, and 4-lane PCIe interface.

An integrated Low-Density Parity Check (LDPC) Error Correction Code (ECC) engine provides the E2000 hardware ECC, which is capable of correcting up to 120 bits per 1 KByte page. This engine, combined with Swissbit Data Care Management firmware, provides both passive and active data management to ensure data integrity and delivers the maximum possible endurance and reliability from the NAND flash array. These routines include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh, and Dynamic Block Remapping.

The risk of data loss because of an unexpected power fail event is mitigated using a special firmware architecture, which prevents the possibility of resident data being corrupted.

4.1 Performance Specifications

The E2000 read/write sequential and random I/O performance benchmarks are detailed below in Table 4.

Table 4: Read/Write Performance

Capacity	Sequential Read (MBPS)		Sequential Write (MBPS)		Random Read 4K (IOPS)		Random Write 4K (IOPS)	
	HMB on	HMB off	HMB on	HMB off	HMB on	HMB off	HMB on	HMB off
60 GBytes	306	296	149	99	21,000	12,000	28,000	20,000
120 GBytes	644	632	396	265	50,000	24,000	70,000	47,000
240 GBytes	1,280	1,234	687	476	97,000	51,000	110,000	93,000
480 GBytes	1,753	1,636	864	770	140,000	84,000	134,000	129,000

4.2 Power Consumption

The drive-level power consumption as a function of operating mode is shown below in Table 5.

Table 5: Power Consumption Typical⁶

Capacity	Sequential Read	Sequential Write	Idle	PS ₃ ⁷	PS ₄ ⁷	Unit
60 GBytes	1,260	1,200	260	12	1.6	mW
120 GBytes	1,530	1,310				
240 GBytes	2,080	1,580				
480 GBytes	2,270	1,860				

Table 6: Current Consumption Max

Capacity	3.3V (PWR 1)	1.8V (PWR 2)	0.9V (PWR 3)	Unit
60 GBytes	200	400	1,500	mA
120 GBytes	300	400		
240 GBytes	400	500		
480 GBytes	700	600		

⁶ All values were recorded at 25 °C

⁷ Measured with enabled ASPM L1.2

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

The recommended operating conditions for the E2000 BGA SSD are provided in Table 7 below.

Table 7: Recommended Operating Conditions⁸

Parameter	Value
Industrial Operating Temperature	-40 °C to 85 °C (T _{ambient})
Industrial Operating Temperature	-40 °C up to 95 °C (T _{case}) ⁹
Power Supply Voltages	3.3V ±5% 1.8V ±5% 0.9V ±5%

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed below in Table 8.

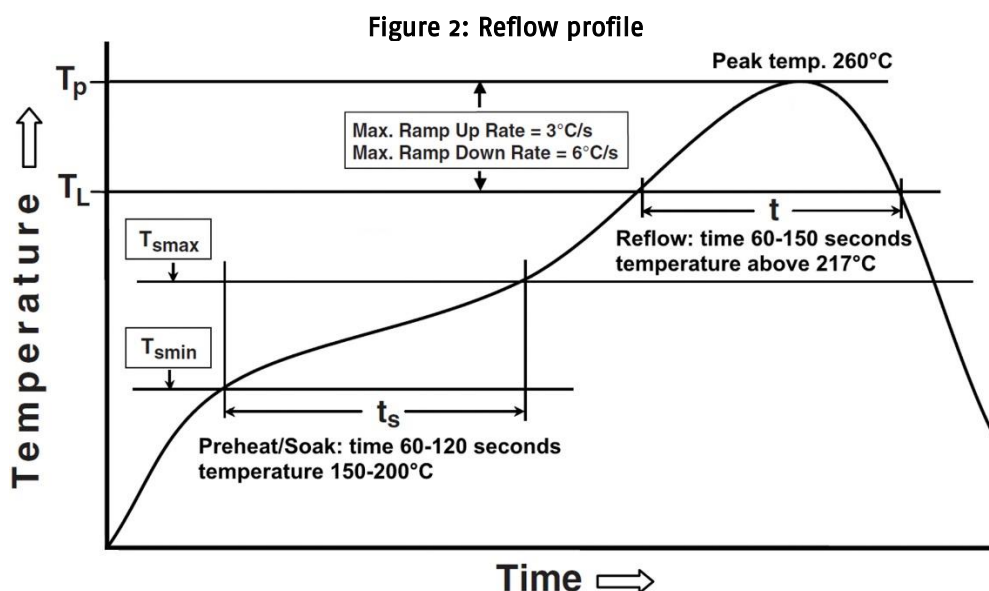
Table 8: Recommended Storage Conditions¹⁰

Parameter	Value
Industrial Storage Temperature	-40 °C to 85 °C

4.3.3 Reflow profile and MSL

Table 9: Reflow and MSL conditions

Parameter	Condition
MSL	Level 3 (storage condition 168 hours, ≤30 °C/ 60% RH)
Reflow	According to IPC/JEDEC J-STD-020D.1: Peak temp 260 °C, 217 °C endurance 60~150 seconds



⁸ Adequate airflow is required to ensure the drive temperature, as reported in the S.M.A.R.T. data, does not exceed CCTEMP (Critical Composite Temperature Threshold) reported in the "Identify Controller Data Structure"

⁹ T_{case} is the case surface temperature at the center of the top side of the device.

¹⁰ The retention at high temperature is reduced. The acceleration factor at 100 °C compared with 40 °C is very high, i.e. the initial retention from 10 years@40 °C is reduced to 33 days@100 °C based on NAND process node.

4.4 Regulatory Compliance

The E2000 devices comply with the following standards¹¹:

- PCI-SIG PCI Express Base Specification Revision 3.1a, December 7, 2015
- PCI-SIG PCI Express M.2 Specification Revision 1.1, December 15, 2016
- NVMe Express Revision 1.3, May 1, 2017
- RoHS, REACH, Halogen Free
- UL94 V-0

4.5 Mechanical Specifications

The E2000 BGA physical dimensions are detailed in Table 10 below.

NOTE: See also the Package Mechanical on page 14.

Figure 4 on page 14 illustrates the E2000 dimensions.

Table 10: Physical Dimensions

Physical Dimensions		Unit
Length	16.00±0.10	mm
Width	20.00±0.10	
Thickness	Max. 1.8	
Weight (Max Capacity)	< 1.0	g

4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed below. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 11: Reliability

Parameter	Value
MTBF (at 25 °C)	> 2,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per 10 ¹⁶ Bits Read
Data Retention (up to 40 °C) ¹²	10 Years at Start (JEDEC JESD47), 1 Year at EOL

¹¹ To check the compatibility of the customer system and the storage device is part of the customer's responsibility. Swissbit can provide guidance and support on request.

¹² NAND Flash suppliers refer to JEDEC JESD47 and JESD22 for Data Retention testing. Based on the information provided by the NAND Flash suppliers, Data Retention is targeted as shown in the table for reference.

Endurance represented as both TeraBytes Written (TBW) and Drive Writes Per Day (DWPD) for two different application scenarios is provided in the following table.

Table 12: Endurance^{13, 14, 15}

Capacity	Sequential		Client		Enterprise	
	TBW	DWPD	TBW	DWPD	TBW	DWPD
60 GBytes	180	2.68	141	2.14	22	0.33
120 GBytes	360	2.74	268	2.03	48	0.36
240 GBytes	720	2.74	471	1.79	91	0.34
480 GBytes	1,440	2.74	964	1.83	151	0.28

4.7 Drive Geometry Specification

The E2000 drive geometry is set to report industry-standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown below in Table 13.

Table 13: Drive Geometry

Raw Drive Capacity	User Capacity ¹⁶	Total LBA	User Addressable Bytes
		Decimal	(Unformatted)
64 GBytes	60 GBytes	117,231,408	60,022,480,896
128 GBytes	120 GBytes	234,441,648	120,034,123,776
256 GBytes	240 GBytes	468,862,128	240,057,409,536
512 GBytes	480 GBytes	937,703,088	480,103,981,056

¹³ Client and Enterprise workloads follow the JEDEC JESD219 standard; Enterprise workload values are measured based on 168 hours of runtime. Values measured with HMB enabled only. 1 TByte = 10¹² bytes

¹⁴ According to JEDEC (JESD471), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume or frequent writing below 0 °C reduces the specified TBW. The values listed are estimates and are subject to change without notice

¹⁵ DWPD values are based on a service life of 3 years. DWPD values with consideration of the limited lifetime warranty period of the storage device according to the used flash type and device capacity. Customer workload with higher DWPD values contributes to an earlier EOL of the storage device.

¹⁶ 1 GByte = 10⁹ bytes

5. Electrical Interface

Please see [design-in guideline](#) for more detailed information.

Figure 3: E2000 BGA Ballmap (top view, balls down)

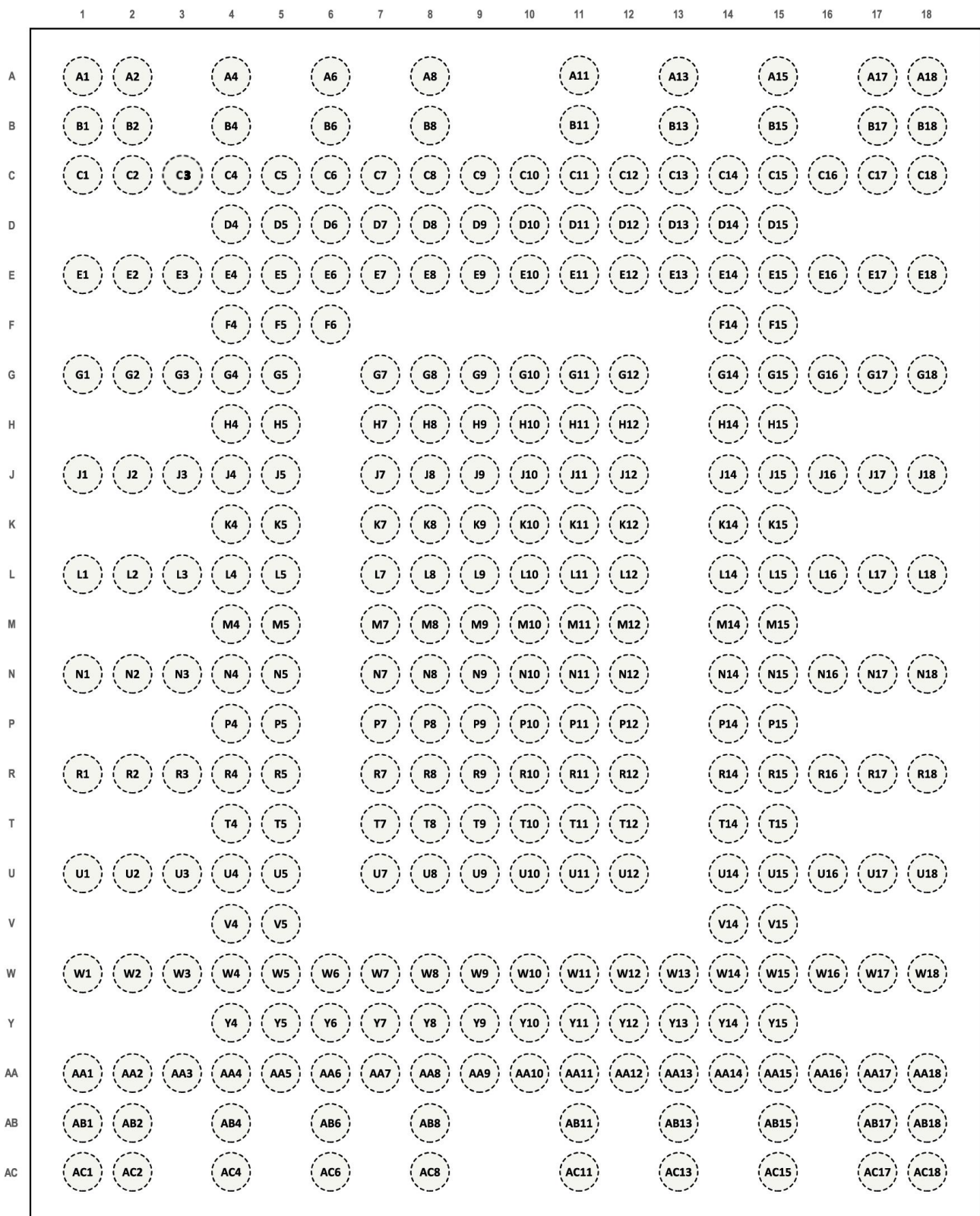


Table 14: Ball Assignment, Name and Description

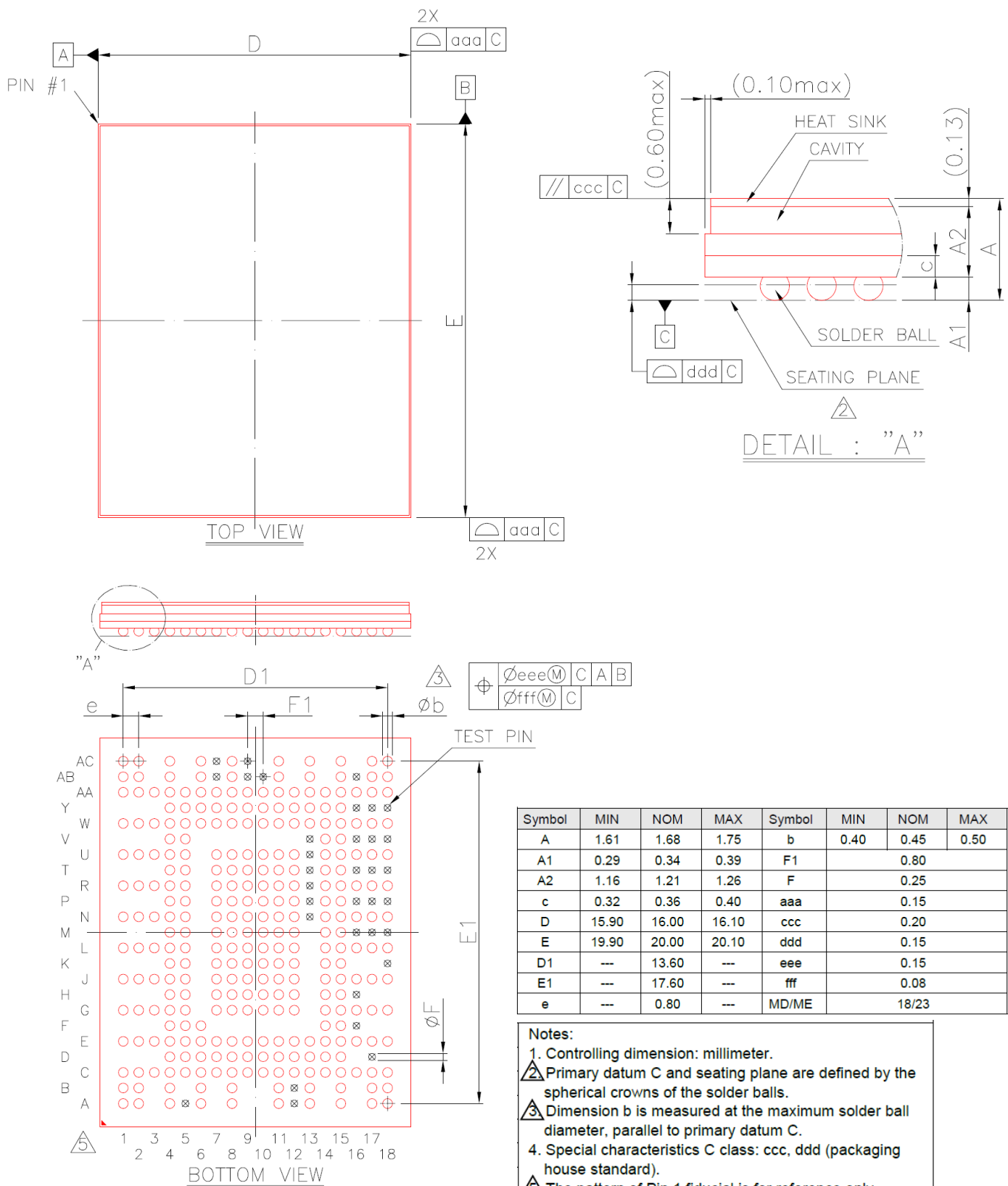
Signal Group	Signal	BGA Ball	I/O	Description	Voltage
PCIe	PERp0	F4	I	PCIe RX Differential signals	
	PERn0	F5	I		
	PERp1	K4	I		
	PERn1	K5	I		
	PERp2	P4	I		
	PERn2	P5	I		
	PERp3	V4	I		
	PERn3	V5	I		
	PETp0	H4	O	PCIe TX Differential signals	
	PETn0	H5	O		
	PETp1	M4	O		
	PETn1	M5	O		
	PETp2	T4	O		
	PETn2	T5	O		
	PETp3	Y4	O		
	PETn3	Y5	O		
	REFCLKp	D4	I	PCIe Reference Clock signal (100 MHz), positive input	
	REFCLKn	D5	I	PCIe Reference Clock signal (100 MHz), negative input	
	PERST#	D7	I	PCIe-Reset is a functional reset	1.8V
	CLKREQ#	D8	I/O	Clock Request is a reference clock request signal. Open Drain with pull up on Platform.	1.8V
Power/ Ground	PWR_1	D10, E9, W9, W10, Y9, Y10	I	Flash supply (6 pins) can be switched off by controller pin A6 (EX_PWD#) +3.3V supply	3.3V
	PWR_1.1	D9, E10	I	+3.3V supply	3.3V
	PWR_2	R8, R11, R12, T7, T8, T11, T12, U7, U8, U11, U12	I	+1.8V supply (11 pins)	1.8V
	PWR_2.1	R7	I	+1.8V supply	1.8V
	PWR_3	G7, G8, G11, G12, H7, H8, H11, H12, J7, J8, J11, J12	I	+core supply (12 pins) can be reduced to 0.75V by controller pin A6 (EX_PWD#) +0.9V supply (12 pins)	0.9V
	GND	C1-C5, C15, D6, D11, E1-E7, E11, E14, E15, F6, G1-G5, G9, G10, G14, G15, H9, H10, J1-J5, J9, J10, J14, J15, K7-K12, L1-L5, L14, L15, M9, M10, N1-N5, N14, N15, P7-P12, R1-R5, R9, R10, R14, R15, T9, T10, U1-U5, U9, U10, U14, U15, W1-W6, W11, W14, W15, Y6, Y11, Y13, AA1-AA5, AA14, AA15	-	Return current path (106 pins)	GND

Signal Group	Signal	BGA Ball	I/O	Description	Voltage
Function Signals	DASP#	W7	I/O	Device activity Can be used as LED indicator (device busy). Keep floating if not used.	
	XIN	C8	I	25MHz crystal input	
	XOUT	C7	O	25MHz crystal output	
	QE	C11	I/O	Quick Erase	
	EX_PWD#	A6	O	Power switch control (for PS4) 0: When device enters PS4, controller core power stays at low power state 1: Normal power supply	3.3V
Test Debug Signals	DEBUG	L18, N18, R17, R18, N17, D13, E13, AC18	-	Swissbit debug only. Recommended to connect to test pin or pad. Keep floating.	
Misc.	DNU	A1, A2, A4, A8, A11, A13, A15, A17, A18, AA16, AA17, AA18, AA6-AA13, AB1, AB2, AB4, AB6, AB8, AB11, AB13, AB15, AB17, AB18, AC1, AC2, AC4, AC6, AC8, AC11, AC13, AC15, AC17, B1, B2, B4, B6, B8, B11, B13, B15, B17, B18, C6, C9, C10, C12, C13, C14, C16, C17, C18, D12, D14, D15, E12, E16, E17, E18, E8, F14, F15, G16, G17, G18, H14, H15, J16, J17, J18, K14, K15, L16, L17, L7-L12, M11, M12, M14, M15, M7, M8, N16, N7-N12, P14, P15, R16, T14, T15, U16, U17, U18, V14, V15, W12, W13, W16, W17, W18, W8, Y7, Y8, Y12, Y14, Y15	-	Do not use Keep signal floating.	

6. Package Mechanical

NOTE: See also the *Mechanical Specifications* section on page 9.

Figure 4: E2000 mechanical drawing



7. NVMe Commands

This section provides information on the NVMe commands supported by the device. The commands are issued by loading the DWords in the command block with the supplied parameter, and then writing the command code to the register. See Table 15 for a list of NVMe commands the device supports. For details about setting up the command registers, see the latest NVMe Specification.

Table 15: NVMe Command Sets

Command	Code	Command	Code
Admin Commands			
Delete I/O Submission Queue	00h	Create I/O Submission Queue	01h
Get Log Page	02h	Delete I/O Completion Queue	04h
Create I/O Completion Queue	05h	Identify	06h
Abort	08h	Set Features	09h
Get Features	0Ah	Asynchronous Event Request	0Ch
Firmware Commit	10h	Firmware Image Download	11h
Device Self-test	14h	Format NVM	80h
Sanitize	84h		
NVM Command Set			
Flush	00h	Write	01h
Read	02h	Write Uncorrectable	04h
Compare	05h	Write Zeroes	08h
Dataset Management	09h		

8. Identify Command

The following tables describe the data the drive returns for the Identify command (06h).

Table 16: Identify Namespace Data Structure (CNS 00h)

Byte(s)	Default Value	Data Field Type Information
0-7	XXXXh ¹⁷	Namespace Size (NSZE)
8-15	XXXXh ¹⁷	Namespace Capacity (NCAP)
16-23	XXXXh ¹⁷	Namespace Utilization (NUSE)
24	00h	Namespace Features (NSFEAT)
25	00h	Number of LBA Formats (NLBAF)
26	00h	Formatted LBA Size (FLBAS)
27	00h	Metadata Capabilities (MC)
28	00h	End-to -end Data Protection Capabilities (DPC)
29	00h	End-to -end Data Protection Type Settings (DPS)
30	00h	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	00h	Reservation Capabilities (RESCAP)
32	00h	Format Progress Indicator (FPI)
33	01h	Deallocate Logical Block Features (DLFEAT)
34-35	0000h	Namespace Atomic Write Unit Normal (NAWUN)

¹⁷ Values depend on device configuration.

Byte(s)	Default Value	Data Field Type Information
36-37	0000h	Namespace Atomic Write Unit Power Fail (NAWUPF)
38-39	0000h	Namespace Atomic Compare & Write Unit (NACWU)
40-41	0000h	Namespace Atomic Boundary Size Normal (NABSN)
42-43	0000h	Namespace Atomic Boundary Offset (NABO)
44-45	0000h	Namespace Atomic Boundary Size Power Fail (NABSPF)
46-47	0000h	Namespace Optimal IO Boundary (NOIOB)
48-63	All 00h	NVM Capacity (NVMCAP)
64-103	All 00h	Reserved
104-119	All 00h	Namespace Globally Unique Identifier (NGUID)
120-127	All 00h	IEEE Extended Unique Identifier (EUI64)
128-131	00090000h	LBA Format 0 Support (LBAFo)
132-191	All 00h	LBA Format 1 to 15 Support (LBAF1 – LBAF15)
192-383	All 00h	Reserved
384-4095	All 00h	Vendor Specific (VS)

Table 17: Identify Controller Data Structure (CNS 01h)

Byte(s)	Default Value	Data Field Type Information
0-1	1DD4h	PCI Vendor ID (VID)
2-3	1DD4h	PCI Subsystem Vendor ID (SSVID)
4-23	XXXXh ¹⁷	Serial Number (SN)
24-63	XXXXh ¹⁷	Model Number (MN)
64-71	XXXXh ¹⁷	Firmware Version (FR)
72	06h	Recommended Arbitration Burst (RAB)
73-75	8C6078h	IEEE OUI Identifier (IEEE)
76	00h	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	06h	Maximum Data Transfer Size (MDTS)
78-79	0001h	Controller ID (CNTLID)
80-83	00010300h	Version (VER)
84-87	000249F0h	Runtime D3 Resume Latency (RTD3R)
88-91	XXXXXXXXh ¹⁷	Runtime D3 Entry Latency (RTD3E)
92-95	00000200h	Optional Asynchronous Events Supported (OAES)
96-99	00000000h	Controller Attributes (CTRATT)
100-111	All 00h	Reserved
112-127	All 00h	FRU Globally Unique Identifier (FGUID)
128-255	All 00h	Reserved
256-257	0016h	Optional Admin Command Support (OACS)
258	04h	Abort Command Limit (ACL)
259	07h	Asynchronous Event Request Limit (AERL)
260	12h	Firmware Updates (FRMW)
261	0Eh	Log Page Attributes (LPA)
262	3Fh	Error Log Page Entries (ELPE)

Byte(s)	Default Value	Data Field Type Information
263	04h	Number of Power States Supported (NPSS)
264	01h	Admin Vendor-Specific Command Configuration (AVSCC)
265	00h	Autonomous Power State Transition Attributes (APSTA)
266-267	0170h	Warning Composite Temperature Threshold in Degrees Kelvin (WCTEMP)
268-269	017Fh	Critical Composite Temperature Threshold in Degrees Kelvin (CCTEMP)
270-271	0064h	Maximum Time for Firmware Activation (MTFA)
272-275	00004000h	Host Memory Buffer Preferred Size (HMPRE)
276-279	00004000h	Host Memory Buffer Minimum Size (HMMIN)
280-295	XXXXh ¹⁷	Total NVM Capacity (TNVMCAP)
296-311	All 00h	Unallocated NVM Capacity (UNVMCAP)
312-315	00000000h	Replay Protected Memory Block Support (RPMBS)
316-317	000Ah	Extended Device Self-test Time (EDSTT)
318	01h	Device Self-test Options (DSTO)
319	04h	Firmware Update Granularity (FWUG)
320-321	0000h	Keep Alive Support (KAS)
322-323	0001h	Host Controlled Thermal Management Attributes (HCTMA)
324-325	0157h	Minimum Thermal Management Temperature (MNTMT)
326-327	017Fh	Maximum Thermal Management Temperature (MXTMT)
328-331	00000002h	Sanitize Capabilities (SANICAP)
332-511	All 00h	Reserved
512	66h	Submission Queue Entry Size (SQES)
513	44h	Completion Queue Entry Size (CQES)
514-515	0000h	Maximum Outstanding Commands (MAXCMD)
516-519	000000001h	Number of Namespaces (NN)
520-521	001Fh	Optional NVM Command Support (ONCS)
522-523	0000h	Fused Operation Support (FUSES)
524	03h	Format NVM Attributes (FNA)
525	01h	Volatile Write Cache (VWC)
526-527	0000h	Atomic Write Unit Normal (AWUN)
528-529	0000h	Atomic Write Unit Power Fail (AWUPF)
530	00h	NVM Vendor-Specific Command Configuration (NVSCC)
531	00h	Reserved
532-533	0000h	Atomic Compare and Write Unit (ACWU)
534-535	0000h	Reserved
536-539	00000000h	Scatter Gather List Support (SGLC)
540-767	All 00h	Reserved
768-1023	All 00h	NVM Subsystem NVMe Qualified Name (SUBNQN)
1024-2047	All 00h	Reserved

2048-2079	XXXXh	Power State 0 Descriptor
2080-2111	XXXXh	Power State 1 Descriptor
2112-2143	XXXXh	Power State 2 Descriptor
2144-2175	XXXXh	Power State 3 Descriptor
2176-2207	XXXXh	Power State 4 Descriptor
2208-3071	All ooh	Power State 5 – 31 Descriptor (Not Applicable)
3072-4095	All ooh	Vendor Specific (VS)

9. Log Pages / Health Monitoring Functionality

The E2000 BGA SSDs support Self-Monitoring, Analysis, and Reporting Technology (SMART) attributes. The SSD supports log information as defined in the NVMe specification. Supported information is shown in the log pages defined in Table 18: Supported Log Pages:

Table 18: Supported Log Pages

Log Page	Log Identifier
Error Information	01h
SMART/Health Information	02h
Firmware Slot Information	03h
Commands Supported and Effects	05h
Device Self-Test Log	06h
Telemetry Host-Initiated	07h
Telemetry Controller-Initiated	08h

See the following table for the 512-byte data structure of the SMART/Health Information log page:

Table 19: SMART/Health Information (Log Identifier 02h)

Byte(s)	Description
0	Critical warning: for the state of the controller
1-2	Composite Temperature: in degrees Kelvin
3	Available Spare: as a percentage of remaining spare capacity
4	Available Spare Threshold
5	Percentage Used: Estimate of the percentage of the NVM subsystem life left based on usage
6-31	Reserved
32-47	Data Units Read: Number of 512-byte sectors read by the host (in 1000 increments)
48-63	Data Units Written: Number of 512-byte sectors written by the host (in 1000 increments)
64-79	Host Read Commands: Number of Read commands completed by the controller
80-95	Host Write Commands: Number of Write commands completed by the controller
96-111	Controller Busy Time: Amount of time, in minutes, the controller was busy with I/O commands
112-127	Power Cycles: Number of power cycles that has occurred over the life of the drive
128-143	Power On Hours: Number of hours the device has been powered over the life of the drive (does not include the time the device is in low power state conditions)
144-159	Unsafe Shutdowns: Number of shutdowns that occurred without a shutdown notification
160-175	Media and Data Integrity Errors: Number of unrecoverable errors, including UECC, CRC checksum failures, and LBA mismatches, that occurred over the life of the drive
176-191	Number of Error Information Log Entries: Number of entries recorded in the Error Information log over the life of the drive
192-195	Warning Composite Temperature Time: Amount of time, in minutes, the controller was operational and the Composite Temperature was equal to or greater than the Warning Composite Temperature Threshold (WCTEMP) but less than the Critical Composite Temperature Threshold (CCTEMP)
196-199	Critical Composite Temperature Time: Amount of time, in minutes, the controller was operational and the Composite Temperature was equal to or greater than the Critical Composite Temperature Threshold (CCTEMP)
200-201	Temperature Sensor 1: Current temperature, in degrees Kelvin, reported by temperature sensor 1
202-203	Temperature Sensor 2: Current temperature, in degrees Kelvin, reported by temperature sensor 2
204-215	Not used
216-219	Thermal Management Temperature 1 Transition Count: number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance
220-223	Thermal Management Temperature 2 Transition Count: number of times the controller transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance
224-227	Total Time For Thermal Management Temperature 1: number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions while minimizing the impact on performance
228-231	Total Time For Thermal Management Temperature 2: number of seconds that the controller had transitioned to lower power active power states or performed vendor specific thermal management actions regardless of the impact on performance
232-511	Reserved

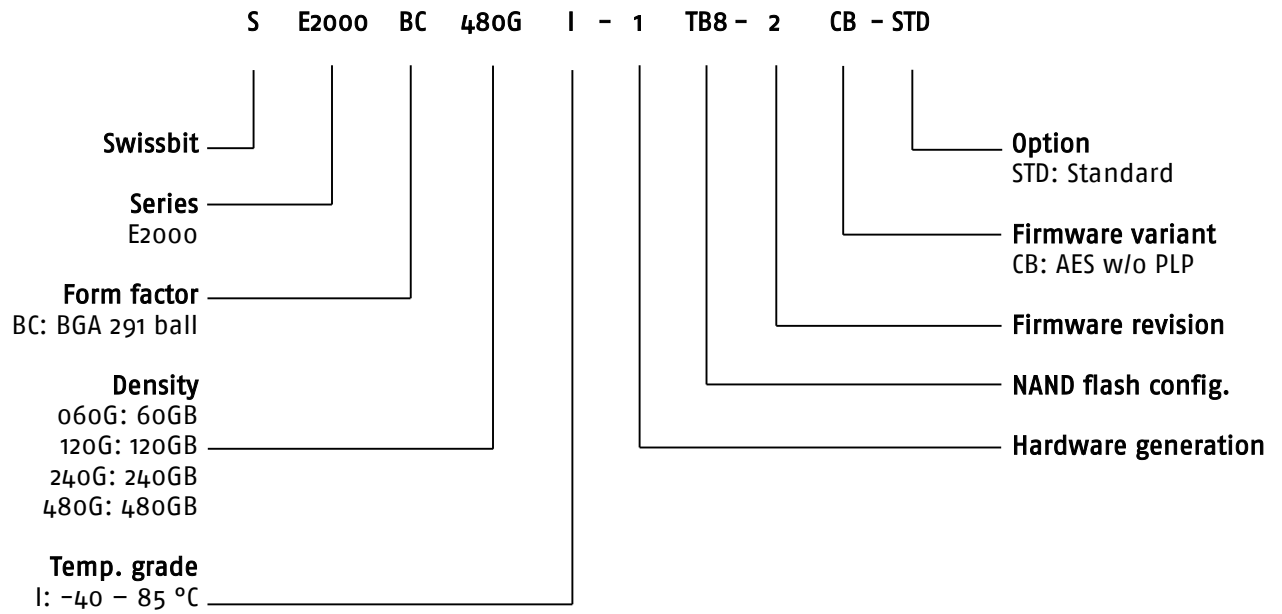
The following data structure is applied to both Telemetry Host-Initiated log and Telemetry Controller-Initiated log:

Table 20: Telemetry Log (Log Identifier 07h)

Byte(s)	Description
Telemetry Header	
0	Log Identifier: This field shall be 07h
1-4	Reserved
5-7	IEEE OUI Identifier (IEEE)
4	Telemetry Host-Initiated Data Area 1 Last Block: This field shall be 0001h
10-381	Reserved
382	Telemetry Controller-Initiated Data Available
383	Telemetry Controller-Initiated Data Generation Number
384-511	Reserved
Telemetry Data Block 1	
528-529	Minimum Temperature, in degrees Kelvin
530-531	Current Temperature, in degrees Kelvin
530-531	Maximum Temperature, in degrees Kelvin
560-561	Number of valid spare blocks
562-563	Number of initial spare blocks
564-565	Run Time Bad Block Count
596-599	SLC Maximum Erase Count
604-607	SLC Average Erase Count
612-615	TLC Maximum Erase Count
620-623	TLC Average Erase Count
640	SLC Remaining Life Percentage Based On P/E in %
646	TLC Remaining Life Percentage Based On P/E in %
772-776	NVMe/PCIe Reset Count
804-807	PCIe Gen1 Link Count
808-811	PCIe Gen2 Link Count
812-815	PCIe Gen3 Link Count
816-823	PCIe ECRC Event Count
824-831	PCIe LCRC Event Count
873	PCIe Power On Link Speed
876	PCIe Current Link Speed

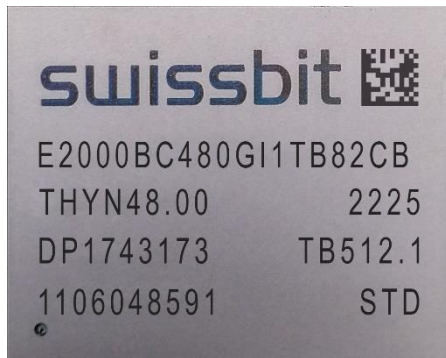
877	PCIe Current Link Width
878	PCIe ASPM Enabled
879	PCIe L1 Sub State Enabled
880-887	PS3 Resume Count
888-895	PS4 Resume Count
932-935	PCIe x1 Link Count
936-939	PCIe x2 Link Count
940-943	PCIe x3 Link Count
944-951	PCIe L1 Event Count

10. Part Number Decoder



11. Swissbit E2000 BGA Marking Specification

11.1 Top View



11.2 Marking Content

- Line 1: Swissbit
- Line 1A: Data Matrix Code (Content: Lot code)
- Line 2: Part number
- Line 3A: Swissbit internal information
- Line 3B: Date Code WWYY (WW = Work Week, YY = Year)
- Line 4A: Flash Lot Number, max. 10 digits
- Line 4B: Raw density
- Line 5: Swissbit internal information
- Line 5A: Suffix

12. Revision History

Table 21: Document Revision History

Date	Revision	Description	Revision Details
December 5, 2023	1.00	Initial release	Doc. req. no. 6745
January 4, 2024	1.01	Updated PN and product illustrations	Doc. req. no. 6802
January 15, 2024	1.02	Chapter 4.2 has been updated	Doc. req. no. 6817
April 30, 2024	1.03	Endurance table has been updated	Doc. req. no. 7058
August 7, 2024	1.04	Product features have been updated	P000000430
November 13, 2024	1.05	Table 12 has been updated	-
January 09, 2025	1.06	Adjusted ball assignment description	-
May 09, 2025	1.07	Updated Industrial Operating Temperature	-
May 26, 2025	1.08	Added variants with firmware "2", updated product illustrations and adjusted electrical interface.	-
September 04, 2025	1.09	Updated Identify Controller Data Structure (CNS 01h)	-
October 16, 2025	1.10	Added reflow profile information	-
November 19, 2025	1.11	Updated Ball Assignment, Name and Description (ball W7, C11)	-

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