Ordering number : EN*A1725

Preliminary

SANYO Semiconductors
DATA SHEET

STK621-047A-E — Thick-Film Hybrid IC 3-phase Inverter Motor Drive Inverter Hybrid IC

Overview

This IC is a 3-phase inverter power hybrid IC containing power elements (IGBT and FRD), pre-driver, over-current and excessive temperature protection circuit.

Applications

- 3-phase inverter motor drive

Features

- Integrates power elements (IGBT and FRD), pre-driver, and protective circuit.
- Protective circuits including over-current (bus line), excessive temperature and pre-drive low voltage protection are built in.
- Direct input of CMOS level control signals without an insulating circuit (photo-coupler, etc) is possible.(Hi Active)
- Single power supply drive is possible by using a bootstrap circuit with a built-in IC.
- Temperature monitor is possible by the thermistor inside the IC.
- Built-in simultaneous upper/lower ON prevention circuit to prevent arm shorting through simultaneous ON input for the upper and lower side transistors.
  (Dead time is required for preventing shorting due to switching delay.)
- SIP (The single in-line package) of the transfer full mold structure.

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Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Supply voltage	V_{CC}	+ - -, surge < 500V *1	450	V
Collector-emitter voltage	V_{CE}	+ - U (V, W) or U (V, W) - -	600	V
Output current	I_O	+, -, U, V, W terminal current	±20	A
Output peak current	Iop	+, -, U, V, W terminal current P.W. = 100μs	±40	A
Pre-driver supply voltage	VD1, 2, 3, 4	VB1 - U, VB2 - V, VB3 - W, V_{DD} - V_{SS} *2	20	V
Input signal voltage	V_{IN}	HIN1, 2, 3, LIN1, 2, 3 terminal	0 to 15	V
FAULT terminal voltage	VFAULT	FAULT terminal	20	V
Maximum loss	Pd	IGBT, Per 1 channel	44.6	W
Junction temperature	Tj	IGBT, FRD junction temperature	150	°C
Storage temperature	Tstg		-40 to +125	°C
Operating temperature	Tc	H-IC case temperature	-20 to +100	°C
Tightening torque	MT	A screw part at use M4 type screw *3	1.17	N•m
Withstand voltage	Vis	50Hz sine wave AC 1 minute *4	2000	VRMS

In the case without the instruction, the voltage standard is - terminal = V_{SS} terminal voltage.

*1 Surge voltage developed by the switching operation due to the wiring inductance between the + and – terminals.
*2 VD1 = between VB1-U, VD2 = VB2-V, VD3 = VB3-W, VD4 = V_{DD}-V_{SS}, terminal voltage.
*3 Flatness of the heat-sink should be lower than 0.25mm.
*4 The test condition is AC 2500V, 1 second.

Electrical Characteristics at Tc=25°C, VD=15V

Parameter	Symbol	Conditions		min	typ	max	unit
Power output part							
Collector-to-emitter cut-off current	I_{CE}	V_{CE} = 600V				0.1	mA
Boot-strap diode reverse current	IR (BD)	VR (BD) = 600V				0.1	mA
Collector-to-emitter saturation voltage	V_{CE} (sat)	I_O = 20A	Upper side		1.8	2.7	V
			Lower side		2.2	3.1	
Diode forward voltage	V_F	I_O = -20A	Upper side		1.6	2.5	V
			Lower side		2.0	2.9	
Junction-to-substrate thermal resistance	θj-c (T)	IGBT				2.8	°C/W
	θj-c (D)	FWD				3.0	°C/W
Control (Pre-driver) part							
Pre-drive power supply consumption electric current	I_D	VD1, 2, 3 = 15V			0.07	0.4	mA
		VD4 = 15V			1.6	4	
Input ON threshold voltage	Vinth (on)	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3-V_{SS} terminal		1.5	2.1	2.5	V
Input OFF threshold voltage	Vinth (off)			0.8	1.3	1.5	V
Input threshold voltage hysteresis	Vinth (hys)			(0.5)	(0.8)		V
Protection part							
Excessive temperature	TSD	The substrate surface		100		120	°C
Over-current protection electric current	ISD	P.W. = 100μs		24.2		30.4	A
Pre-drive low voltage protection	UVLO			10		12	V
FAULT terminal input electric current	IOSD	VFAULT = 0.1V			2		mA
FAULT clearness delay time	FLTCLR	After each protection operation ending		18		80	ms
Board Temperature Mounting resistance	Rt	Resistance between the FAULT and V_{SS} terminals		90	100	110	kΩ
Switching time	tON	I_O = 20A, Inductive load		0.3	0.6	1.3	μs
	tOFF				0.9	1.5	
Electric current output signal level	ISO	I_O = 20A		0.38	0.4	0.42	V
Reverse bias safe operating area	RBSOA	I_O = 40A, V_{CE} = 450V			Full Square		
Short circuit safe operating area	SCSOA	V_{CE} = 200V		4			μs
Allowable offset voltage slew rate	dv/dt	U (V, W) - - terminal		-50		50	V/ns

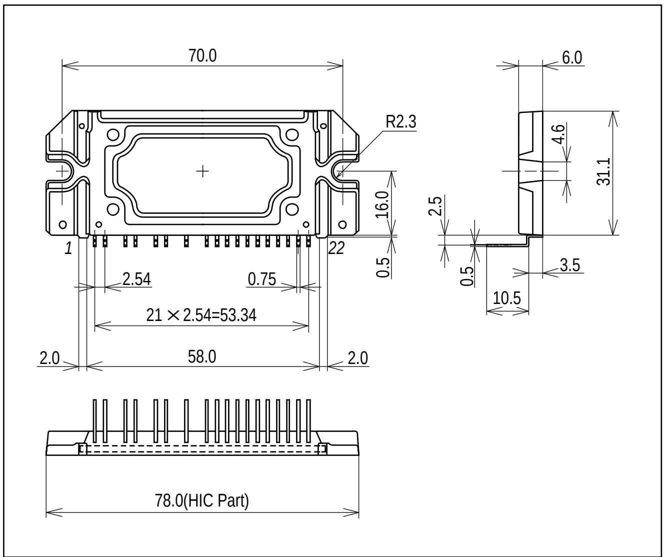
In the case without the instruction, the voltage standard is - terminal = V_{SS} terminal voltage.

Notes

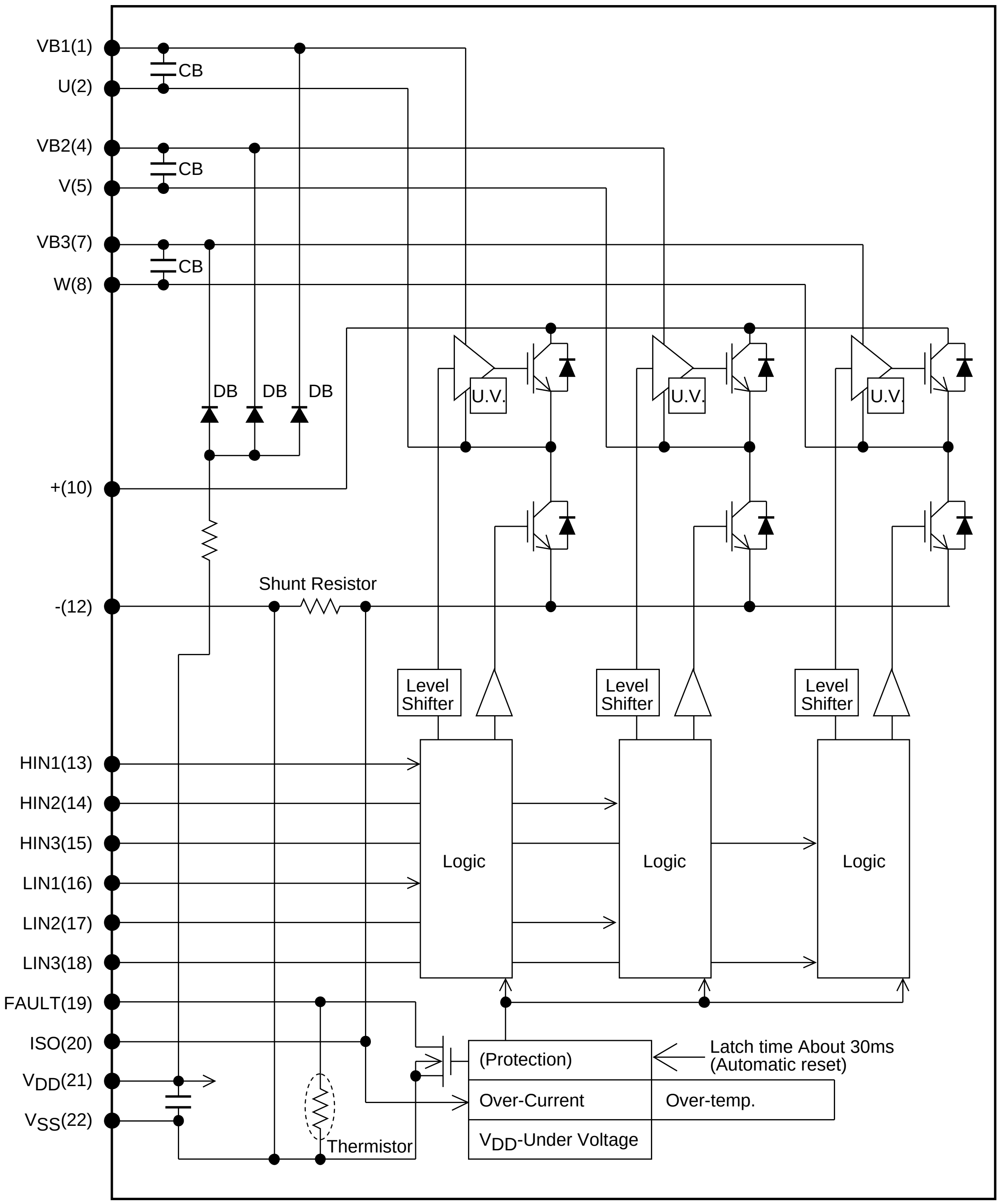
1. “Input ON threshold voltage” indicates a value to turn on output stage IGBT.
   “Input OFF threshold voltage” indicates a value to turn off output stage IGBT.
   At the time of output ON, set the input signal voltage Vinth (max) to 15V.
   At the time of output OFF, set the input signal voltage 0V to Vinth (min).
   *1 : ”Input threshold voltage hysteresis” indicates a reference value based on the design value of built-in pre-driver IC.
2. When the internal protection circuit operates, there is a Fault signal ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal doesn't latch.
   After protection operation ends, it returns automatically within about 18ms to 80ms and resumes operation beginning condition. So, after Fault signal detection, set OFF (Low) to all input signals at once.
   However, the operation of pre-drive power supply low voltage protection (UVLO: it has a hysteresis about 0.2V) is as follows.
   Upper side → There is no FAULT signal output, but it does a corresponding gate signal OFF.
   Incidentally, it returns to the regular operation when recovering to the normal voltage, but the latch continues among input signal ON (High).
   Lower side → It outputs FAULT signal with gate signal OFF.
   However, it is different from the protection operation of upper side, it automatically resets about 18ms to 80ms later and resumes operation beginning condition when recovering to normal voltage.
   (The protection operation doesn't latch by the input signal.)
3. When assembling the hybrid IC on the heat sink with M4 type screw, tightening torque range is 0.79N•m to 1.17N•m.
   Flatness of the heat-sink should be lower than 0.25mm.
4. The pre-drive low voltage protection is the feature to protect a device when the pre-driver supply voltage declines with the operating malfunction. As for the pre-driver supply voltage decline in case of operation beginning, and so on, we request confirmation in the set.

Package Dimensions

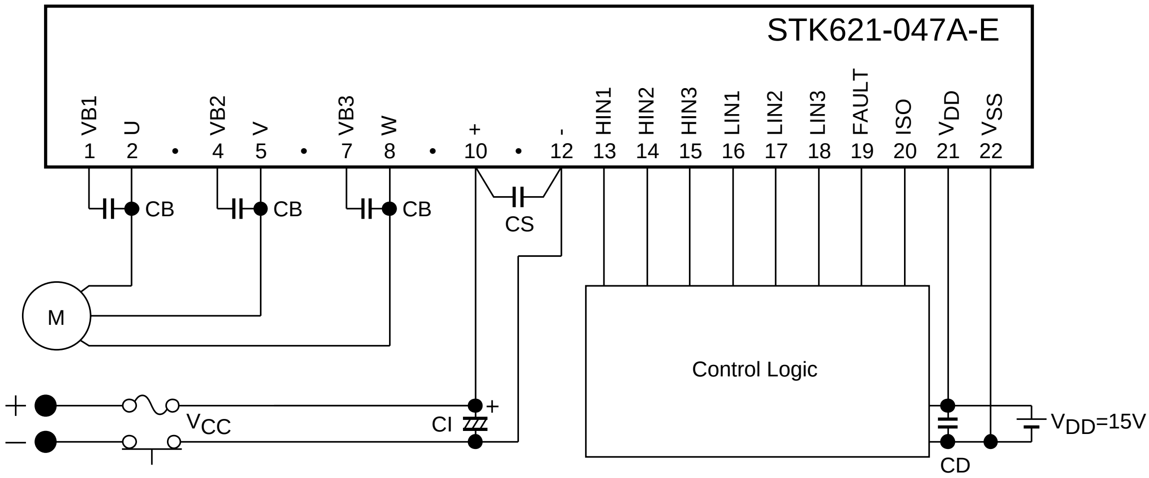
unit:mm (typ)



Internal equivalent circuit diagram



Example of the application circuit



Recommendation Operating Conditions

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage	V_{CC}	+ - - terminal	0	280	400	V
Pre-driver supply voltage	VD1, 2, 3	VB1 - U, VB2 - V, VB3 - W	12.5	15	17.5	V
	VD4	V_{DD} - V_{SS} *1	13.5	15	16.5	
ON state input voltage	V_{IN} (ON)	HIN1, HIN2, HIN3, LIN1, LIN2, LIN3 Terminal	3.0		5.0	V
OFF state input voltage	V_{IN} (OFF)		0		0.3	
PWM frequency	fPWM		1		20	kHz
Dead-time	DT	Upper/lower input signal downtime	2			µs
Allowable input pulse width	PWIN	ON and OFF	1			µs
Tightening torque	MT	‘M4’ type screw	0.79		1.17	N•m

*1 Pre-driver power supply (VD4 = 15±1.5V) must have the capacity of I_O = 20mA (DC), 0.5A (Peak).

Precautions

1. The STK621-047A-E can be driven with a single power supply by placing 1 to 47μF bootstrap capacitors (CB) between pins No.1 and No.2, pins No.4 and No.5, and pins No.7 and No.8 for each. In this technique, charge the bootstrap capacitors (CB) by turning the lower side MOSFETs on to output LOW. (Without this technique, each upper side MOSFET needs external power supply independently.) If more than 47μF capacitance is used for this technique, connect a resistor (around 20Ω) between upper side power supply pin (VB1/2/3) and the capacitor in series for each. Since the upper side supply voltage is insufficient due to the control technique, check whether the voltage is adequate or not by testing on the actual application.

2. Switching operation can be affected by the floating inductance of the external wiring connected to + and – pins and some voltage spike occurs. To prevent this, shorten the length of wire from CI to each pin as much as possible to minimize the wiring inductance. In addition, configure a snubber circuit by connecting a capacitor CS2 of about 0.22 to 10μF to suppress surge voltage.

3. ISO pin (pin 20) is used to monitor current. Connect 5.6kΩ or more resistance externally. Do not have ISO pin short-circuited to V_{SS} pin. That disables the overcurrent protection.

4. The FAULT/EN pin (pin 19) operates when the signal is low (open drain output). Since a thermistor is built in between FAULT and V_{SS} pins, the substrate temperature can be monitored using the divided voltage with the pull-up resistor RP. For the pull-up resistance, connect 10kΩ or larger capacitor when VP = 5V, 39kΩ or larger capacitor when VP = 15V.

5. Though the STK621-047A-E incorporates 33kΩ (typ) pull-down resistance connected to signal input pins, to further decrease the influence of wiring noise, connect 2.2kΩ to 3.3kΩ pull-down resistors also externally.

6. The overcurrent protection is effective only when the controller operates normally. To assure further safety, set a fuse in V_{CC} line.

7. The HIC may be destroyed if the motor connecting pin (pins 4, 6, or 8) becomes open when the motor is in rotation. Pay attention to the connecting condition of these pins including soldering condition.

8. When the input signal pulse width is shorter than 1μs, there are times the output does not respond to the input signal for neither ON nor OFF operation.

* This sample application circuit does not guarantee the design of mass production.

This catalog provides information as of October, 2010. Specifications and information herein are subject to change without notice.