

Ordering Information		
Part Numbers	Description	Module Speed
SG572128FH8P0LC	512Mx72 (4GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 256Mx8 Based, DDR3-1066-7-7-7, 1.5V, 30.00mm, Green Module (RoHS Compliant).	PC3-8500 @ CL 7, 8
SG572128FH8P0PH	512Mx72 (4GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 256Mx8 Based, DDR3-1333-9-9-9, 1.5V, 30.00mm, Green Module (RoHS Compliant).	PC3-10600 @ CL 9
SG572128FH8P0RN	512Mx72 (4GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 256Mx8 Based, DDR3-1600-11-11-11, 1.5V, 30.00mm, Green Module (RoHS Compliant).	PC3-12800 @ CL 11
SG572128FJ8P0LC	512Mx72 (4GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 256Mx8 Based, DDR3-1066-7-7-7, 1.35V/1.5V, 30.00mm, Green Module (RoHS Compliant).	PC3L-8500 @ CL 7, 8
SG572128FJ8P0PH	512Mx72 (4GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 256Mx8 Based, DDR3-1333-9-9-9, 1.35V/1.5V, 30.00mm, Green Module (RoHS Compliant).	PC3L-10600 @ CL 9
SG572128FJ8P0RN	512Mx72 (4GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 256Mx8 Based, DDR3-1600-11-11-11, 1.35V/1.5V, 30.00mm, Green Module (RoHS Compliant).	PC3L-12800 @ CL 11

(All specifications of this module are subject to change without notice.)

Revision History

- **April 26, 2010**

Changed datasheet part number from SG572128FH8P0UU to SG572128FU8P0UU because of the addition of a new module voltage.

Added SG572128FH8P0RN, SG572128FJ8P0LC, SG572128FJ8P0PH & SG572128FJ8P0RN to the Ordering Information on page 1.

- **March 2, 2010**

Datasheet released.

4GByte (512Mx72) DDR3 SDRAM Module - 256Mx8 Based 240-pin DIMM, Registered, Parity, ECC

Features

- Standard = JEDEC
- Configuration = ECC
- Number of Module Ranks = 2
- Number of Devices = 18
- $V_{DD} = V_{DDQ} = 1.35V/1.5V$ or 1.5V
- $V_{DDSPD} = 1.7V$ to 3.6V
- Cycle Time = 1.875 (PC3-8500)
1.5ns (PC3-10600)
1.25ns (PC3-12800)
- $\overline{CAS}$ Latency = 5, 6, 7, 8, 9, 10, 11
- Additive Latency = 0, CL-1, and CL-2
- $\overline{CAS}$ Write Latency (CWL) = 5, 6, 7, 8
- Burst Length = BC4, BL8, BC4 or BL8 (on the fly)
- Burst Length = Nibble Sequential & Interleave Mode
- Internal Banks per SDRAM = 8
- Refresh = 8K/64ms
- Device Package = FBGA
- Lead Finish = Gold
- Length x Height = 133.35mm x 30.00mm
- No. of sides = Double-sided
- Mating Connector (Examples)
Vertical = AMP - 5-1932000-9
- ZQ calibration supported
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM write data-in at both the rising and falling edges of the data strobe
- All addresses and control inputs latched on the rising edges of the clock
- Dynamic On Die Termination supported
- Driver strength selected by EMRS
- Asynchronous RESET pin supported
- Write Levelization supported
- 8-bit pre-fetch

Addressing

Device Configuration	256Mx8
Number of Internal Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BC switch on the fly	A12/ $\overline{BC}$
Row Address	A0 - A14
Column Address	A0 - A9

Pin Description Table

Symbol	Type	Polarity	Function
$\overline{CK0} \sim \overline{CK1}$, $\overline{CK0} \sim \overline{CK1}$	SSTL_15	Differential Crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM address/control inputs are sampled on the crossing of the positive edge of CK and the negative edge of $\overline{CK}$. Output (read) data is referenced to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE0, CKE1	SSTL_15	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0} \sim \overline{CS1}$	SSTL_15	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
ODT0, ODT1	SSTL_15	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming this function is enabled on the DRAM.
BA0~BA2	SSTL_15	-	Selects which SDRAM bank of the eight is activated.

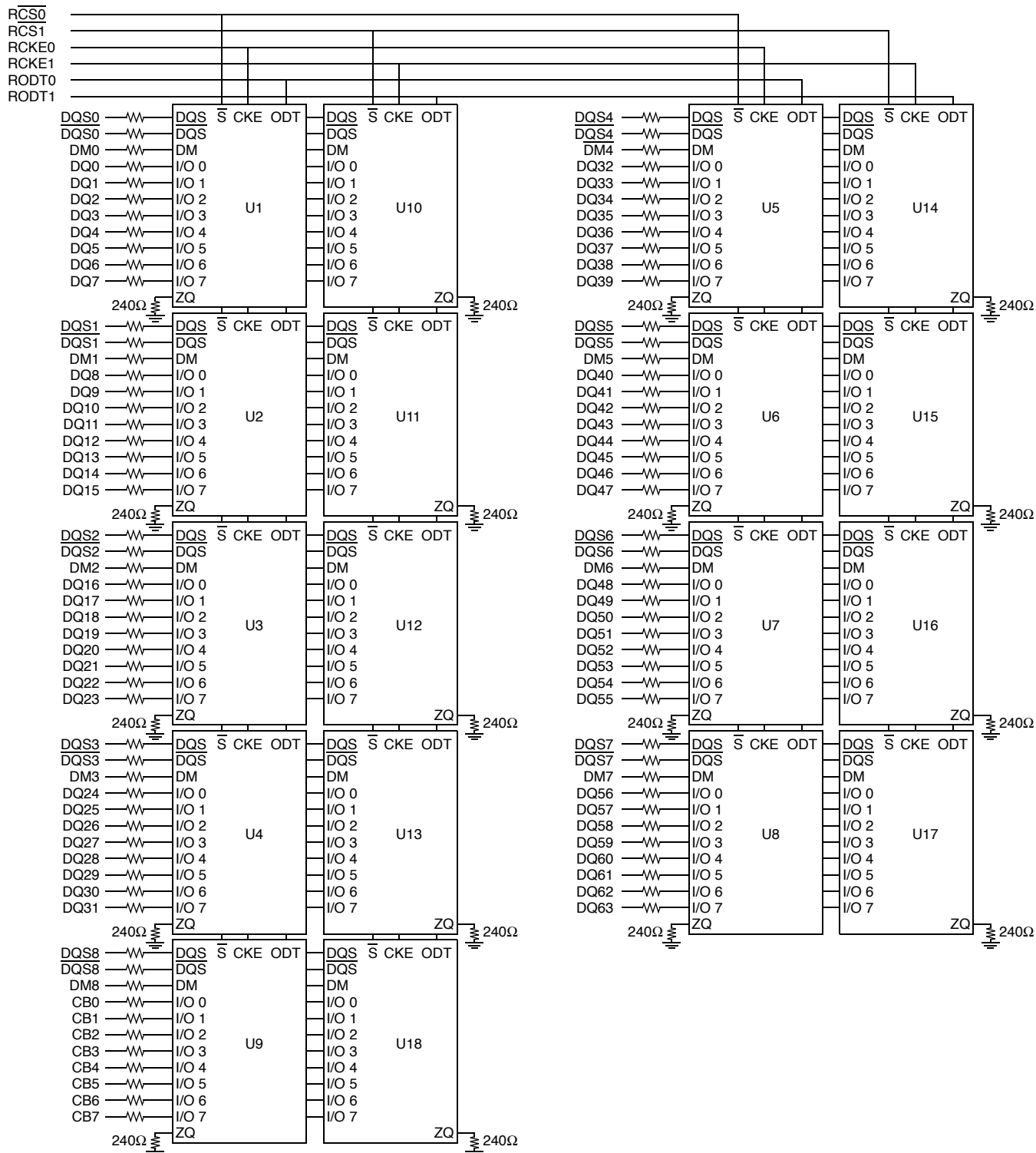
Pin Description Table (Contd.)

Symbol	Type	Polarity	Function
A0~A15	Input	-	During a Bank Activate command cycle, address inputs define the row address (RA0-RA14). During a Read or Write command cycle, address inputs define the column address (CA0-CA9). In addition to the column address, AP is used to invoke auto-precharge operation at the end of the burst read or write cycle. If AP is high, auto-precharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to pre-charge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped). A15 is only connected to the register for the parity check.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DQ0~DQ63 CB0~CB7	Input/ Output	-	Data and Check Bit Input/Output pins.
DQS0~DQS8 $\overline{DQS0}$ ~ $\overline{DQS8}$	Input/ Output	Differential Crossing	Data strobe for input and output data.
DM0~DM8	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
PAR_IN	Input	Active High	Parity bit for the Address and Control bus. ("1": Odd, "0": Even)
$\overline{ERR_OUT}$	Output	Active Low	Parity error detected on the Address and Control bus. A resistor may be connected from $\overline{ERR_OUT}$ bus line to V_{DD} on the system planar to act as a pull up.
SA0~SA2	Input	-	These signals are tied at the system to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	Input/ Output	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus tied to V_{DDSPD} to act as a pullup on the system board.
$\overline{EVENT}$	Output	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part. No pull-up resistor is provided on DIMM.
$\overline{RESET}$	Input	Active Low	Asynchronous Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} .
V_{DD} , V_{SS}	Supply	-	Power and ground for the DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules. V_{SS} pins are tied to V_{SS} planes on these modules.
V_{DDQ}	Supply	-	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. V_{DDQ} shares the same power plane as V_{DD} pins.
V_{REFDQ}	Supply		Reference voltage for I/O inputs.
V_{REFCA}	Supply	-	Reference voltage for address/command inputs.
V_{DDSPD}	Supply	-	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.
V_{TT}	Supply	-	Termination voltage for address/command/control/clock nets.
NC	-	-	No Connect.

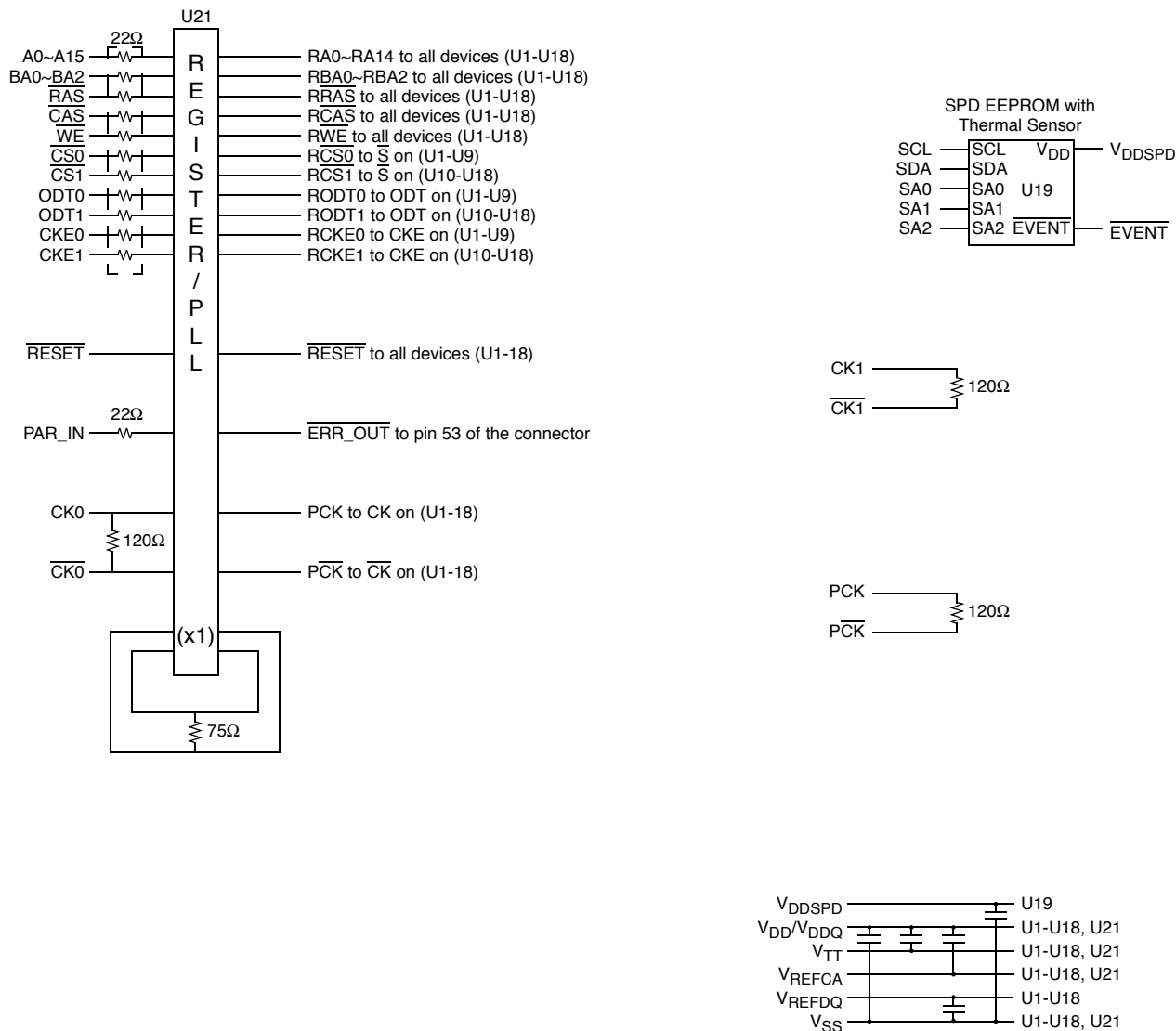


DDR3 240-pin DIMM Pin List

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	V _{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V _{SS}	151	V _{SS}	181	A1	211	V _{SS}
2	V _{SS}	32	V _{SS}	62	V _{DD}	92	V _{SS}	122	DQ4	152	DM3	182	V _{DD}	212	DM5
3	DQ0	33	$\overline{\text{DQS3}}$	63	CK1	93	$\overline{\text{DQS5}}$	123	DQ5	153	NC	183	V _{DD}	213	NC
4	DQ1	34	DQS3	64	$\overline{\text{CK1}}$	94	DQS5	124	V _{SS}	154	V _{SS}	184	CK0	214	V _{SS}
5	V _{SS}	35	V _{SS}	65	V _{DD}	95	V _{SS}	125	DM0	155	DQ30	185	$\overline{\text{CK0}}$	215	DQ46
6	$\overline{\text{DQS0}}$	36	DQ26	66	V _{DD}	96	DQ42	126	NC	156	DQ31	186	V _{DD}	216	DQ47
7	DQS0	37	DQ27	67	V _{REFCA}	97	DQ43	127	V _{SS}	157	V _{SS}	187	$\overline{\text{EVENT}}$	217	V _{SS}
8	V _{SS}	38	V _{SS}	68	PAR_IN	98	V _{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	V _{DD}	99	DQ48	129	DQ7	159	CB5	189	V _{DD}	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	V _{SS}	160	V _{SS}	190	BA1	220	V _{SS}
11	V _{SS}	41	V _{SS}	71	BA0	101	V _{SS}	131	DQ12	161	DM8	191	V _{DD}	221	DM6
12	DQ8	42	$\overline{\text{DQS8}}$	72	V _{DD}	102	$\overline{\text{DQS6}}$	132	DQ13	162	NC	192	$\overline{\text{RAS}}$	222	NC
13	DQ9	43	DQS8	73	$\overline{\text{WE}}$	103	DQS6	133	V _{SS}	163	V _{SS}	193	$\overline{\text{CS0}}$	223	V _{SS}
14	V _{SS}	44	V _{SS}	74	$\overline{\text{CAS}}$	104	V _{SS}	134	DM1	164	CB6	194	V _{DD}	224	DQ54
15	$\overline{\text{DQS1}}$	45	CB2	75	V _{DD}	105	DQ50	135	NC	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	$\overline{\text{CS1}}$	106	DQ51	136	V _{SS}	166	V _{SS}	196	A13	226	V _{SS}
17	V _{SS}	47	V _{SS}	77	ODT1	107	V _{SS}	137	DQ14	167	NC	197	V _{DD}	227	DQ60
18	DQ10	48	NC	78	V _{DD}	108	DQ56	138	DQ15	168	$\overline{\text{RESET}}$	198	$\overline{\text{CS3}}$ (NC)	228	DQ61
19	DQ11	49	NC	79	$\overline{\text{CS2}}$ (NC)	109	DQ57	139	V _{SS}	169	CKE1	199	V _{SS}	229	V _{SS}
20	V _{SS}	50	CKE0	80	V _{SS}	110	V _{SS}	140	DQ20	170	V _{DD}	200	DQ36	230	DM7
21	DQ16	51	V _{DD}	81	DQ32	111	$\overline{\text{DQS7}}$	141	DQ21	171	A15	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V _{SS}	172	A14	202	V _{SS}	232	V _{SS}
23	V _{SS}	53	$\overline{\text{ERR_OUT}}$	83	V _{SS}	113	V _{SS}	143	DM2	173	V _{DD}	203	DM4	233	DQ62
24	$\overline{\text{DQS2}}$	54	V _{DD}	84	$\overline{\text{DQS4}}$	114	DQ58	144	NC	174	A12/ $\overline{\text{BC}}$	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V _{SS}	175	A9	205	V _{SS}	235	V _{SS}
26	V _{SS}	56	A7	86	V _{SS}	116	V _{SS}	146	DQ22	176	V _{DD}	206	DQ38	236	V _{DDSPD}
27	DQ18	57	V _{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V _{SS}	178	A6	208	V _{SS}	238	SDA
29	V _{SS}	59	A4	89	V _{SS}	119	SA2	149	DQ28	179	V _{DD}	209	DQ44	239	V _{SS}
30	DQ24	60	V _{DD}	90	DQ40	120	V _{TT}	150	DQ29	180	A3	210	DQ45	240	V _{TT}

Block Diagram


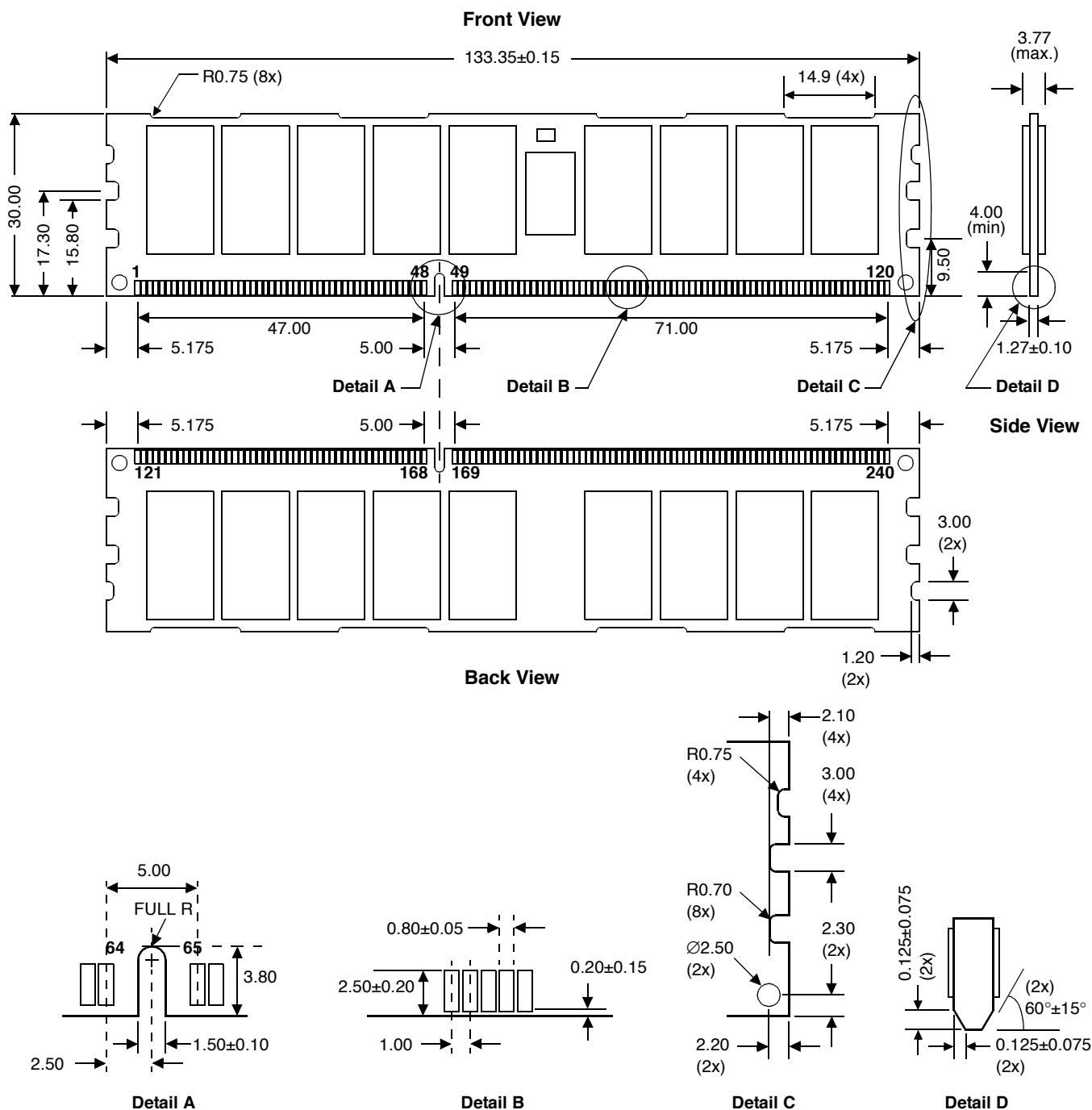
Note: Unless otherwise noted, data resistor values are $15\Omega \pm 5\%$.

Block Diagram (Contd.)

Notes:

- Each address, clock, command and control signal output line from the register is terminated at the end of the line through a 39Ω series resistor to V_{TT}.
- Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 6.

Physical Dimensions

240-pin DIMM Module



(All dimensions are in millimeters with $\pm 0.15\text{mm}$ tolerance unless specified otherwise.)

1.35V Serial Presence Detect Table (SG572128FJ8P0LC/PH/RN)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
0	No. of Bytes Used, No. of Bytes in SPD Device, CRC Coverage	All	176, 256, 0~116	92h
1	SPD Revision	All	Revision 1.0	10h
2	Key Byte/DRAM Device Type	All	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	All	RDIMM	01h
4	SDRAM Density and Banks	All	2Gb, 8 Banks	03h
5	SDRAM Addressing	All	15 Rows, 10 Columns	19h
6	Module Nominal Voltage, V_{DD}	All	1.35V/1.5V	02h
7	Module Organization	All	2 Ranks, x8	09h
8	Module Memory Bus Width	All	x72	0Bh
9	Fine Timebase (FTB) Dividend/Divisor	All	2.5ps	52h
10	Medium Timebase Dividend	All	1	01h
11	Medium Timebase Divisor	All	8	08h
12	Minimum SDRAM Cycle Time (t_{CKmin})	-LC -PH -RN	1.875ns 1.5ns 1.25ns	0Fh 0Ch 0Ah
13	Reserved	All	-	00h
14	CAS Latencies Supported (CL4-CL11)	-LC -PH -RN	5, 6, 7, 8 5, 6, 7, 8, 9 5, 6, 7, 8, 9, 10, 11	1Eh 3Eh FEh
15	CAS Latencies Supported (CL12-CL18)	All	-	00h
16	Minimum CAS Latency Time (t_{AAmin})	All	13.125ns	69h
17	Minimum Write Recovery Time (t_{WRmin})	All	15ns	78h
18	Minimum $\overline{RAS}$ to CAS Delay Time (t_{RCDmin})	All	13.125ns	69h
19	Minimum Row Active to Row Active Delay Time (t_{RRDmin})	-LC -PH/RN	7.5ns 6ns	3Ch 30h
20	Minimum Row Precharge Delay Time (t_{RPmin})	All	13.125ns	69h
21	Upper Nibbles for t_{RAS} and t_{RC}	All	-	11h
22	Minimum Active to Precharge Delay Time (t_{RASmin})	-LC -PH -RN	37.5ns 36ns 35ns	2Ch 20h 18h

1.35V Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
23	Minimum Active to Active/Refresh Delay Time (t_{RCmin})	-LC -PH -RN	50.625ns 49.125ns 48.125ns	95h 89h 81h
24	Minimum Refresh Recovery Delay Time (t_{RFCmin}) (LSB)	All	160ns	00h
25	Minimum Refresh Recovery Delay Time (t_{RFCmin}) (MSB)	All	160ns	05h
26	Minimum Internal Write to Read Command Delay Time (t_{WTRmin})	All	7.5ns	3Ch
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTPmin})	All	7.5ns	3Ch
28	Upper Nibble for t_{FAW}	-LC -PH/RN	37.5ns 30ns	01h 00h
29	Minimum Four Active Window Delay Time (t_{FAW})	-LC -PH/RN	37.5ns 30ns	2Ch F0h
30	SDRAM Output Drivers Supported	All	DLL-off Mode, RZQ/7, RZQ/6	83h
31	SDRAM Thermal and Refresh Options	All	ASR, Ext. Temp. Range	05h
32	Module Thermal Sensor	All	EEPROM with Thermal Sensor	80h
33	SDRAM Device Type	All	Monolithic	00h
34~59	Reserved	All	-	00h
60	Module Nominal Height	All	30.00mm	0Fh
61	Module Maximum Thickness	All	Front = 1.2mm Back = 1.2mm	11h
62	Reference Raw Card Used	All	R/C B, Rev. 0	01h
63	DIMM Module Attributes	All	1 Row, 1 Register	05h
64	RDIMM Thermal Heat Spreader	All	None	00h
65	Register Manufacturer ID Code (LSB)	All	Generic	00h
66	Register Manufacturer ID Code (MSB)	All	Generic	00h
67	Register Revision Number	All	-	FFh
68	Register Type	All	SSTE32882	00h

1.35V Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
69	RC1 (MS Nibble) / RC0 (MS Nibble)	All	Raw Card B	01h
70	RC3 (MS Nibble) / RC2 (MS Nibble)	All	Raw Card B	50h
71	RC5 (MS Nibble) / RC4 (MS Nibble)	All	Raw Card B	00h
72	RC7 (MS Nibble) / RC6 (MS Nibble)	All	Raw Card B	00h
73	RC9 (MS Nibble) / RC8 (MS Nibble)	All	Raw Card B	10h
74	RC11 (MS Nibble) / RC10 (MS Nibble)	-LC -PH -RN	1.35V DDR3-1066 1.35V DDR3-1333 1.35V DDR3-1600	11h 12h 13h
75	RC13 (MS Nibble) / RC12 (MS Nibble)	All	Raw Card B	00h
76	RC15 (MS Nibble) / RC14 (MS Nibble)	All	Raw Card B	00h
77~116	Reserved	All	-	00h
117	Module Manufacturer ID Code (LSB)	All	Continuation Code	01h
118	Module Manufacturer ID Code (MSB)	All	Smart ID code	94h
119	Module Manufacturing Location	All	See Note 1	01h
120	Module Manufacturing Date (Year)	All	Date	Date
121	Module Manufacturing Date (Week)	All	Date	Date
122~125	Module Serial Number	All	Serial Number	S. No
126	SPD Cyclical Redundancy Code	-LC -PH -RN		FEh 22h 9Ch
127	SPD Cyclical Redundancy Code	-LC -PH -RN		45h 53h E6h
128~145	Module Part Number	-LC -PH -RN	SG572128FJ8P0LC SG572128FJ8P0PH SG572128FJ8P0RN	
146	Module Revision Code (SPD Revision)	All	Revision 0	00h
147	Module Revision Code	All	-	00h
148	DRAM Manufacturer ID Code (LSB)	All	Generic	00h
149	DRAM Manufacturer ID Code (MSB)	All	Generic	00h

1.35V Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
150~173	Manufacturer Specific Data	All	SMART Modular Technologies	
174~175	Manufacturer Specific Data	All	-	00h
176~255	Open for Customer use	All	-	00h

Note:

- Manufacturing Location:
 00h - Undefined,
 01h - Fremont, USA,
 02h - Aguada, Puerto Rico,
 03h - East Kilbride, Scotland,
 04h - Penang, Malaysia,
 05h - Bangalore, India,
 06h - Sao Paulo, Brazil,
 07h - Aguadilla, Puerto Rico,
 08h - Mayaguez, Puerto Rico,
 09h - Santo Domingo, Dominican Republic,
 0Ah - Dongguan, China,

1.5V Serial Presence Detect Table (SG572128FH8P0LC/PH/RN)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
0	No. of Bytes Used, No. of Bytes in SPD Device, CRC Coverage	All	176, 256, 0~116	92h
1	SPD Revision	All	Revision 1.0	10h
2	Key Byte/DRAM Device Type	All	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	All	RDIMM	01h
4	SDRAM Density and Banks	All	2Gb, 8 Banks	03h
5	SDRAM Addressing	All	15 Rows, 10 Columns	19h
6	Module Nominal Voltage, V_{DD}	All	1.5V	00h
7	Module Organization	All	2 Ranks, x8	09h
8	Module Memory Bus Width	All	x72	0Bh
9	Fine Timebase (FTB) Dividend/Divisor	All	2.5ps	52h
10	Medium Timebase Dividend	All	1	01h
11	Medium Timebase Divisor	All	8	08h
12	Minimum SDRAM Cycle Time (t_{CKmin})	-LC -PH -RN	1.875ns 1.5ns 1.25ns	0Fh 0Ch 0Ah
13	Reserved	All	-	00h
14	CAS Latencies Supported (CL4-CL11)	-LC -PH -RN	5, 6, 7, 8 5, 6, 7, 8, 9 5, 6, 7, 8, 9, 10, 11	1Eh 3Eh FEh
15	CAS Latencies Supported (CL12-CL18)	All	-	00h
16	Minimum CAS Latency Time (t_{AAmin})	All	13.125ns	69h
17	Minimum Write Recovery Time (t_{WRmin})	All	15ns	78h
18	Minimum RAS to CAS Delay Time (t_{RCDmin})	All	13.125ns	69h
19	Minimum Row Active to Row Active Delay Time (t_{RRDmin})	-LC -PH/RN	7.5ns 6ns	3Ch 30h
20	Minimum Row Precharge Delay Time (t_{RPmin})	All	13.125ns	69h
21	Upper Nibbles for t_{RAS} and t_{RC}	All	-	11h
22	Minimum Active to Precharge Delay Time (t_{RASmin})	-LC -PH -RN	37.5ns 36ns 35ns	2Ch 20h 18h

1.5V Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
23	Minimum Active to Active/Refresh Delay Time (t_{RCmin})	-LC -PH -RN	50.625ns 49.125ns 48.125ns	95h 89h 81h
24	Minimum Refresh Recovery Delay Time (t_{RFCmin}) (LSB)	All	160ns	00h
25	Minimum Refresh Recovery Delay Time (t_{RFCmin}) (MSB)	All	160ns	05h
26	Minimum Internal Write to Read Command Delay Time (t_{WTRmin})	All	7.5ns	3Ch
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTPmin})	All	7.5ns	3Ch
28	Upper Nibble for t_{FAW}	-LC -PH/RN	37.5ns 30ns	01h 00h
29	Minimum Four Active Window Delay Time (t_{FAW})	-LC -PH/RN	37.5ns 30ns	2Ch F0h
30	SDRAM Output Drivers Supported	All	DLL-off Mode, RZQ/7, RZQ/6	83h
31	SDRAM Thermal and Refresh Options	All	ASR, Ext. Temp. Range	05h
32	Module Thermal Sensor	All	EEPROM with Thermal Sensor	80h
33	SDRAM Device Type	All	Monolithic	00h
34~59	Reserved	All	-	00h
60	Module Nominal Height	All	30.00mm	0Fh
61	Module Maximum Thickness	All	Front = 1.2mm Back = 1.2mm	11h
62	Reference Raw Card Used	All	R/C B, Rev. 0	01h
63	DIMM Module Attributes	All	1 Row, 1 Register	05h
64	RDIMM Thermal Heat Spreader	All	None	00h
65	Register Manufacturer ID Code (LSB)	All	Generic	00h
66	Register Manufacturer ID Code (MSB)	All	Generic	00h
67	Register Revision Number	All	-	FFh
68	Register Type	All	SSTE32882	00h

1.5V Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
69	RC1 (MS Nibble) / RC0 (MS Nibble)	All	Raw Card B	01h
70	RC3 (MS Nibble) / RC2 (MS Nibble)	All	Raw Card B	50h
71	RC5 (MS Nibble) / RC4 (MS Nibble)	All	Raw Card B	00h
72	RC7 (MS Nibble) / RC6 (MS Nibble)	All	Raw Card B	00h
73	RC9 (MS Nibble) / RC8 (MS Nibble)	All	Raw Card B	10h
74	RC11 (MS Nibble) / RC10 (MS Nibble)	-LC -PH -RN	1.5V DDR3-1066 1.5V DDR3-1333 1.5V DDR3-1600	01h 02h 03h
75	RC13 (MS Nibble) / RC12 (MS Nibble)	All	Raw Card B	00h
76	RC15 (MS Nibble) / RC14 (MS Nibble)	All	Raw Card B	00h
77~116	Reserved	All	-	00h
117	Module Manufacturer ID Code (LSB)	All	Continuation Code	01h
118	Module Manufacturer ID Code (MSB)	All	Smart ID code	94h
119	Module Manufacturing Location	All	See Note 1	01h
120	Module Manufacturing Date (Year)	All	Date	Date
121	Module Manufacturing Date (Week)	All	Date	Date
122~125	Module Serial Number	All	Serial Number	S. No
126	SPD Cyclical Redundancy Code	-LC -PH -RN		33h EFh 51h
127	SPD Cyclical Redundancy Code	-LC -PH -RN		0Ah 1Ch A9h
128~145	Module Part Number	-LC -PH -RN	SG572128FH8P0LC SG572128FH8P0PH SG572128FH8P0RN	
146	Module Revision Code (SPD Revision)	All	Revision 0	00h
147	Module Revision Code	All	-	00h
148	DRAM Manufacturer ID Code (LSB)	All	Generic	00h
149	DRAM Manufacturer ID Code (MSB)	All	Generic	00h

1.5V Serial Presence Detect Table (Contd.)

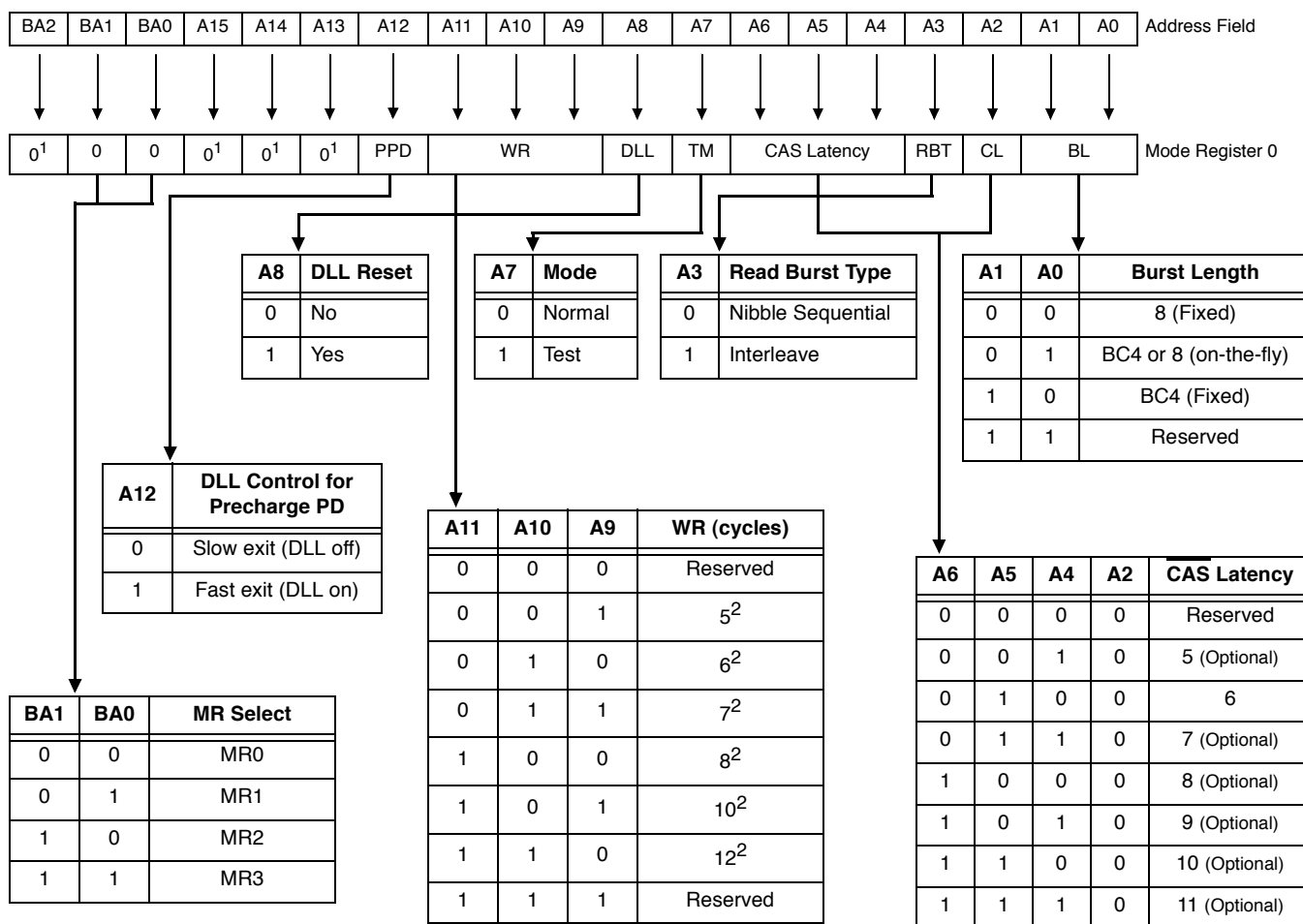
Byte No.	Byte Description	Speed	Value Supported	Hex Value
150~173	Manufacturer Specific Data	All	SMART Modular Technologies	
174~175	Manufacturer Specific Data	All	-	00h
176~255	Open for Customer use	All	-	00h

Note:

- Manufacturing Location:
 00h - Undefined,
 01h - Fremont, USA,
 02h - Aguada, Puerto Rico,
 03h - East Kilbride, Scotland,
 04h - Penang, Malaysia,
 05h - Bangalore, India,
 06h - Sao Paulo, Brazil,
 07h - Aguadilla, Puerto Rico,
 08h - Mayaguez, Puerto Rico,
 09h - Santo Domingo, Dominican Republic,
 0Ah - Dongguan, China,

Mode Register (MR0) Table Definition

The mode register stores the data for controlling the various operating modes of DDR3 SDRAM. It controls CAS latency, burst length, burst chop, burst sequence, test mode, DLL reset, t_{WR} and various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1 and BA2 while controlling the state of address pins A0~A15.

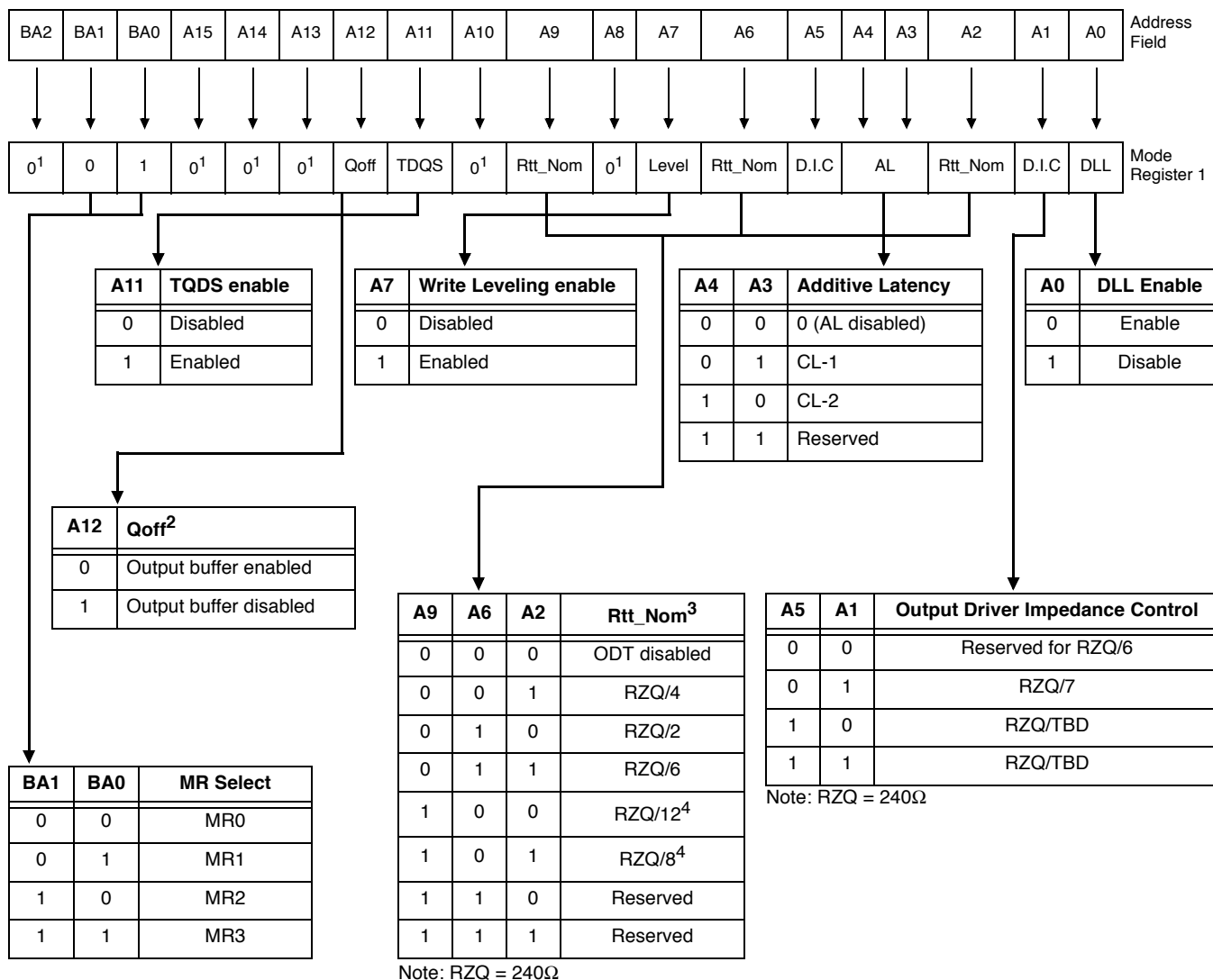


Notes:

- BA2 and A13~A15 are reserved for future use and must be programmed to 0 during MRS.
- WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Round-up}(t_{WR}[\text{ns}] / t_{CK}[\text{ns}])$. The WR value in the mode register must be programmed to be equal or larger than WR_{min} . The programmed WR value is used with t_{RP} to determine t_{DAL} .

Mode Register (MR1) Table Definition

The Mode Registers MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write Leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1 and BA2, while controlling the state of address pins A0~A15.

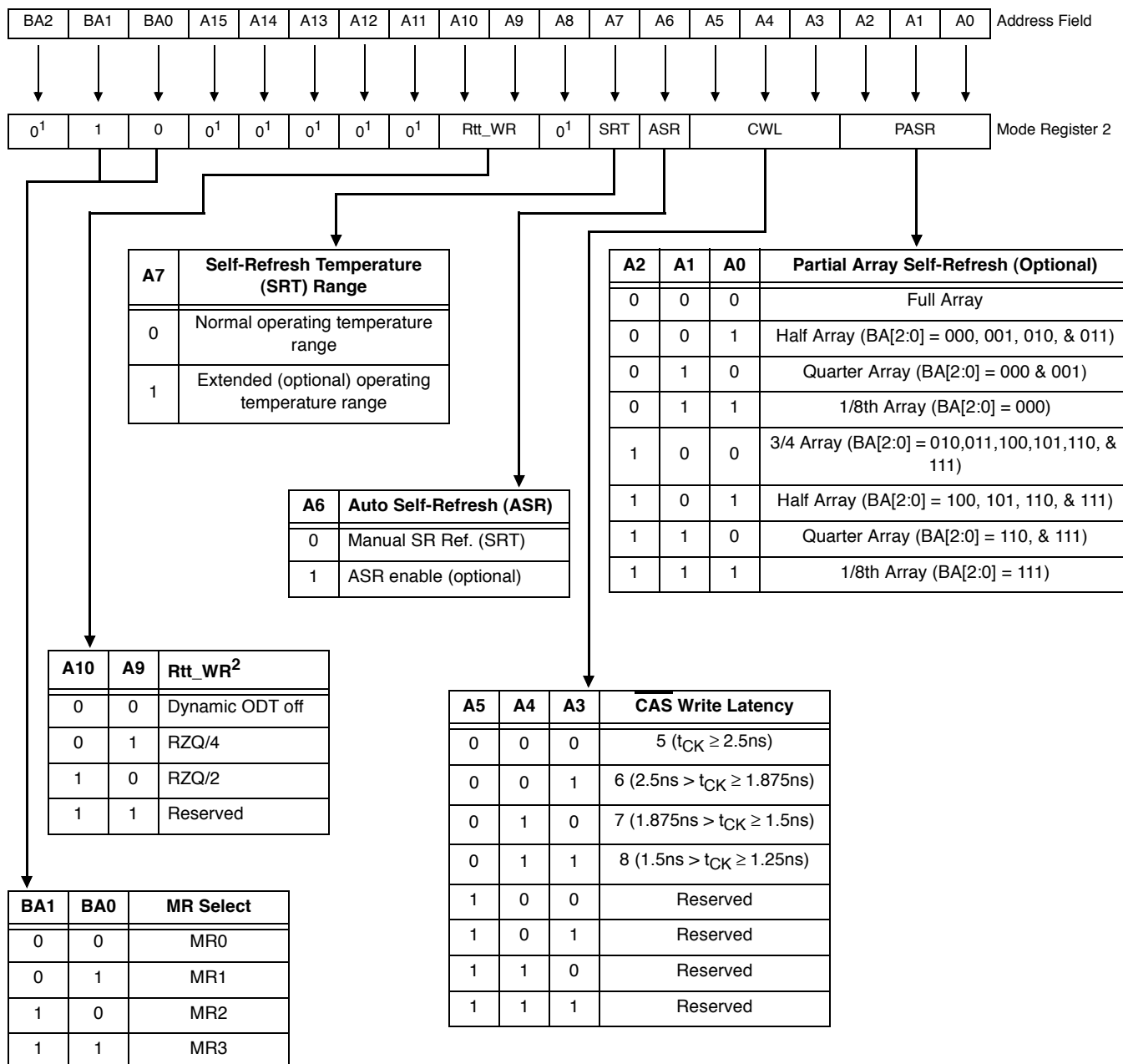


Notes:

- BA2 and A8, A10, A13~A15 are reserved for future use and must be programmed to 0 during MRS.
- Outputs disabled - DQs, DQSs, DQSs.
- In Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all Rtt_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only Rtt_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
- If Rtt_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

Mode Register (MR2) Table Definition

The Mode Registers MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS Write Latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and low on BA0 and BA2 while controlling the state of address pins A0~A15.

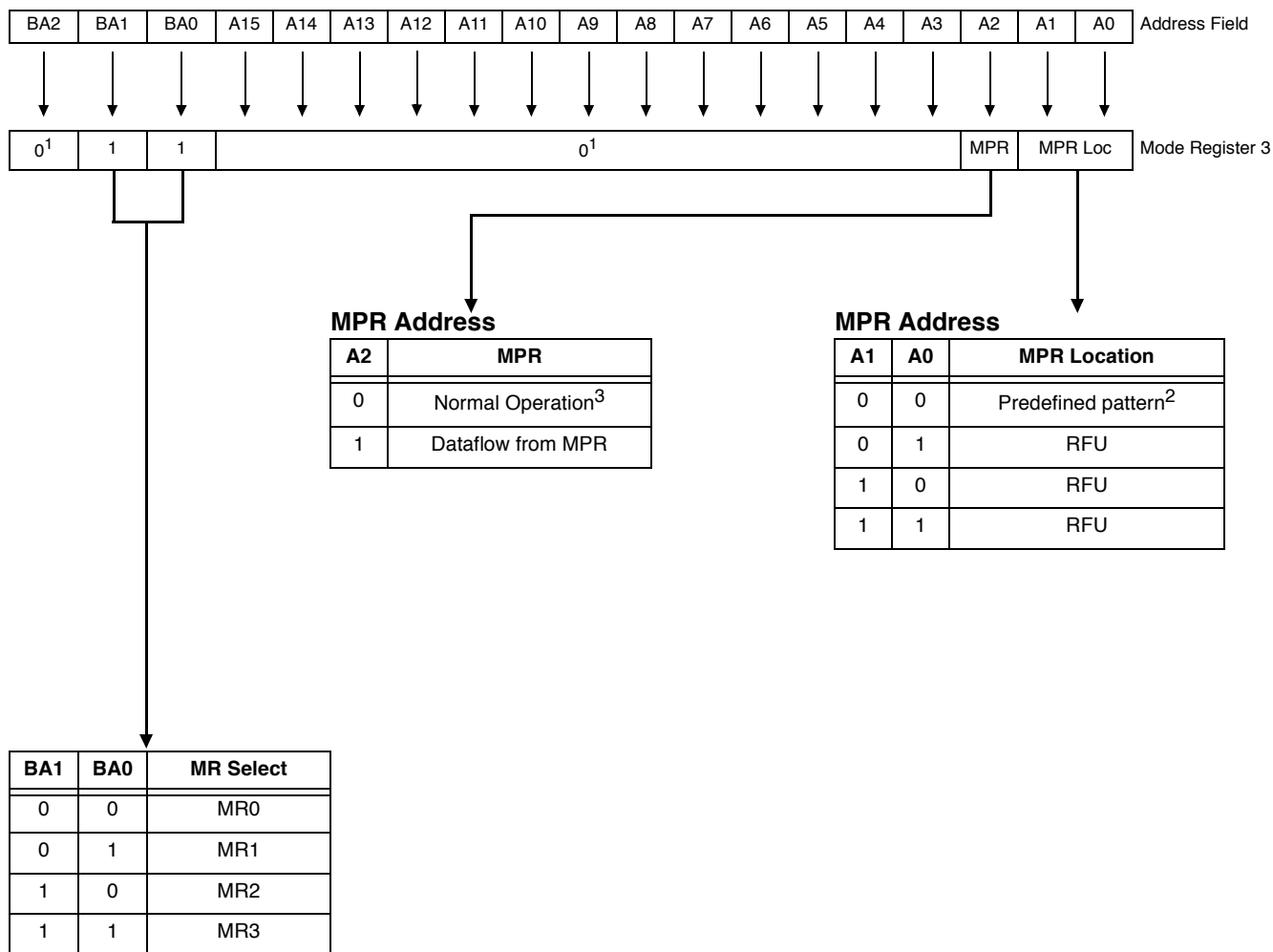


Notes:

- BA2, A8 and A11~A15 are reserved for future use and must be programmed to 0 during MRS.
- If Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During Write Leveling, Dynamic ODT is not available.

Mode Register (MR3) Table Definition

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, low on BA2 while controlling the state of address pins A0~A15.



Notes:

1. BA2, A3~A15 are reserved for future use and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0), then MR3 A[1:0] will be ignored.

Command Truth Table

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

(a) Notes 1- 4 apply to the entire Command Truth Table.

(b) Note 5 applies to all Read/Write command.

[BA= Bank address, RA= row Address, CA = Column Address, $\overline{BC}$ = Burst chop, X = Don't care, V = Valid]

Function	Abbreviation	CKE		CS	RAS	CAS	WE	BA0~BA2	A13~A15	A12/ BC	A10/ AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self-Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7, 9, 12
Self-Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7, 8, 9, 12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge All Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power-Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
Power-Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Command Truth Table Notes:

1. All DDR3 SDRAM commands are defined by states of $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. $\overline{\text{RESET}}$ command is enabled when Low, which will be used only for asynchronous reset, so $\overline{\text{RESET}}$ must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS, BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by the MRS.
6. The Power-Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
8. Self-Refresh Exit is asynchronous.
9. VREF (Both VREFDQ and VREFCA) must be maintained during Self-Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read and write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

- (a) Notes 1-7 apply to the entire CKE Truth Table.
 (b) CKE low is allowed only if tMRD and tMOD are satisfied.

Current State	CKE		Command (N) ³ RAS, CAS, WE, CS	Action (N) ³	Notes
	Previous Cycle (N-1)	Current Cycle (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	Deselect or NOP	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	Deselect or NOP	Self-Refresh Exit	8, 12, 16
Bank Activate	H	L	Deselect or NOP	Active Power-Down Entry	11, 13, 14
Reading	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Writing	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	Deselect or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	11, 13, 14, 18
		L	Refresh	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on the previous pages.					10

Notes:

- CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
- COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
- All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
- CKE must be registered with the same value on t_{CKEmin} consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the t_{CKEmin} clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKEmin} + t_{IH}.
- Deselect and NOP are defined in the Command Truth Table.
- On Self-Refresh Exit, Deselect or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
- Self-Refresh mode can only be entered from the All Banks Idle state.
- Must be a legal command as defined in the Command Truth Table.
- Valid commands for Power-Down Entry and Exit are NOP and Deselect only.
- Valid commands for Self-Refresh Exit are NOP and Deselect only.
- Self-Refresh can not be entered during Read or Write operations.
- The Power-Down does not perform any refresh operations.
- "X" means "don't care" (including floating around V_{REF}) in Self-Refresh and Power-Down. It also applies to Address pins.
- V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation.
- If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
- "Idle state" is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-0.4 ~ 1.975	V	1, 3
V_{DDQ}	Voltage on V_{DDQ} relative to V_{SS}	-0.4 ~ 1.975	V	1, 3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V	1
V_{DDSPD}	Voltage on V_{DDSPD} relative to V_{SS}	1.7 ~ 3.6	V	1
T_{STG}	Storage Temperature	-50 to +100	°C	1, 2

Notes:

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.
- V_{DD} and V_{DDQ} must be within 300 mV of each other at all times and V_{REF} must be not greater than $0.6 \cdot V_{DDQ}$. When V_{DD} and V_{DDQ} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

Operating Temperature Range

Symbol	Parameter	Range	Units	Notes
T_{OPER}	Normal Operating Temperature Range (Case)	0 to 85	°C	1, 2
	Extended Operating Temperature Range (Optional)	85 to 95	°C	1, 3

Notes:

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9μs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8μs) in the Extended Temperature Range. Please refer to the SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the SPD for option availability.

Recommended DC Operating Conditions

Symbol	Parameter	Voltage	Rating			Units	Notes
			Min	Typ	Max		
V _{DD}	Supply Voltage	1.35V	1.2825	1.35	1.45	V	1, 2, 3
		1.5V	1.425	1.5	1.575	V	1, 2, 3
V _{DDQ}	Supply Voltage for Output	1.35V	1.2825	1.35	1.45	V	1, 2, 3
		1.5V	1.425	1.5	1.575	V	1, 2, 3
V _{DDSPD}	SPD Supply Voltage		3.0	3.3	3.6	V	
V _{TT}	SPD Supply Voltage		0.7125	0.75	0.7875	V	4
V _{SS}	Ground		0	0	0	V	

Notes:

- Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
- V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
- V_{DD} & V_{DDQ} rating are determined by operation voltage.
- V_{TT} = V_{DDQ}/2

AC and DC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-1066, 1333 & 1600		Units	Notes
		Min	Max		
1.35V					
V _{IH(DC)}	DC input logic high	V _{REF} + 0.90	V _{DD}	V	1
V _{IL(DC)}	DC input logic low	V _{SS}	V _{REF} - 0.90	V	1
V _{IH(AC)}	AC input logic high	V _{REF} + 0.160	-	V	1
V _{IL(AC)}	AC input logic low	-	V _{REF} - 0.160	V	1
1.5V					
V _{IH(DC)}	DC input logic high	V _{REF} + 0.100	V _{DD}	V	1
V _{IL(DC)}	DC input logic low	V _{SS}	V _{REF} - 0.100	V	1
V _{IH(AC)}	AC input logic high	V _{REF} + 0.175	-	V	1
V _{IL(AC)}	AC input logic low	-	V _{REF} - 0.175	V	1

Notes:

- For DQ and DM, V_{REF} = V_{REFDQ}. For input only pins except RESET#, V_{REF} = V_{REFCA}.
- The ac peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF(DC)} by more than ±1% V_{DD} (for reference: approx. ±15mV).
- For reference: approx. V_{DD}/2 ± 15mV.

Differential Swing Requirements for Clock ($\overline{\text{CK}}/\text{CK}$) and Strobe ($\overline{\text{DQS}}/\text{DQS}$)

Symbol	Parameter	DDR3-1066, 1333 & 1600		Units	Notes
		Min	Max		
V_{IHDIFF}	Differential input logic high	0.200	Note 3	V	1
V_{ILDIFF}	Differential input logic high	Note 3	-0.200	V	1
$V_{\text{IHDIFF(AC)}}$	AC input logic high	$2 * (V_{\text{IH(AC)}} - V_{\text{REF}})$	Note 3	V	2
$V_{\text{ILDIFF(AC)}}$	AC input logic low	Note 3	$2 * (V_{\text{REF}} - V_{\text{IL(AC)}})$	V	2

Notes:

- Used to define a differential signal slew-rate.
- For $\text{CK}/\overline{\text{CK}}$, use $V_{\text{IH}}/V_{\text{IL(AC)}}$ of ADD/CMD and V_{REFCA} ; for $\overline{\text{DQS}}/\text{DQS}$, use $V_{\text{IH}}/V_{\text{IL(AC)}}$ of DQs and V_{REFDQ} ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$ need to be within the respective limits ($V_{\text{IH(DC)max}}$, $V_{\text{IL(DC)min}}$) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-ended Input Slew Rate Definition

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{REF}	$V_{\text{IL(AC)min}}$	$\frac{V_{\text{IH(AC)min}} - V_{\text{REF}}}{\Delta \text{TRS}}$	Setup (t_{IS} , t_{DS})
Input slew rate for falling edge	V_{REF}	$V_{\text{IL(AC)max}}$	$\frac{V_{\text{REF}} - V_{\text{IL(AC)max}}}{\Delta \text{TFS}}$	
Input slew rate for rising edge	$V_{\text{IL(DC)max}}$	V_{REF}	$\frac{V_{\text{REF}} - V_{\text{IL(DC)max}}}{\Delta \text{TFH}}$	Hold (t_{IH} , t_{DH})
Input slew rate for falling edge	$V_{\text{IL(DC)min}}$	V_{REF}	$\frac{V_{\text{IH(DC)min}} - V_{\text{REF}}}{\Delta \text{TRH}}$	

Input/Output Capacitance (1.35V)

Speed Bin		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, $\overline{\text{DQS}}$, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	C_{IO}	3	5	TBD	TBD	TBD	TBD	pF	1, 2
Input/output capacitance delta, (DQ, DM, $\overline{\text{DQS}}$, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	C_{DIO}	-1	0.6	TBD	TBD	TBD	TBD	pF	2, 7
Input/output capacitance delta (DQS and $\overline{\text{DQS}}$)	C_{DDQS}	0	0.4	TBD	TBD	TBD	TBD	pF	2, 4
Input capacitance, (CK and $\overline{\text{CK}}$)	C_{CK}	2.0	3.0	TBD	TBD	TBD	TBD	pF	2
Input capacitance delta, (CK and $\overline{\text{CK}}$)	C_{DCK}	-	0.5	TBD	TBD	TBD	TBD	pF	2, 3
Input capacitance, (ADD/CMD/ CTRL input-only pins)	C_{I}	1.5	2.5	TBD	TBD	TBD	TBD	pF	2, 5
Input capacitance delta, (All ADD/CMD/CTRL input-only pins)	C_{DI}	-	0.5	TBD	TBD	TBD	TBD	pF	2, 6

Notes:

- Although the DM, TDQS and $\overline{\text{TDQS}}$ pins have different functions, the loading matches DQ and DQS.
- This parameter is not subject to production test. It is verified by design and characterization.
- Absolute value of $C_{\text{CK}} - C_{\overline{\text{CK}}}$
- Absolute value of $C_{\text{IO}}(\text{DQS}) - C_{\text{IO}}(\overline{\text{DQS}})$
- C_{I} applies to ODT, $\overline{\text{CS}}$, CKE, A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$.
- C_{DI} applies to ODT, $\overline{\text{CS}}$ and CKE, A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$.
- $C_{\text{DIO}} = C_{\text{IO}}(\text{DQ,DM}) - 0.5 * (C_{\text{IO}}(\text{DQS}) + C_{\text{IO}}(\overline{\text{DQS}}))$

Input/Output Capacitance (1.5V)

Speed Bin		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
Parameter	Symbol	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, $\overline{\text{DQS}}$, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	C_{IO}	3	5.4	3	5	TBD	TBD	pF	1, 2
Input/output capacitance delta, (DQ, DM, $\overline{\text{DQS}}$, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	C_{DIO}	-1	0.6	-1	0.6	TBD	TBD	pF	2, 7
Input/output capacitance delta (DQS and $\overline{\text{DQS}}$)	C_{DDQS}	0	0.4	0	0.3	TBD	TBD	pF	2, 4
Input capacitance, (CK and $\overline{\text{CK}}$)	C_{CK}	2.0	3.0	2.0	3.0	TBD	TBD	pF	2
Input capacitance delta, (CK and $\overline{\text{CK}}$)	C_{DCK}	-	0.5	-	0.5	TBD	TBD	pF	2, 3
Input capacitance, (ADD/CMD/ CTRL input-only pins)	C_{I}	1.5	2.5	1.5	2.5	TBD	TBD	pF	2, 5
Input capacitance delta, (All ADD/CMD/CTRL input-only pins)	C_{DI}	-	0.5	-	0.5	TBD	TBD	pF	2, 6

Notes:

- Although the DM, TDQS and $\overline{\text{TDQS}}$ pins have different functions, the loading matches DQ and DQS.
- This parameter is not subject to production test. It is verified by design and characterization.
- Absolute value of $C_{\text{CK}} - C_{\overline{\text{CK}}}$
- Absolute value of $C_{\text{IO}}(\text{DQS}) - C_{\text{IO}}(\overline{\text{DQS}})$
- C_{I} applies to ODT, $\overline{\text{CS}}$, CKE, A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$.
- C_{DI} applies to ODT, $\overline{\text{CS}}$ and CKE, A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$.
- $C_{\text{DIO}} = C_{\text{IO}}(\text{DQ,DM}) - 0.5 * (C_{\text{IO}}(\text{DQS}) + C_{\text{IO}}(\overline{\text{DQS}}))$

IDD and IDDQ Measurement-Loop Patterns Timing

Speed Bin	DDR3-1066	DDR3-1333	Units
Parameter	7-7-7	9-9-9	
$t_{CKmin}(IDD)$	1.875	1.5	ns
CL(IDD)	7	9	nCK
nRCD	7	9	nCK
nRC	27	33	nCK
nRAS	20	24	nCK
nRP	7	9	nCK
nFAW	20	20	nCK
nRRD	6	5	nCK
nRFC	86	107	nCK

Definitions for IDD Measurement Conditions

- “0” and “LOW” is defined as $V_{IN} \leq V_{ILAC(max)}$.
- “1” and “HIGH” is defined as $V_{IN} \geq V_{IHAC(min)}$.
- “MID-LEVEL” is defined as inputs that are $V_{REF} = V_{DD}/2$.
- Timings used for IDD and IDDQ Measurement-Loop Patterns are provided in IDD and IDDQ Timings on page 29.
- Basic IDD and IDDQ Measurement Conditions are described in IDD Measurement Conditions on pages 30-32.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in IDD Measurement-Loop Patterns on pages 33-38.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting:
 - RON = RZQ/7 (34 Ohm in MR1);
 - Qoff = 0_B (Output Buffer enabled in MR1);
 - RTT_Nom = RZQ/6 (40 Ohm in MR1);
 - RTT_Wr = RZQ/2 (120 Ohm in MR2);
 - TDQS Feature disabled in MR1.
- **Attention:** The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define $\underline{D} = \{\underline{CS}, \underline{RAS}, \underline{CAS}, \underline{WE}\} = \{\text{HIGH}, \text{LOW}, \text{LOW}, \text{LOW}\}$
- Define $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{\text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}\}$



IDD Measurement Conditions

Symbol	Description	Conditions
I_{DD0}	Operating One Bank Active-Precharge Current	CKE: High; External clock: On; tCK, nRC, nRAS, CL: See IDD and IDDQ Timings on page 29; BL: 8^1 ; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to IDD0 Measurement-Loop Pattern on page 33; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (See IDD0 Measurement-Loop Pattern on page 33); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD0 Measurement-Loop Pattern on page 33.
I_{DD1}	Operating One Bank Active-Read-Pre-charge Current	CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: See IDD and IDDQ Timings on page 29; BL: $8^1, 6$; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data I/O: partially toggling according to IDD1 Measurement-Loop Pattern on page 34; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (See IDD1 Measurement-Loop Pattern on page 34); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD1 Measurement-Loop Pattern on page 34.
I_{DD2P0}	Precharge Power-Down Current Slow Exit	CKE: Low; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8^1 ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit ³ .
I_{DD2P1}	Precharge Power-Down Current Fast Exit	CKE: Low; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8^1 ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit ³ .
I_{DD2Q}	Precharge Quiet Standby Current	CKE: High; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8^1 ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0.
I_{DD2N}	Precharge Standby Current	CKE: High; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8^1 ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to IDD2N and IDD3N Measurement-Loop Pattern on page 35; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD2N and IDD3N Measurement-Loop Pattern on page 35.

IDD Measurement Conditions (Contd.)

Symbol	Description	Conditions
I _{DD2NT}	Precharge Standby ODT Current	CKE: High; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to IDD2NT Measurement-Loop Pattern on page 35; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: toggling according to IDD2NT Measurement-Loop Pattern on page 35; Pattern Details: See IDD2NT Measurement-Loop Pattern on page 35.
I _{DD3P}	Active Power Down Current	CKE: Low; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0.
I _{DD3N}	Active Standby Current	CKE: High; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to IDD2N and IDD3N Measurement-Loop Pattern on page 35; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD2N and IDD3N Measurement-Loop Pattern on page 35.
I _{DD4R}	Operating Burst Read Current	CKE: High; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8 ^{1, 6} ; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to IDD4R Measurement-Loop Pattern on page 36; Data I/O: seamless read data burst with different data between one burst and the next one according to IDD4R Measurement-Loop Pattern on page 36; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (See IDD4R Measurement-Loop Pattern on page 36); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD4R Measurement-Loop Pattern on page 36.
I _{DD4W}	Operating Burst Write Current	CKE: High; External clock: On; tCK, CL: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to IDD4W Measurement-Loop Pattern on page 36; Data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern on page 36; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (See IDD4W Measurement-Loop Pattern on page 36); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at HIGH; Pattern Details: See IDD4W Measurement-Loop Pattern on page 36.

IDD Measurement Conditions (Contd.)

Symbol	Description	Conditions
I _{DD5B}	Burst Refresh Current	CKE: High; External clock: On; tCK, CL, nRFC: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to IDD5B Measurement-Loop Pattern on page 37; Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: REF command every nRFC (See IDD5B Measurement-Loop Pattern on page 37); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD5B Measurement-Loop Pattern on page 37.
I _{DD6}	Self-Refresh Current: Normal Temperature Range	T _{CASE} : 0 - 85°C; Auto Self-Refresh (ASR): Disabled ⁴ ; Self-Refresh Temperature Range (SRT): Normal ⁵ ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$, Command, Address, Bank Address, Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL.
I _{DD6ET}	Self-Refresh Current: Extended Temperature Range	T _{CASE} : 85 - 95°C; Auto Self-Refresh (ASR): Disabled ⁴ ; Self-Refresh Temperature Range (SRT): Extended ⁵ ; CKE: Low; External clock: Off; CK and CK#: LOW; CL: See IDD and IDDQ Timings on page 29; BL: 8 ¹ ; AL: 0; $\overline{CS}$, Command, Address, Bank Address, Data I/O: MID-LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL.
I _{DD7}	All Bank Interleave Read Current	CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: See IDD and IDDQ Timings on page 29; BL: 8 ^{1, 6} ; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to IDD7 Measurement-Loop Pattern on page 37; Data I/O: read data bursts with different data between one burst and the next one according to IDD7 Measurement-Loop Pattern on page 37; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, See IDD7 Measurement-Loop Pattern on page 37; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: See IDD7 Measurement-Loop Pattern on page 37.

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B.
2. Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B.
3. Precharge Power Down Mode: set MR0 A[12] = 0B for Slow Exit or MR0 A[12]=1B for Fast Exit.
4. Auto Self-Refresh (ASR): set MR2 A[6] = 0B to disable or 1B to enable feature.
5. Self-Refresh Temperature Range (SRT): set MR2 A[7] = 0B for normal or 1B for extended temperature range.
6. Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B.

IDD Measurement Conditions (Contd.)

IDD0 Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if necessary												
			1*nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRAS - 1. Truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if necessary												
		1	2*nRC	Repeat Sub-Loop 0, but BA[2:0] = 1												
		2	4*nRC	Repeat Sub-Loop 0, but BA[2:0] = 2												
		3	6*nRC	Repeat Sub-Loop 0, but BA[2:0] = 3												
		4	8*nRC	Repeat Sub-Loop 0, but BA[2:0] = 4												
		5	10*nRC	Repeat Sub-Loop 0, but BA[2:0] = 5												
		6	12*nRC	Repeat Sub-Loop 0, but BA[2:0] = 6												
		7	14*nRC	Repeat Sub-Loop 0, but BA[2:0] = 7												

Notes:

- DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD Measurement Conditions (Contd.)

IDD1 Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1-2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3-4	D, D	1	1	1	1	0	0	00	0	0	0	0	-
			...	Repeat pattern 1-4 until nRCD - 1. Truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if necessary												
			1*nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1-2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3-4	D, D	1	1	1	1	0	0	00	0	0	F	0	-
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRCD - 1. Truncate if necessary												
			1*nRC + nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRAS - 1. Truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if necessary												
		1	2*nRC	Repeat Sub-Loop 0, but BA[2:0] = 1												
		2	4*nRC	Repeat Sub-Loop 0, but BA[2:0] = 2												
		3	6*nRC	Repeat Sub-Loop 0, but BA[2:0] = 3												
		4	8*nRC	Repeat Sub-Loop 0, but BA[2:0] = 4												
		5	10*nRC	Repeat Sub-Loop 0, but BA[2:0] = 5												
		6	12*nRC	Repeat Sub-Loop 0, but BA[2:0] = 6												
		7	14*nRC	Repeat Sub-Loop 0, but BA[2:0] = 7												

Notes:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Measurement Conditions (Contd.)

IDD2N and IDD3N Measurement-Loop Pattern

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	D	1	1	1	1	0	0	00	0	0	F	0	-
			3	D	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	Repeat Sub-Loop 0, but BA[2:0] = 1												
		2	8-11	Repeat Sub-Loop 0, but BA[2:0] = 2												
		3	12-15	Repeat Sub-Loop 0, but BA[2:0] = 3												
		4	16-19	Repeat Sub-Loop 0, but BA[2:0] = 4												
		5	20-23	Repeat Sub-Loop 0, but BA[2:0] = 5												
		6	24-27	Repeat Sub-Loop 0, but BA[2:0] = 6												
		7	28-31	Repeat Sub-Loop 0, but BA[2:0] = 7												

IDD2NT Measurement-Loop Pattern

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	D	1	1	1	1	0	0	00	0	0	F	0	-
			3	D	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	Repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	Repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	Repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	Repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	Repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-27	Repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	Repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

Notes:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD Measurement Conditions (Contd.)

IDD4R Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2-3	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6-7	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	Repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	Repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	Repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	Repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	Repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	Repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	Repeat Sub-Loop 0, but BA[2:0] = 7												

IDD4W Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2-3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6-7	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	Repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	Repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	Repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	Repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	Repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	Repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	Repeat Sub-Loop 0, but BA[2:0] = 7												

Notes:

- DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

IDD Measurement Conditions (Contd.)

IDD5B Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	REF	0	0	0	1	0	0	00	0	0	0	0	-
		1	1-2	D	1	0	0	0	0	0	00	0	0	0	0	-
			3-4	D	1	1	1	1	0	0	00	0	0	F	0	-
			5-8	Repeat cycles 1-4, but BA[2:0] = 1												
			9-12	Repeat cycles 1-4, but BA[2:0] = 2												
			13-16	Repeat cycles 1-4, but BA[2:0] = 3												
			17-20	Repeat cycles 1-4, but BA[2:0] = 4												
			21-24	Repeat cycles 1-4, but BA[2:0] = 5												
			25-28	Repeat cycles 1-4, but BA[2:0] = 6												
			29-32	Repeat cycles 1-4, but BA[2:0] = 7												
		2	33-nRFC - 1	Repeat Sub-Loop 1 until nRFC - 1. Truncate if necessary												

IDD7 Measurement-Loop Pattern¹

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	Repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	Repeat above D Command until 2*nRRD - 1												
		2	2*nRRD	Repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	Repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												

IDD Measurement Conditions (Contd.)

IDD7 Measurement-Loop Pattern (Contd.)¹

ATTENTION: Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²
		5	nFAW	Repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW + 2*nRRD	Repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW + 3*nRRD	Repeat Sub-Loop 1, but BA[2:0] = 7												
toggling	Static High	9	nFAW + 4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2*nFAW - 1, if necessary												
		10	2*nFAW	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW + 1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2*nFAW + 2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2*nFAW + nRRD - 1												
		11	2*nFAW + nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW + nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW + nRRD + 2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2*nFAW + 2*nRRD - 1												
		12	2*nFAW + 2*nRRD	Repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW + 3*nRRD	Repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW + 4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3*nFAW - 1, if necessary												
		15	3*nFAW	Repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW + nRRD	Repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW + 2*nRRD	Repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW + 3*nRRD	Repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW + 4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4*nFAW - 1, if necessary												

Notes:

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to RD Commands, otherwise MID-LEVEL
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications

Speed Bin	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
	7-7-7		9-9-9		11-11-11			
Parameter	1.35V	1.5V	1.35V	1.5V	1.35V	1.5V		
I _{DD0}	1775	1820	1883	1955	TBD	2045	mA	
I _{DD1}	1955	2000	2018	2090	TBD	2135	mA	
I _{DD2P0}	866	866	866	866	TBD	866	mA	
I _{DD2P1}	1100	1190	1190	1280	TBD	1280	mA	
I _{DD2Q}	1370	1460	1442	1550	TBD	1370	mA	
I _{DD2N}	1370	1460	1442	1550	TBD	1406	mA	
I _{DD2NT}	1406	1550	1460	1640	TBD	1550	mA	
I _{DD3P}	1370	1460	1433	1505	TBD	1550	mA	
I _{DD3N}	1550	1640	1586	1730	TBD	1730	mA	
I _{DD4R}	2369	2405	2558	2630	TBD	2810	mA	
I _{DD4W}	2405	2450	2603	2675	TBD	2855	mA	
I _{DD5B}	2990	3035	3008	3080	TBD	3125	mA	
I _{DD6}	231	231	231	231	TBD	231	mA	
I _{DD6ET}	285	285	285	285	TBD	285	mA	
I _{DD7}	4115	4160	4583	4655	TBD	5105	mA	

Refresh Parameters

Parameter		Symbol	2Gb	Units
REF command to ACT or REF command time		t _{RFC}	160	ns
Average periodic refresh interval	0 °C ≤ T _{CASE} ≤ 85 °C	t _{REFI}	7.8	μs
	85 °C ≤ T _{CASE} ≤ 95 °C		3.9	μs

Device Standard Speed Bins

DDR3-1066 Speed Bins

Speed Bin			DDR3-1066		Units	Notes
CL - nRCD - nRP			7-7-7			
Parameter	Symbol	Min	Max			
Internal read command to first data	t _{AA}	13.125	20		ns	
ACT to internal read or write delay time	t _{RCD}	13.125	-		ns	
Pre command period	t _{RP}	13.125	-		ns	
ACT to ACT or REF command period	t _{RC}	50.625	-		ns	
ACT to PRE command period	t _{RAS}	37.5	9 * t _{REFI}		ns	
CL = 5	CWL = 5	t _{CK} (avg)	3.0	3.3	ns	1, 2, 3, 5, 8
	CWL = 6	t _{CK} (avg)	Reserved		ns	4
CL = 6	CWL = 5	t _{CK} (avg)	2.5	3.3	ns	1, 2, 3, 5
	CWL = 6	t _{CK} (avg)	Reserved		ns	4
CL = 7	CWL = 5	t _{CK} (avg)	Reserved		ns	4
	CWL = 6	t _{CK} (avg)	1.875	< 2.5	ns	1, 2, 3
CL = 8	CWL = 5	t _{CK} (avg)	Reserved		ns	4
	CWL = 6	t _{CK} (avg)	1.875	< 2.5	ns	1, 2, 3
Supported CL Settings		5, 6, 7, 8			n _{CK}	
Supported CWL Settings		5, 6			n _{CK}	

Device Standard Speed Bins (Contd.)

DDR3-1333 Speed Bins

Speed Bin		DDR3-1333		Units	Notes	
CL - nRCD - nRP		9-9-9				
Parameter	Symbol	Min	Max			
Internal read command to first data	t _{AA}	13.125	20	ns		
ACT to internal read or write delay time	t _{RCD}	13.125	-	ns		
Pre command period	t _{RP}	13.125	-	ns		
ACT to ACT or REF command period	t _{RC}	49.125	-	ns		
ACT to PRE command period	t _{RAS}	36	9 * t _{REFI}	ns		
CL = 5	CWL = 5	t _{CK} (avg)	3.0	3.3	ns	1, 2, 3, 6, 8
	CWL = 6, 7		Reserved		ns	4
CL = 6	CWL = 5	t _{CK} (avg)	2.5	3.3	ns	1, 2, 3, 6
	CWL = 6, 7		Reserved		ns	4
CL = 7	CWL = 5	t _{CK} (avg)	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 6
	CWL = 7		Reserved		ns	4
CL = 8	CWL = 5	t _{CK} (avg)	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 6
	CWL = 7		Reserved		ns	4
CL = 9	CWL = 5, 6	t _{CK} (avg)	Reserved		ns	4
	CWL = 7		1.5	< 1.875	ns	1, 2, 3
Supported CL Settings		5, 6, 7, 8, 9		n _{CK}		
Supported CWL Settings		5, 6, 7		n _{CK}		

Device Standard Speed Bins (Contd.)

DDR3-1600 Speed Bins

Speed Bin			DDR3-1600		Units	Notes
CL - nRCD - nRP			11-11-11			
Parameter		Symbol	Min	Max		
Internal read command to first data		t _{AA}	13.125	20	ns	
ACT to internal read or write delay time		t _{RCD}	13.125	-	ns	
Pre command period		t _{RP}	13.125	-	ns	
ACT to ACT or REF command period		t _{RC}	48.125	-	ns	
ACT to PRE command period		t _{RAS}	35	9 * t _{REFI}	ns	
CL = 5	CWL = 5	t _{CK} (avg)	3.0	3.3	ns	1, 2, 3, 7, 8
	CWL = 6, 7, 8		Reserved		ns	4
CL = 6	CWL = 5	t _{CK} (avg)	2.5	3.3	ns	1, 2, 3, 7
	CWL = 6, 7, 8		Reserved		ns	4
CL = 7	CWL = 5	t _{CK} (avg)	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7, 8		Reserved		ns	4
CL = 8	CWL = 5	t _{CK} (avg)	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7, 8		Reserved		ns	4
CL = 9	CWL = 5, 6	t _{CK} (avg)	Reserved		ns	4
	CWL = 7		1.5	< 1.875	ns	1, 2, 3, 7
	CWL = 8		Reserved		ns	4
CL = 10	CWL = 5, 6	t _{CK} (avg)	Reserved		ns	4
	CWL = 7		1.5	< 1.875	ns	1, 2, 3, 7
	CWL = 8		Reserved		ns	4
CL = 11	CWL = 5, 6, 7	t _{CK} (avg)	Reserved		ns	4
	CWL = 8		1.25	< 1.5	ns	1, 2, 3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11		n _{CK}	
Supported CWL Settings			5, 6, 7, 8		n _{CK}	

Speed Bin Tables Notes

1. The CL setting and CWL setting result in $t_{CK(AVG)}min$ and $t_{CK(AVG)}max$ requirements. When making a selection of $t_{CK(AVG)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(AVG)}min$ limits: Since $\overline{CAS}$ Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{CK(AVG)}$ value (2.5, 1.875, or 1.5) when calculating $CL [nCK] = t_{AA} [ns] / t_{CK(AVG)} [ns]$, rounding up to the next 'Supported CL'.
3. $t_{CK(AVG)}max$ limits: Calculate $t_{CK(AVG)} = t_{AA}max / CL \text{ SELECTED}$ and round the resulting $t_{CK(AVG)}$ down to the next valid speed bin (i.e. 3.3ns, 2.5ns, or 1.875 ns). This result is $t_{CK(AVG)}max$ corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. DDR3-800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.

Device Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum clock cycle time (DLL off mode)	t _{CK(DLL_OF F)}	8	-	8	-	8	-	t _{CK}	6
Average clock period	t _{CK(avg)}	Refer to Speed Bin on pages 40-42.						ps	
Average high pulse width	t _{CH(avg)}	0.47	0.53	0.47	0.53	0.47	0.53	t _{CK(avg)}	
Average low pulse width	t _{CL(avg)}	0.47	0.53	0.47	0.53	0.47	0.53	t _{CK(avg)}	
Absolute clock period	t _{CK(abs)}	t _{CK(avg)} min +t _{JIT} (per)min	t _{CK(avg)} max +t _{JIT} (per)max	t _{CK(avg)} min +t _{JIT} (per)min	t _{CK(avg)} max +t _{JIT} (per)max	t _{CK(avg)} min +t _{JIT} (per)min	t _{CK(avg)} max +t _{JIT} (per)max	ps	
Absolute clock high pulse width	t _{CH(abs)}	0.43	-	0.43	-	0.43	-	t _{CK(avg)}	25
Absolute clock low pulse width	t _{CL(abs)}	0.43	-	0.43	-	0.43	-	t _{CK(avg)}	26
Clock period jitter	t _{JIT(per)}	-90	90	-80	80	-70	70	ps	
Clock period jitter during DLL locking period	t _{JIT(per, lck)}	-80	80	-70	70	-60	60	ps	
Cycle to cycle period jitter	t _{JIT(CC)}	180		160		140		ps	
Cycle to cycle period jitter during DLL locking period	t _{JIT(CC, lck)}	160		140		120		ps	
Duty cycle jitter	t _{JIT(duty)}	-	-	-	-	-	-	ps	
Cumulative error across 2 cycles	t _{ERR(2per)}	-132	132	-118	118	-103	103	ps	
Cumulative error across 3 cycles	t _{ERR(3per)}	-157	157	-140	140	-122	122	ps	
Cumulative error across 4 cycles	t _{ERR(4per)}	-175	175	-155	155	-136	136	ps	
Cumulative error across 5 cycles	t _{ERR(5per)}	-188	188	-168	168	-147	147	ps	
Cumulative error across 6 cycles	t _{ERR(6per)}	-200	200	-177	177	-155	155	ps	
Cumulative error across 7 cycles	t _{ERR(7per)}	-209	209	-186	186	-163	163	ps	
Cumulative error across 8 cycles	t _{ERR(8per)}	-217	217	-193	193	-169	169	ps	
Cumulative error across 9 cycles	t _{ERR(9per)}	-224	224	-200	200	-175	175	ps	
Cumulative error across 10 cycles	t _{ERR(10per)}	-231	231	-205	205	-180	180	ps	
Cumulative error across 11 cycles	t _{ERR(11per)}	-237	237	-210	210	-184	184	ps	
Cumulative error across 12 cycles	t _{ERR(12per)}	-242	242	-215	215	-188	188	ps	
Cumulative error across n = 13-50 cycles	t _{ERR(nper)}	t _{ERR(nper)min} = (1 + 0.68ln(n)) * t _{JIT(per)min} t _{ERR(nper)max} = (1 + 0.68ln(n)) * t _{JIT(per)max}						ps	24

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data Timing									
DQS, $\overline{DQS}$ to DQ skew, per group, per access	t _{DQSQ}	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, $\overline{DQS}$	t _{QH}	0.38	-	0.38	-	0.38	-	t _{CK(} avg)ps	13, b
DQ low-impedance from CK, $\overline{CK}$	t _{LZ(DQ)}	-600	300	-500	250	-450	225	ps	13, 14, a
DQ high-impedance from CK, $\overline{CK}$	t _{HZ(DQ)}	-	300	-	250	-	225	ps	13, 14, a
Data setup time to DQS, $\overline{DQS}$ referenced to V _{IH(AC)} / V _{IL(AC)} levels	t _{DS(base)} AC175	25	-	-	-	-	-	ps	17, d
Data setup time to DQS, $\overline{DQS}$ referenced to V _{IH(AC)} / V _{IL(AC)} levels	t _{DS(base)} AC150	75	-	30	-	10	-	ps	17, d
Data hold time from DQS, $\overline{DQS}$ referenced to V _{IH(DC)} / V _{IL(DC)} levels	t _{DH(base)} DC100	100	-	65	-	45	-	ps	17, d
DQ and DM input pulse width for each input	t _{DIPW}	490	-	400	-	360	-	ps	28
Data Strobe Timing									
DQS, $\overline{DQS}$ differential READ preamble	t _{RPRE}	0.9	Note 19	0.9	Note 19	0.9	Note 19	t _{CK(} avg)ps	13, 19, b
DQS, $\overline{DQS}$ differential READ postamble	t _{RPST}	0.3	Note 11	0.3	Note 11	0.3	Note 11	t _{CK(} avg)ps	11, 13, b
DQS, $\overline{DQS}$ differential output high time	t _{QSH}	0.38	-	0.4	-	0.4	-	t _{CK(} avg)ps	13, b
DQS, $\overline{DQS}$ differential output low time	t _{QSL}	0.38	-	0.4	-	0.4	-	t _{CK(} avg)ps	13, b
DQS, $\overline{DQS}$ differential WRITE preamble	t _{WPRE}	0.9	-	0.9	-	0.9	-	t _{CK(} avg)ps	
DQS, $\overline{DQS}$ differential WRITE postamble	t _{WPST}	0.3	-	0.3	-	0.3	-	t _{CK(} avg)ps	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t _{DQSCK}	-300	300	-255	255	-225	225	ps	13, a
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL - 1)	t _{LZ(DQS)}	-600	300	-500	250	-450	225	ps	13, 14, a
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL + BL / 2)	t _{HZ(DQS)}	-	300	-	250	-	225	ps	13, 14, a
DQS, $\overline{DQS}$ differential input low pulse width	t _{DQSL}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK(} avg)ps	
DQS, $\overline{DQS}$ differential input high pulse width	t _{DQSH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK(} avg)ps	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	t _{DQSS}	-0.25	0.25	-0.25	0.25	-0.27	0.27	t _{CK(} avg)ps	c
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	t _{DSS}	0.2	-	0.2	-	0.18	-	t _{CK(} avg)ps	c
DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	t _{DSH}	0.2	-	0.2	-	0.18	-	t _{CK(} avg)ps	c

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
Command and Address Timing									
DLL locking time	t _{DLLK}	512	-	512	-	512	-	nCK	
Internal READ command to PRE-CHARGE command delay	t _{RTP}	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal READ command	t _{WTR}	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		18, e
WRITE recovery time	t _{WR}	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	t _{MRD}	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	t _{MOD}	max (12nCK, 15ns)	-	max (12nCK, 15ns)	-	max (12nCK, 15ns)	-		
ACT to internal read or write delay time	t _{RCD}	Refer to Speed Bin on pages 40-42.							e
PRECHARGE command period	t _{RP}	Refer to Speed Bin on pages 40-42.							e
ACT to ACT or REF command period	t _{RC}	Refer to Speed Bin on pages 40-42.							e
CAS to CAS command delay	t _{CCD}	4	-	4	-	4	-	nCK	
Auto-precharge write recovery + pre-charge time	t _{DAL(min)}	WR + roundup (t _{RP} / t _{CK(avg)})						nCK	
Multi-purpose register recovery time	t _{MPRR}	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	t _{RAS}	Refer to Speed Bin on pages 40-42.							e
ACTIVE to ACTIVE command period for 1KB page size	t _{RRD}	max (4nCK, 7.5ns)	-	max (4nCK, 6ns)	-	max (4nCK, 6ns)	-		e
Four activate window for 1KB page size	t _{FAW}	37.5	-	30	-	30	-	ns	e
Command and Address setup time to CK, CK referenced to V _{IH(AC)} / V _{IL(AC)} levels	t _{IS(base) AC175}	125	-	65	-	45	-	ps	16, b
Command and Address setup time to CK, CK referenced to V _{IH(AC)} / V _{IL(AC)} levels	t _{IS(base) AC150}	275	-	190	-	170	-	ps	16, 27, b
Command and Address hold time to CK, CK referenced to V _{IH(DC)} / V _{IL(DC)} levels	t _{IH(base) DC100}	200	-	140	-	120	-	ps	16, b
Control and address input pulse width for each input	t _{IPW}	780	-	620	-	560	-	ps	28

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
Calibration Timing									
Power-up and RESET calibration time	t _{ZQinit}	max (512nCK, 640ns)	-	max (512nCK, 640ns)	-	max (512nCK, 640ns)	-		
Normal operation Full calibration time	t _{ZQoper}	max (256nCK, 320ns)	-	max (256nCK, 320ns)	-	max (256nCK, 320ns)	-		
Normal operation Short calibration time	t _{ZQCS}	max (64nCK, 80ns)	-	max (64nCK, 80ns)	-	max (64nCK, 80ns)	-		23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	t _{XPR}	max (5nCK, t _{RFC} min + 10ns)	-	max (5nCK, t _{RFC} min + 10ns)	-	max (5nCK, t _{RFC} min + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh from to commands not requiring a locked DLL	t _{XS}	max (5nCK, t _{RFC} min + 10ns)	-	max (5nCK, t _{RFC} min + 10ns)	-	max (5nCK, t _{RFC} min + 10ns)	-		
Exit Self Refresh from to commands requiring a locked DLL	t _{XSDLL}	t _{DLLK} min	-	t _{DLLK} min	-	t _{DLLK} min	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing	t _{CKESR}	t _{CKE} min + 1nCK	-	t _{CKE} min + 1nCK	-	t _{CKE} min + 1nCK	-		
Valid clock requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t _{CKSRE}	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-		
Valid clock requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t _{CKSRX}	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t _{XP}	max (3nCK, 7.5ns)	-	max (3nCK, 6ns)	-	max (3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t _{XPDLL}	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
CKE minimum pulse width	t _{CKE}	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5ns)	-	nCK	

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
Command pass disable delay	t_{CPDED}	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKEmin}	$9 * t_{REFI}$	t_{CKEmin}	$9 * t_{REFI}$	t_{CKEmin}	$9 * t_{REFI}$		15
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	$RL + 4 + 1$	-	$RL + 4 + 1$	-	$RL + 4 + 1$	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	$WL + 4 + (t_{WR} / t_{CK(avg)})$	-	$WL + 4 + (t_{WR} / t_{CK(avg)})$	-	$WL + 4 + (t_{WR} / t_{CK(avg)})$	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	$WL + 4 + WR + 1$	-	$WL + 4 + WR + 1$	-	$WL + 4 + WR + 1$	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	t_{WRPDEN}	$WL + 2 + (t_{WR} / t_{CK(avg)})$	-	$WL + 2 + (t_{WR} / t_{CK(avg)})$	-	$WL + 2 + (t_{WR} / t_{CK(avg)})$	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPDEN}$	$WL + 2 + WR + 1$	-	$WL + 2 + WR + 1$	-	$WL + 2 + WR + 1$	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	1	-	nCK	20, 21
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MODmin}	-	t_{MODmin}	-	t_{MODmin}	-		
ODT Timing									
ODT turn on latency	$ODTLon$	$WL - 2 = CWL + AL - 2$						nCK	
ODT turn off latency	$ODTLoFF$	$WL - 2 = CWL + AL - 2$						nCK	
ODT high time without Write command or with Write command and BC4	$ODTH4$	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	$ODTH8$	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONPD}	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFPD}	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	t_{AON}	-300	300	-250	250	-225	225	ps	7, a
RTT_Nom and RTT_WR turn-off time from ODTLoFF reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	8, a
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	a

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write Leveling Timing									
First DQS/DQS rising edge after write leveling mode is programmed	t _{WLMRD}	40	-	40	-	40	-	nCK	3
DQS/DQS delay after write leveling mode is programmed	t _{WLDQSEN}	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	t _{WLS}	245	-	195	-	165	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t _{WLH}	245	-	195	-	16	-	ps	
Write leveling output delay	t _{WLO}	0	9	0	9	0	7.5	ns	
Write leveling output error	t _{WLOE}	0	2	0	2	0	2	ns	

Device Timing Parameters Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in the Mode Register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI} .
7. Minimum RTT turn-on time (t_{AONmin}) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AONmax}) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.
8. Minimum RTT turn-off time (t_{AOFmin}) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (t_{AOFmax}) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR} / t_{CK} to the next integer.
10. WR is in clock cycles as programmed in MR0.
11. The maximum postamble is bound by $t_{HZDQS(max)}$.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. t_{REFI} depends on T_{OPER} .
16. $t_{IS(base)}$ and $t_{IH(base)}$ values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate. Note for DQ and DM signals, $V_{REF(DC)} = V_{REFDQ(DC)}$. For input only pins except $\overline{RESET}$, $V_{REF(DC)} = V_{REFCA(DC)}$.
17. $t_{DS(base)}$ and $t_{DH(base)}$ values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, $V_{REF(DC)} = V_{REFDQ(DC)}$. For input only pins except $\overline{RESET}$, $V_{REF(DC)} = V_{REFCA(DC)}$.
18. Start of internal write transaction is defined as follows:
 For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by $t_{LZDQS(min)}$.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN(min)}$ is satisfied, there are cases where additional time such as $t_{XPDL(min)}$ is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
 One method for calculating the interval between ZQCS commands, given the temperature ($T_{driftrate}$) and voltage ($V_{driftrate}$) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times T_{driftrate}) + (VSens \times V_{driftrate})}$$

where $TSens = \max(dRTTdT, dRONdTM)$ and $VSens = \max(dRTTdV, dRONdVM)$ define the SDRAM temperature and voltage sensitivities.

For example, if $TSens = 1.5\% / ^\circ C$, $VSens = 0.15\% / mV$, $T_{driftrate} = 1 ^\circ C / sec$ and $V_{driftrate} = 15 mV / sec$, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 + 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The $t_{IS(base)}$ AC150 specifications are adjusted from the $t_{IS(base)}$ specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point $[(175 mV - 150 mV) / 1 V/ns]$.
28. Pulse width of a input signal is defined as the width between the first crossing of V_{REFDC} and the consecutive crossing of V_{REFDC} .

Jitter Notes

- a When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(mper)act}$ of the input clock, where $2 \leq m \leq 12$. (Output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has $t_{ERR(mper)act,min} = -172$ ps and $t_{ERR(mper)act,max} = +193$ ps, then $t_{DQSCkmin}(derated) = t_{DQSCkmin} - t_{ERR(mper)act,max} = -400$ ps - 193 ps = -593 ps and $t_{DQSCkmax}(derated) = t_{DQSCkmax} - t_{ERR(mper)act,min} = 400$ ps + 172 ps = +572 ps. Similarly, $t_{LZ(DQ)}$ for DDR3-800 derates to $t_{LZ(DQ)min}(derated) = -800$ ps - 193 ps = -993 ps and $t_{LZ(DQ)max}(derated) = 400$ ps + 172 ps = +572 ps. (Caution on the min/max usage!)

Note that $t_{ERR(mper)act,min}$ is the minimum measured value of $t_{ERR(nper)}$ where $2 \leq n \leq 12$, and $t_{ERR(mper)act,max}$ is the maximum measured value of $t_{ERR(nper)}$ where $2 \leq n \leq 12$.

- b When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)act}$ of the input clock. (Output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has $t_{CK(avg)act} = 2500$ ps, $t_{JIT(per)act,min} = -72$ ps and $t_{JIT(per)act,max} = +93$ ps, then $t_{RPREmin}(derated) = t_{RPREmin} + t_{JIT(per)act,min} = 0.9 \times t_{CK(avg)act} + t_{JIT(per)act,min} = 0.9 \times 2500$ ps - 72 ps = +2178 ps. Similarly, $t_{QHmin}(derated) = t_{QHmin} + t_{JIT(per)act,min} = 0.38 \times t_{CK(avg)act} + t_{JIT(per)act,min} = 0.38 \times 2500$ ps - 72 ps = +878 ps. (Caution on the min/max usage!)

- c These parameters are measured from a data strobe signal ($DQS, \overline{DQS}$) crossing to its respective clock signal ($CK, \overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, $t_{JIT(cc)}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- d These parameters are measured from a data signal ($DM, DQ0, DQ1$, etc.) transition edge to its respective data strobe signal ($DQS, \overline{DQS}$) crossing.
- e For these parameters, the DDR3 SDRAM device supports $t_{nPARAM} [nCK] = RU\{t_{PARAM} [ns] / t_{CK(avg)} [ns]\}$, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP} = RU\{t_{RP} / t_{CK(avg)}\}$, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which $t_{RP} = 15$ ns, the device will support $t_{nRP} = RU\{t_{RP} / t_{CK(avg)}\} = 6$, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at $Tm+6$ is valid even if $(Tm+6 - Tm)$ is less than 15 ns due to input clock jitter.

Part Number Decode

<u>S</u>	<u>G</u>	<u>5</u>	<u>72</u>	<u>12</u>	<u>8</u>	<u>F</u>	<u>U</u>	<u>8</u>	<u>P</u>	<u>0</u>	<u>U</u>	<u>U</u>
1	2	3	4	5	6	7	8	9	10	11	12	13

- | | |
|--|--|
| <p>1 SMART Modular Technologies</p> <p>2 Module Process Technology
G: Green Module (RoHS Compliant)</p> <p>3 Product Category
5: SDRAM DIMM with Standard Testing</p> <p>4 Module Data Bus Width
72: x72</p> <p>5 Module Address Depth
12: 512M</p> <p>6 Device Data Width
8: x8</p> <p>7 Special Device Feature
F: Standard FBGA (8 Bank SDRAM)</p> <p>8 Technology/Voltage
H: DDR3 SDRAM/1.5V
J: DDR3 SDRAM/1.35V</p> <p>9 Refresh/Power
8: 8K Refresh/Standard Power</p> <p>10 Module Configuration
P: 240-pin DIMM Registered, Parity</p> <p>11 Device Physicals
0: 2Gbit Device Based</p> <p>12 CAS Latencies Supported
L: 5, 6, 7, 8
P: 5, 6, 7, 8, 9
R: 5, 6, 7, 8, 9, 10, 11</p> | <p>13 Cycle Time (Clock Speed)
C: 1.875ns (533MHz, PC3-8500, DDR3-1066-7-7-7)
H: 1.5ns (667MHz, PC3-10600, DDR3-1333-9-9-9)
N: 1.25ns (800MHz, PC3-12800, DDR3-1600-11-11-11)</p> |
|--|--|

Note: "U" in the part number should be replaced by user specified option.

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