

Ordering Information		
Part Numbers	Description	Module Speed
SG572288FH8DWKA1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-800-555, 25.40mm, Green Module (RoHS Compliant).	PC3-6400 @ CL 5, 6
SG572288FH8DW6B1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-800-666, 25.40mm, Green Module (RoHS Compliant).	PC3-6400 @ CL 6
SG572288FH8DWRE1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-1066-666, 25.40mm, Green Module (RoHS Compliant).	PC3-8500 @ CL 6, 7, 8
SG572288FH8DWLC1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-1066-777, 25.40mm, Green Module (RoHS Compliant).	PC3-8500 @ CL 7, 8
SG572288FH8DWMD1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-1066-888, 25.40mm, Green Module (RoHS Compliant).	PC3-8500 @ CL 8
SG572288FH8DWNG1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-1333-888, 25.40mm, Green Module (RoHS Compliant).	PC3-10600 @ CL 8, 9
SG572288FH8DWPH1	128Mx72 (1GB), DDR3, 204-pin Unbuffered SO-UDIMM, ECC, 128Mx8 Based, DDR3-1333-999, 25.40mm, Green Module (RoHS Compliant).	PC3-10600 @ CL 9

Note:

Part numbers above in black are the recommended part numbers. Part numbers in gray are available if required.

(All specifications of this module are subject to change without notice.)



Revision History

- **June 26, 2009**
Corrected pin 83 to CB3 in the Pin List on page 5.
- **March 26, 2009**
Datasheet released.



**1GByte (128Mx72) DDR3 SDRAM Module - 128Mx8 Based
204-pin SO-UDIMM, Unbuffered, ECC**

Features

- Standard = JEDEC
- Configuration = ECC
- Number of Module Ranks = 1
- Number of Devices = 9
- $V_{DD} = V_{DDQ} = 1.5V$
- $V_{DDSPD} = 1.7V$ to 3.6V
- Cycle Time = 2.5ns (PC3-6400)
1.875ns (PC3-8500)
1.5ns (PC3-10600)
- \overline{CAS} Latency = 5, 6, 7, 8, and 9
- Additive Latency = 0, CL-1, and CL-2
- \overline{CAS} Write Latency (CWL) = 5, 6, 7, 8
- Burst Length = BC4, BL8, BC4 or BL8 (on the fly)
- Burst Length = Nibble Sequential & Interleave Mode
- Internal Banks per SDRAM = 8
- Refresh = 8K/64ms
- Device Package = FBGA
- Lead Finish = Gold
- Length x Height = 133.35mm x 25.40mm
- No. of sides = Double-sided
- Mating Connector (Examples)
Horizontal = Foxconn - AS0A626-UASN-7F
- On chip DLL align DQ, DQS and \overline{DQS} transition with CK transition
- DM write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs latched on the rising edges of the clock
- Dynamic On Die Termination supported
- Driver strength selected by EMRS
- Asynchronous RESET pin supported
- Write Levelization supported
- 8-bit pre-fetch

Addressing

Device Configuration	128Mx8
Number of Internal Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BC switch on the fly	A12/BC
Row Address	A0 - A13
Column Address	A0 - A9

Pin Description Table

Symbol	Type	Polarity	Function
$\overline{CK0} \sim \overline{CK1}$, $CK0 \sim CK1$	SSTL_15	Differential Crossing	CK and \overline{CK} are differential clock inputs. All the DDR3 SDRAM address/control inputs are sampled on the crossing of the positive edge of CK and the negative edge of \overline{CK} . Output (read) data is referenced to the crossing of CK and \overline{CK} (Both directions of crossing).
CKE0	SSTL_15	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$	SSTL_15	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
ODT0	SSTL_15	Active High	When high, termination resistance is enabled for all DQ, DQS, \overline{DQS} and DM pins, assuming this function is enabled on the DRAM.



Pin Description Table (Contd.)

Symbol	Type	Polarity	Function
BA0~BA2	SSTL_15	-	Selects which SDRAM bank of the eight is activated.
A0~A13	SSTL_15	-	During a Bank Activate command cycle, address inputs define the row address (RA0–RA13). During a Read or Write command cycle, address inputs define the column address (CA0–CA9). In addition to the column address, AP is used to invoke auto-precharge operation at the end of the burst read or write cycle. If AP is high, auto-precharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
\overline{RAS} , \overline{CAS} , \overline{WE}	SSTL_15	Active Low	\overline{RAS} , \overline{CAS} , and \overline{WE} (along with \overline{CS}) define the command being entered.
DQ0~DQ63 CB0~CB7	SSTL_15	-	Data and Check Bit Input/Output pins.
$\overline{DQS0}$ ~ $\overline{DQS8}$ $\overline{DQS0}$ ~ $\overline{DQS8}$	SSTL_15	Differential Crossing	Data strobe for input and output data.
DM0~DM8	SSTL_15	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
SA0~SA1		-	These signals are tied at the system to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA		-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL		-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus tied to V_{DDSPD} to act as a pullup on the system board.
\overline{EVENT}	Output	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the \overline{EVENT} pin on TS/SPD part. No pull-up resistor is provided on DIMM.
\overline{RESET}	CMOS	Active Low	Asynchronous Reset is active when \overline{RESET} is LOW, and inactive when \overline{RESET} is HIGH. \overline{RESET} must be HIGH during normal operation. \overline{RESET} is CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} .
V_{DD} , V_{SS}	Supply	-	Power and ground for the DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules.
V_{DDQ}	Supply	-	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. V_{DDQ} shares the same power plane as V_{DD} pins.
V_{REFDQ}	Supply	-	Reference voltage for I/O inputs.
V_{REFCA}	Supply	-	Reference voltage for address/command inputs.
V_{DDSPD}	Supply	-	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.
V_{TT}	Supply	-	Termination voltage for address/command/control/clock nets.
NC	-	-	No Connect.

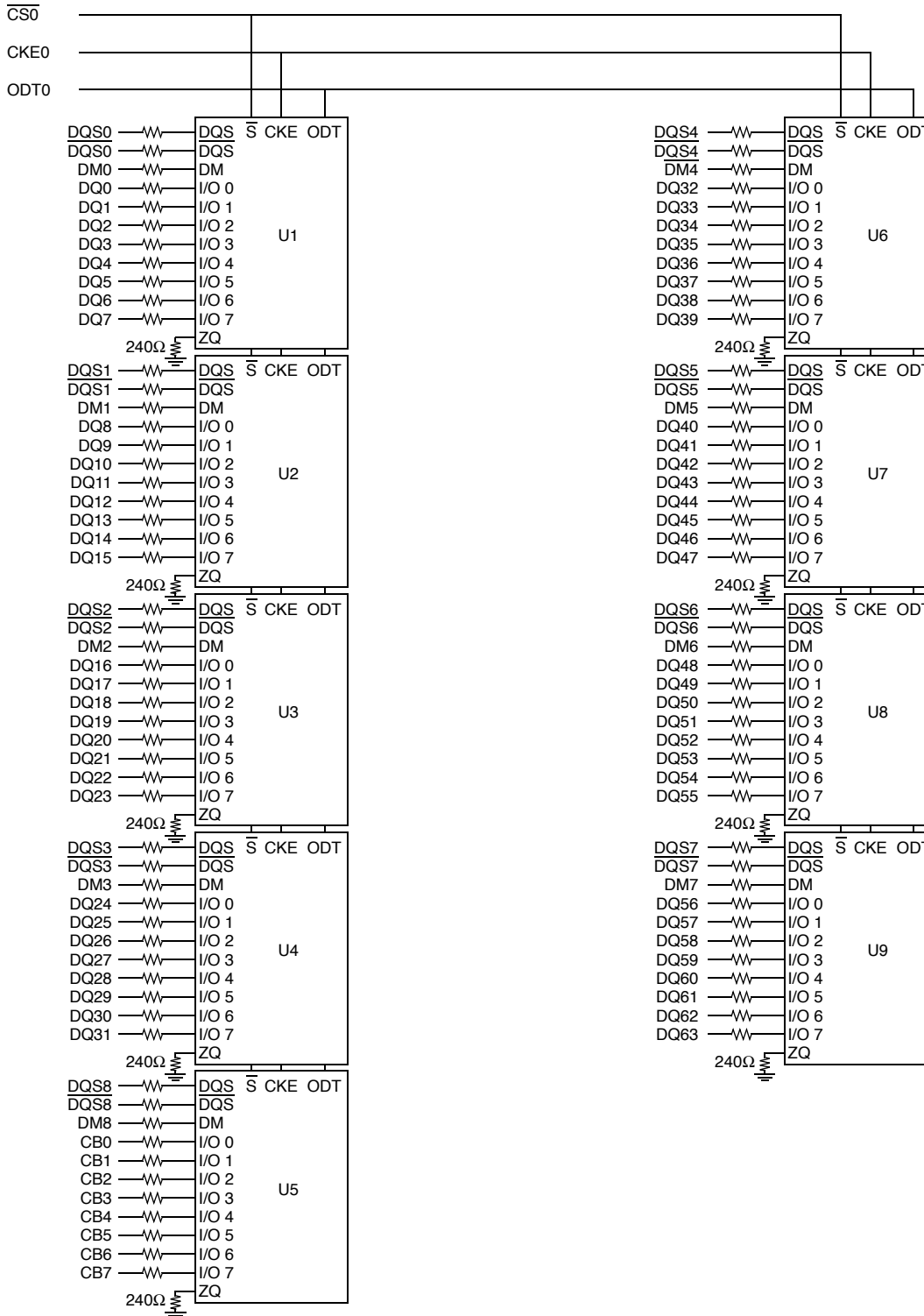


DDR3 204-pin SO-UDIMM Pin List

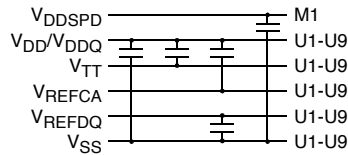
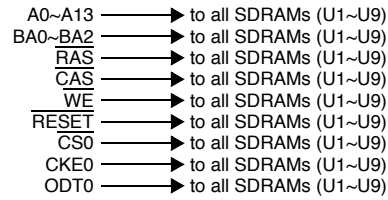
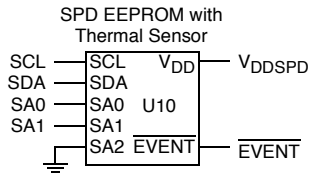
Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	VREFDQ	2	VSS	53	VSS	54	DQ28	105	A1	106	A2	157	DM5	158	VSS
3	VSS	4	DQ4	55	DQ24	56	DQ29	107	A0	108	BA1	159	DQ42	160	DQ46
5	DQ0	6	DQ5	57	DQ25	58	VSS	109	VDD	110	VDD	161	DQ43	162	DQ47
7	DQ1	8	VSS	59	DM3	60	$\overline{DQS3}$	111	CK0	112	CK1	163	VSS	164	VSS
9	VSS	10	$\overline{DQS0}$	61	VSS	62	DQS3	113	$\overline{CK0}$	114	$\overline{CK1}$	165	DQ48	166	DQ52
11	DM0	12	DQS0	63	DQ26	64	VSS	115	VDD	116	VDD	167	DQ49	168	DQ53
13	DQ2	14	VSS	65	DQ27	66	DQ30	117	A10/AP	118	$\overline{CS3}$ (NC)	169	VSS	170	VSS
15	DQ3	16	DQ6	67	VSS	68	DQ31	119	BA0	120	$\overline{CS2}$ (NC)	171	$\overline{DQS6}$	172	DM6
17	VSS	18	DQ7	69	CB0	70	VSS	121	\overline{WE}	122	\overline{RAS}	173	DQS6	174	DQ54
19	DQ8	20	VSS	71	CB1	72	CB4	123	VDD	124	VDD	175	VSS	176	DQ55
21	DQ9	22	DQ12	73	VSS	74	CB5	125	\overline{CAS}	126	ODT0	177	DQ50	178	VSS
23	VSS	24	DQ13	75	$\overline{DQS8}$	76	DM8	127	$\overline{CS0}$	128	ODT1 (NC)	179	DQ51	180	DQ60
25	$\overline{DQS1}$	26	VSS	77	DQS8	78	VSS	129	$\overline{CS1}$ (NC)	130	A13	181	VSS	182	DQ61
27	DQS1	28	DM1	79	VSS	80	CB6	131	VDD	132	VDD	183	DQ56	184	VSS
29	VSS	30	\overline{RESET}	81	CB2	82	CB7	133	DQ32	134	DQ36	185	DQ57	186	$\overline{DQS7}$
31	DQ10	32	VSS	83	CB3	84	VREFCA	135	DQ33	136	DQ37	187	VSS	188	DQS7
33	DQ11	34	DQ14	85	VDD	86	VDD	137	VSS	138	VSS	189	DM7	190	VSS
35	VSS	36	DQ15	87	CKE0	88	A15 (NC)	139	$\overline{DQS4}$	140	DM4	191	DQ58	192	DQ62
37	DQ16	38	VSS	89	CKE1 (NC)	90	A14 (NC)	141	DQS4	142	DQ38	193	DQ59	194	DQ63
39	DQ17	40	DQ20	91	BA2	92	A9	143	VSS	144	DQ39	195	VSS	196	VSS
41	VSS	42	DQ21	93	VDD	94	VDD	145	DQ34	146	VSS	197	SA0	198	\overline{EVENT}
43	$\overline{DQS2}$	44	DM2	95	A12/ \overline{BC}	96	A11	147	DQ35	148	DQ44	199	VDDSPD	200	SDA
45	DQS2	46	VSS	97	A8	98	A7	149	VSS	150	DQ45	201	SA1	202	SCL
47	VSS	48	DQ22	99	A5	100	A6	151	DQ40	152	VSS	203	VTT	204	VTT
49	DQ18	50	DQ23	101	VDD	102	VDD	153	DQ41	154	$\overline{DQS5}$				
51	DQ19	52	VSS	103	A3	104	A4	155	VSS	156	DQS5				



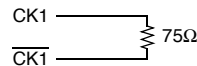
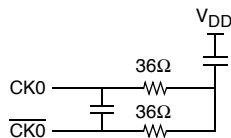
Block Diagram



Note: Unless otherwise noted, data resistor values are $15\Omega \pm 5\%$.



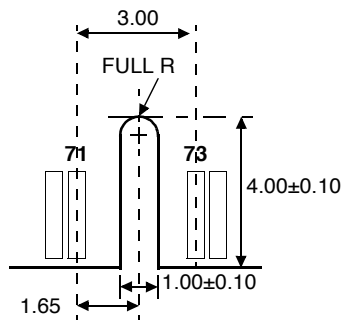
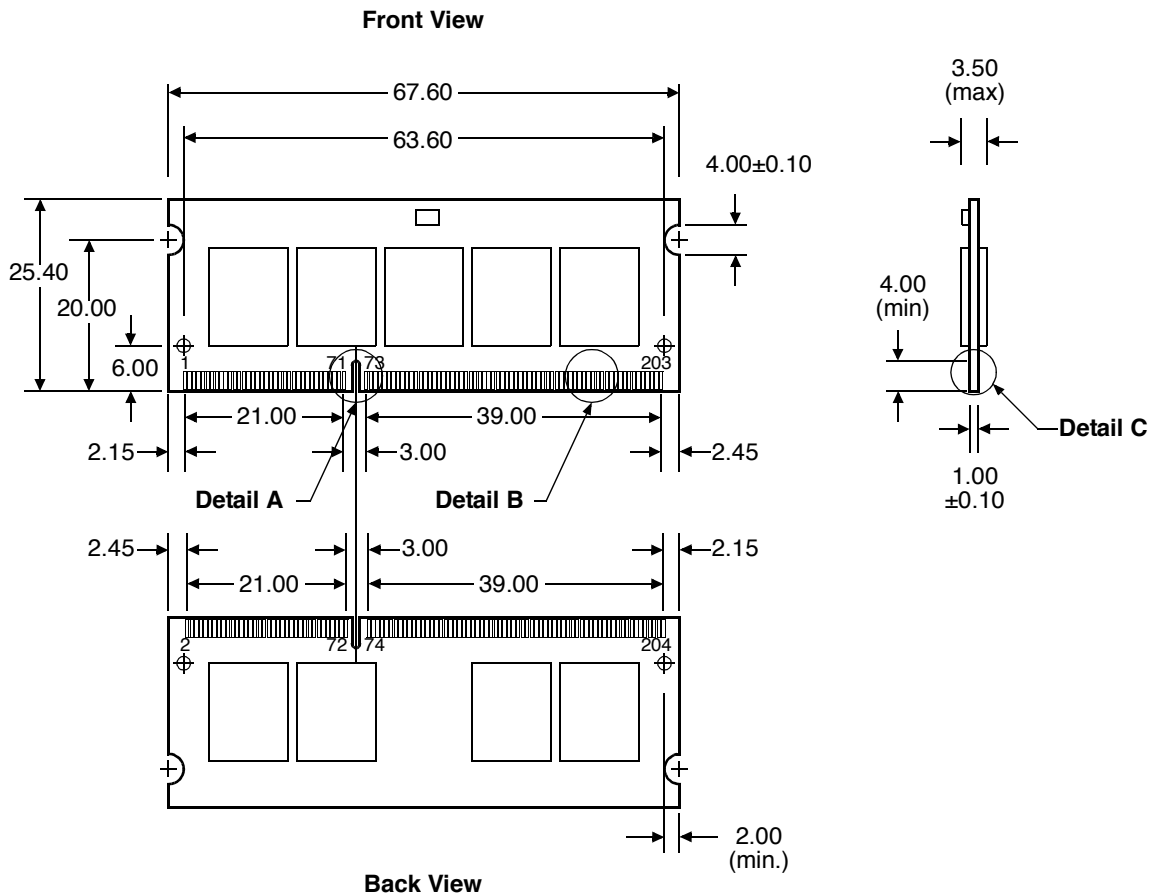
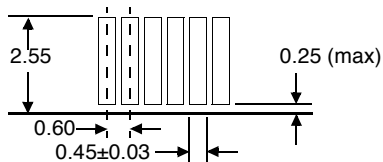
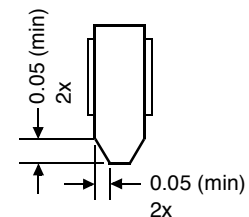
Clock Wiring	
CK0/CK0	9 SDRAMs
CK1/CK1	0 SDRAMs


Notes:

1. All address, command and control signal lines are terminated through a 36Ω series resistor to V_{TT}.
2. Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 6.

Physical Dimensions

204-pin SO-UDIMM Module


Detail A: Position of Voltage Notch

Detail B: Edge Connector

Detail C

 (All dimensions are in millimeters with $\pm 0.15\text{mm}$ tolerance unless specified otherwise.)



Serial Presence Detect Table (SPD provided for SG572288FH8DWLC1/PH1. All others are TBD.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
0	No. of Bytes Used, No. of Bytes in SPD Device, CRC Coverage	All	176, 256, 0~116	92h
1	SPD Revision	All	Revision 1.0	10h
2	Key Byte/DRAM Device Type	All	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	All	x72 SO-DIMM	07h
4	SDRAM Density and Banks	All	1Gb, 8 Banks	02h
5	SDRAM Addressing	All	14 Rows, 10 Columns	11h
6	Module Nominal Voltage, V _{DD}	All	1.5V	00h
7	Module Organization	All	1 Rank, x8	01h
8	Module Memory Bus Width	All	x72	0Bh
9	Fine Timebase (FTB) Dividend/Divisor	All	2.5ps	52h
10	Medium Timebase Dividend	All	1	01h
11	Medium Timebase Divisor	All	8	08h
12	Minimum SDRAM Cycle Time (t _{CKmin})	-LC -PH	1.875ns 1.5ns	0Fh 0Ch
13	Reserved	All	-	00h
14	CAS Latencies Supported (CL4-CL11)	-LC -PH	6, 7, 8 6, 8, 9	1Ch 34h
15	CAS Latencies Supported (CL12-CL18)	All	-	00h
16	Minimum CAS Latency Time (t _{AAmin})	-LC -PH	13.125ns 13.5ns	69h 6Ch
17	Minimum Write Recovery Time (t _{WRmin})	All	15ns	78h
18	Minimum RAS to CAS Delay Time (t _{RCDmin})	-LC -PH	13.125ns 13.5ns	69h 6Ch
19	Minimum Row Active to Row Active Delay Time (t _{RRDmin})	-LC -PH	7.5ns 6ns	3Ch 30h
20	Minimum Row Precharge Delay Time (t _{RPmin})	-LC -PH	13.125ns 13.5ns	69h 6Ch
21	Upper Nibbles for t _{RAS} and t _{RC}	All	-	11h
22	Minimum Active to Precharge Delay Time (t _{RASmin})	-LC -PH	37.5ns 36ns	2Ch 20h



Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Speed	Value Supported	Hex Value
23	Minimum Active to Active/Refresh Delay Time (t_{RCmin})	-LC -PH	50.625ns 49.5ns	95h 8Ch
24	Minimum Refresh Recovery Delay Time (t_{RFCmin}) (LSB)	All	110ns	70h
25	Minimum Refresh Recovery Delay Time (t_{RFCmin}) (MSB)	All	110ns	03h
26	Minimum Internal Write to Read Command Delay Time (t_{WTRmin})	All	7.5ns	3Ch
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTPmin})	All	7.5ns	3Ch
28	Upper Nibble for t_{FAW}	-LC -PH	37.5ns 30ns	01h 00h
29	Minimum Four Active Window Delay Time (t_{FAW})	-LC -PH	37.5ns 30ns	2Ch F0h
30	SDRAM Output Drivers Supported	All	DLL-off Mode, RZQ/7, RZQ/6	83h
31	SDRAM Thermal and Refresh Options	All	ASR, Ext. Temp. Range	05h
32	Module Thermal Sensor	All	EEPROM with Thermal Sensor	80h
33	SDRAM Device Type	All	Monolithic	00h
34~59	Reserved	All	-	00h
60	Module Nominal Height	All	25.4mm	0Bh
61	Module Maximum Thickness	All	Double-sided	11h
62	Reference Raw Card Used	All	R/C B, Rev 0	01h
63	Address Mapping from Edge Connector to DRAM	All	Standard	00h
64~116	Reserved	All	-	00h
117	Module Manufacturer ID Code (LSB)	All	Continuation Code	01h
118	Module Manufacturer ID Code (MSB)	All	Smart ID code	94h
119	Module Manufacturing Location	All	See Note 1	01h
120	Module Manufacturing Date (Year)	All	Date	Date
121	Module Manufacturing Date (Week)	All	Date	Date
122~125	Module Serial Number	All	Serial Number	S. No

Serial Presence Detect Table (Contd.)

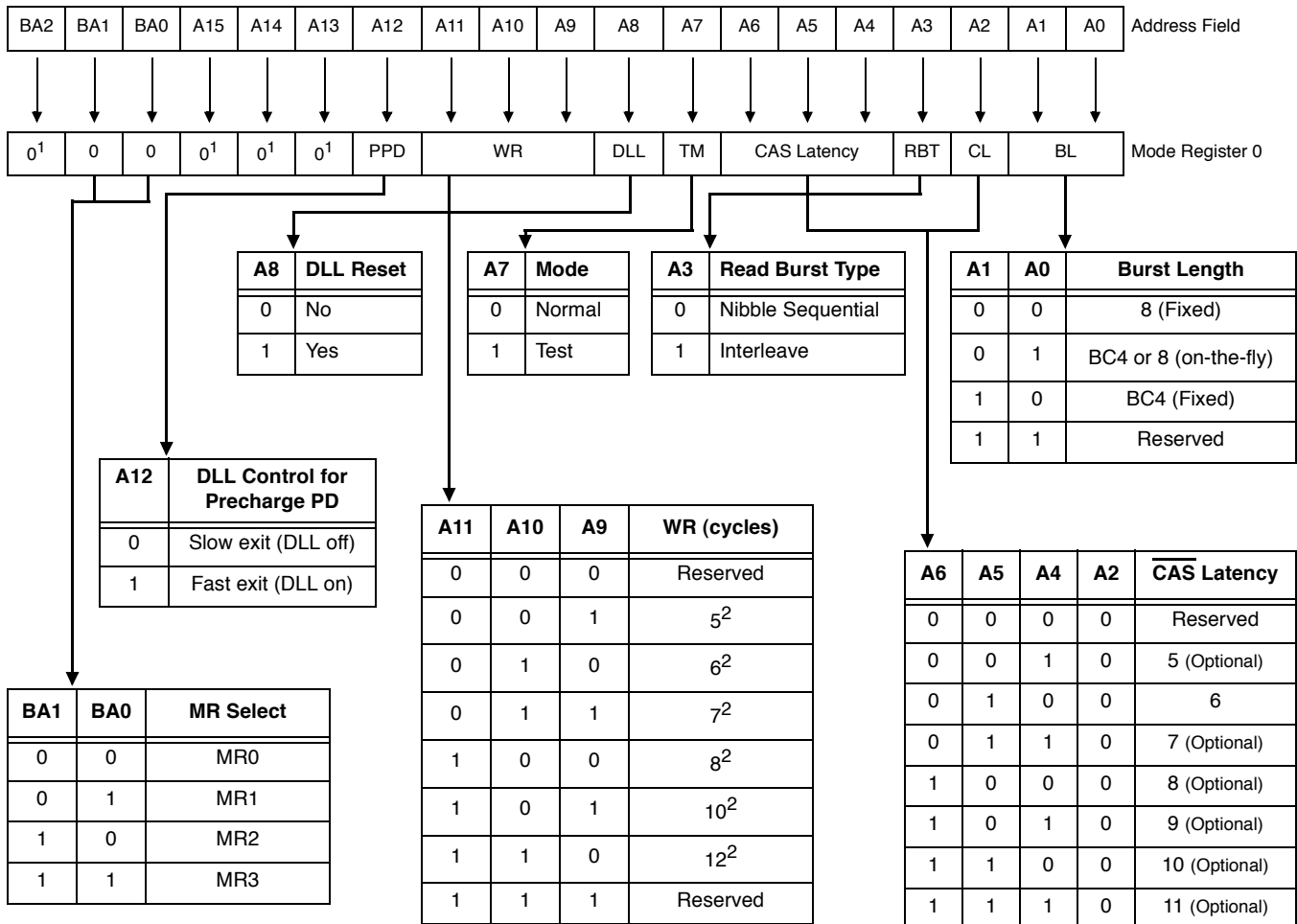
Byte No.	Byte Description	Speed	Value Supported	Value in Hex
126	SPD Cyclical Redundancy Code	-LC -PH		6Bh B9h
127	SPD Cyclical Redundancy Code	-LC -PH		F6h D0h
128~145	Module Part Number	All	SG572288FH8DWUU1	
146	Module Revision Code (SPD Revision)	All	Revision 0	00h
147	Module Revision Code	All	-	00h
148	DRAM Manufacturer ID Code (LSB)	All	Generic	00h
149	DRAM Manufacturer ID Code (MSB)	All	Generic	00h
150~173	Manufacturer Specific Data	All	SMART Modular Technologies	
174~175	Manufacturer Specific Data	All	-	00h
176~255	Open for Customer use	All	-	00h

Note:

- Manufacturing Location:
 - 00h - Undefined,
 - 01h - Fremont, USA,
 - 02h - Aguada, Puerto Rico,
 - 03h - East Kilbride, Scotland,
 - 04h - Penang, Malaysia,
 - 05h - Bangalore, India,
 - 06h - Sao Paulo, Brazil,
 - 07h - Aguadilla, Puerto Rico,
 - 08h - Mayaguez, Puerto Rico,
 - 09h - Santo Domingo, Dominican Republic,
 - 0Ah - Dongguan, China,

Mode Register (MR0) Table Definition

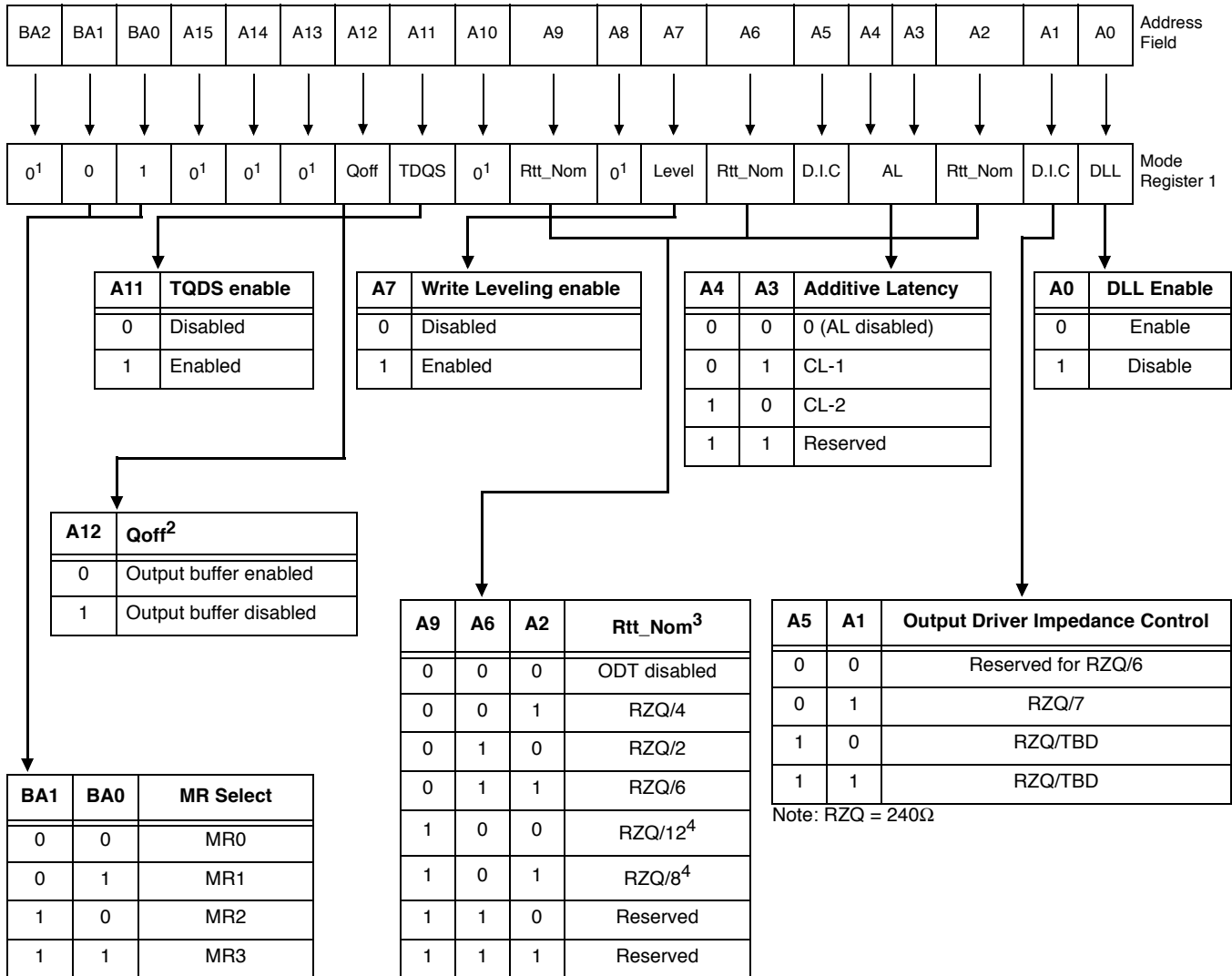
The mode register stores the data for controlling the various operating modes of DDR3 SDRAM. It controls CAS latency, burst length, burst chop, burst sequence, test mode, DLL reset, t_{WR} and various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , BA0, BA1 and BA2 while controlling the state of address pins A0~A15.


Notes:

- BA2 and A13~A15 are reserved for future use and must be programmed to 0 during MRS.
- WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: $WR_{min}[\text{cycles}] = \text{Round-up}(t_{WR}[\text{ns}] / t_{CK}[\text{ns}])$. The WR value in the mode register must be programmed to be equal or larger than WR_{min} . The programmed WR value is used with t_{RP} to determine t_{DAL} .

Mode Register (MR1) Table Definition

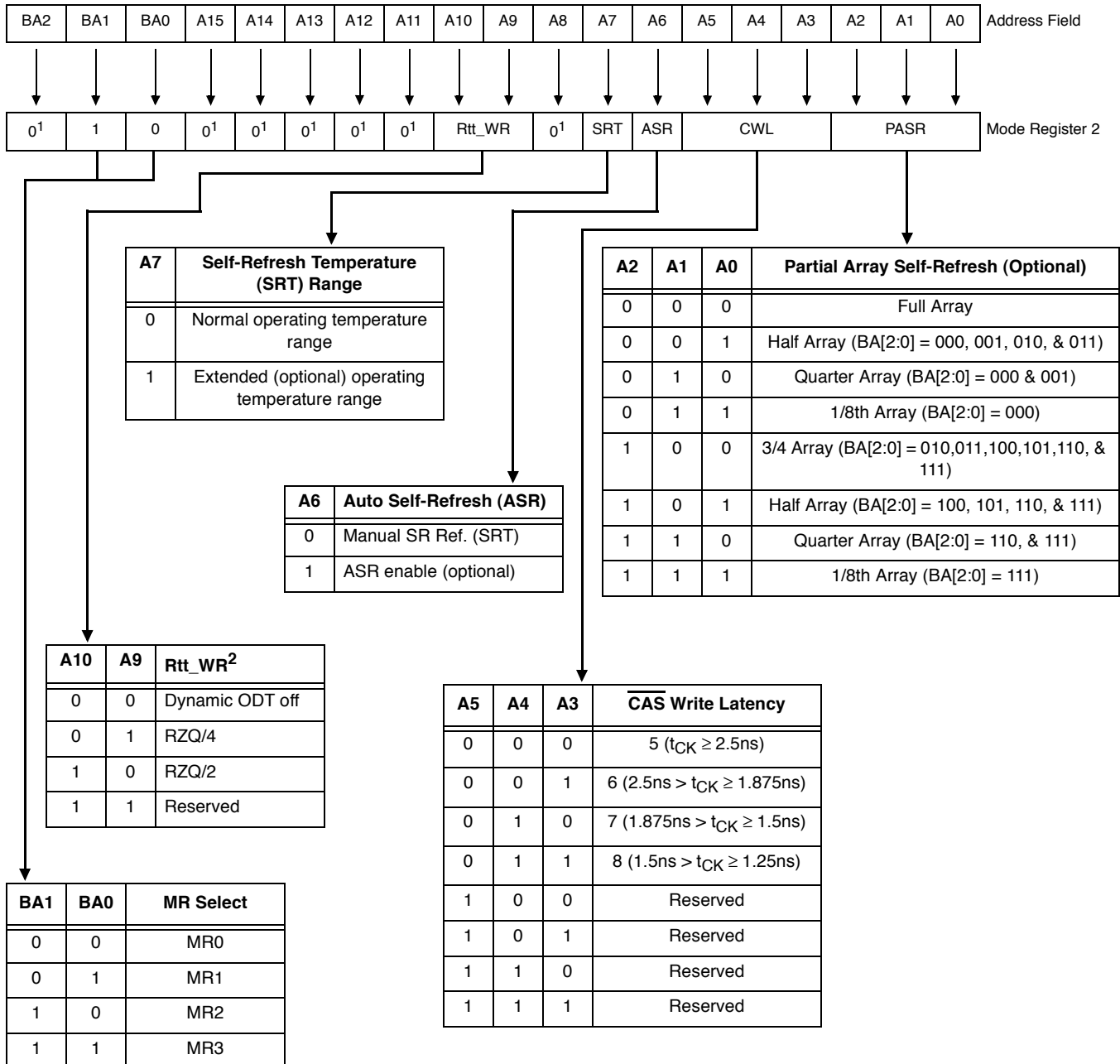
The Mode Registers MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write Leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , high on BA0 and low on BA1 and BA2, while controlling the state of address pins A0~A15.


Notes:

1. BA2 and A8, A10, A13~A15 are reserved for future use and must be programmed to 0 during MRS.
2. Outputs disabled - DQs, DQSs, DQSs.
3. In Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all Rtt_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only Rtt_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
4. If Rtt_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

Mode Register (MR2) Table Definition

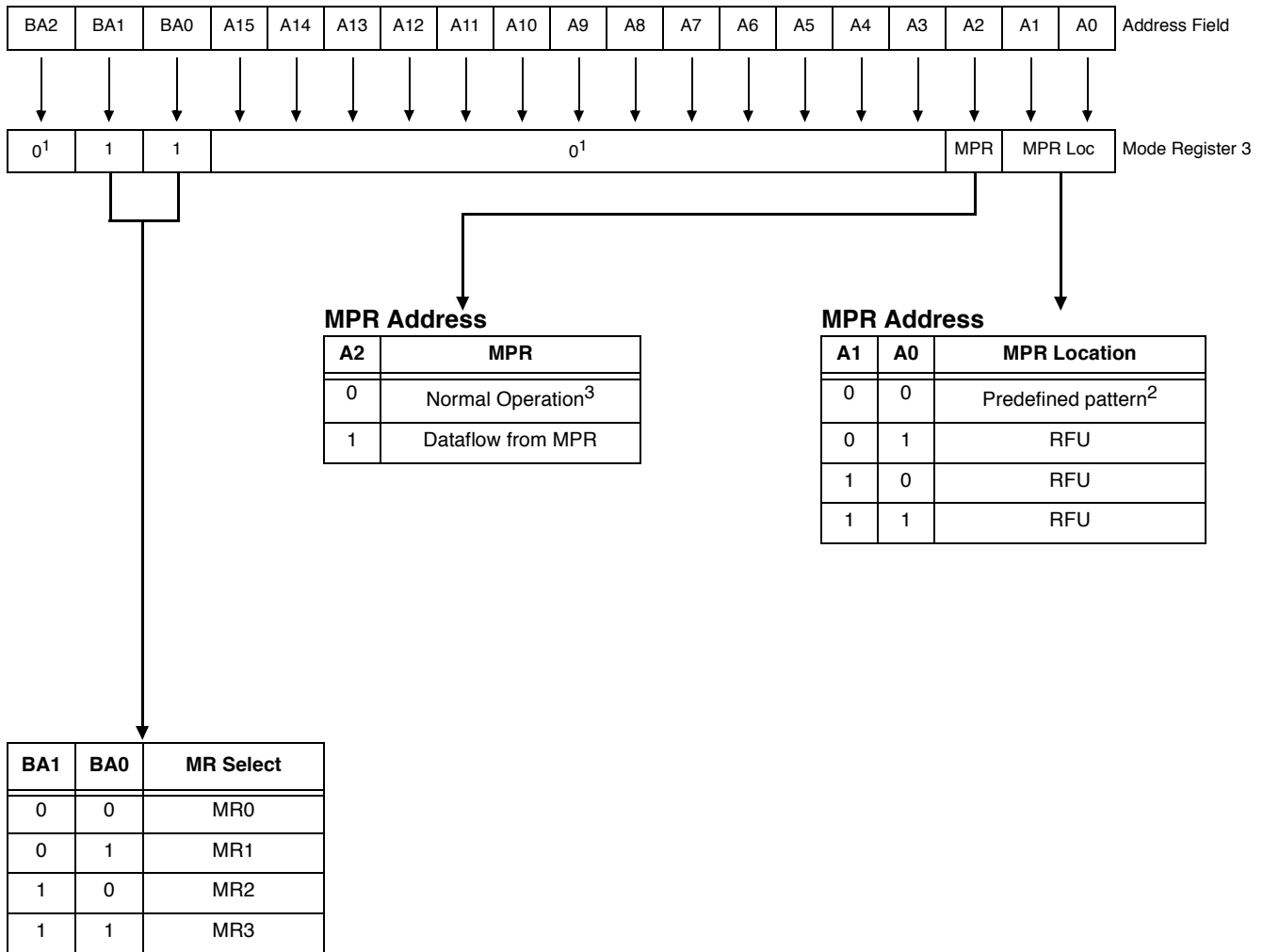
The Mode Registers MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS Write Latency. The Mode Register 2 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and low on BA0 and BA2 while controlling the state of address pins A0~A15.


Notes:

- BA2, A8 and A11~A15 are reserved for future use and must be programmed to 0 during MRS.
- If Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During Write Leveling, Dynamic ODT is not available.

Mode Register (MR3) Table Definition

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , high on BA1 and BA0, low on BA2 while controlling the state of address pins A0~A15.


Notes:

1. BA2, A3~A15 are reserved for future use and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0), then MR3 A[1:0] will be ignored.



Command Truth Table

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

- (a) Notes 1- 4 apply to the entire Command Truth Table.
- (b) Note 5 applies to all Read/Write command.

[BA= Bank address, RA= row Address, CA = Column Address, \overline{BC} = Burst chop, X = Don't care, V = Valid]

Function	Abbreviation	CKE		\overline{CS}	\overline{RAS}	\overline{CAS}	\overline{WE}	BA0~BA2	A13~A15	A12/ \overline{BC}	A10/AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self-Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7, 9, 12
Self-Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7, 8, 9, 12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge All Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power-Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
Power-Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	



Command Truth Table Notes:

1. All DDR3 SDRAM commands are defined by states of \overline{CS} , \overline{RAS} , \overline{CAS} , \overline{WE} , and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. \overline{RESET} command is enabled when Low, which will be used only for asynchronous reset, so \overline{RESET} must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS, BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by the MRS.
6. The Power-Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
8. Self-Refresh Exit is asynchronous.
9. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read and write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

- (a) Notes 1-7 apply to the entire CKE Truth Table.
 (b) CKE low is allowed only if tMRD and tMOD are satisfied.

Current State	CKE		Command (N) ³ RAS, CAS, WE, CS	Action (N) ³	Notes
	Previous Cycle (N-1)	Current Cycle (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	Deselect or NOP	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	Deselect or NOP	Self-Refresh Exit	8, 12, 16
Bank Activate	H	L	Deselect or NOP	Active Power-Down Entry	11, 13, 14
Reading	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Writing	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	Deselect or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	11, 13, 14, 18
		L	Refresh	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on the previous pages.					10

Notes:

- CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
- Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
- COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
- All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
- CKE must be registered with the same value on t_{CKEmin} consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the t_{CKEmin} clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKEmin} + t_{IH}.
- Deselect and NOP are defined in the Command Truth Table.
- On Self-Refresh Exit, Deselect or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
- Self-Refresh mode can only be entered from the All Banks Idle state.
- Must be a legal command as defined in the Command Truth Table.
- Valid commands for Power-Down Entry and Exit are NOP and Deselect only.
- Valid commands for Self-Refresh Exit are NOP and Deselect only.
- Self-Refresh can not be entered during Read or Write operations.
- The Power-Down does not perform any refresh operations.
- "X" means "don't care" (including floating around V_{REF}) in Self-Refresh and Power-Down. It also applies to Address pins.
- V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation.
- If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
- "Idle state" is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V _{DD}	Voltage on V _{DD} relative to V _{SS}	-0.4 ~ 1.975	V	1, 3
V _{DDQ}	Voltage on V _{DDQ} relative to V _{SS}	-0.4 ~ 1.975	V	1, 3
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.4 ~ 1.975	V	1
V _{DDSPD}	Voltage on V _{DDSPD} relative to V _{SS}	1.7 ~ 3.6	V	1
T _{STG}	Storage Temperature	-50 to +100	°C	1, 2

Notes:

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.
- V_{DD} and V_{DDQ} must be within 300 mV of each other at all times and V_{REF} must be not greater than 0.6*V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

Operating Temperature Range

Symbol	Parameter	Max	Units	Notes
T _{OPER}	Normal Operating Temperature Range (Case)	0 to 85	°C	1, 2
	Extended Operating Temperature Range (Optional)	85 to 95	°C	1, 3

Notes:

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the Extended Temperature Range. Please refer to the SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the SPD for option availability.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min	Typ	Max		
V _{DD}	Supply Voltage	1.425	1.5	1.575	V	1, 2
V _{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1
V _{DDSPD}	SPD Supply Voltage	3.0	3.3	3.6	V	
V _{TT}	SPD Supply Voltage	0.7125	0.75	0.7875	V	3
V _{SS}	Ground	0	0	0	V	

Notes:

- Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
- V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
- V_{TT} = V_{DDQ}/2

AC and DC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-800, 1066, & 1333		Units	Notes
		Min	Max		
V _{IH(DC)}	DC input logic high	V _{REF} + 0.100	V _{DD}	V	1
V _{IL(DC)}	DC input logic low	V _{SS}	V _{REF} - 0.100	V	1
V _{IH(AC)}	AC input logic high	V _{REF} + 0.175	-	V	1
V _{IL(AC)}	AC input logic low	-	V _{REF} - 0.175	V	1

Notes:

- For DQ and DM, V_{REF} = V_{REFDQ}. For input only pins except RESET#, V_{REF} = V_{REFCA}.
- The ac peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF(DC)} by more than ±1% V_{DD} (for reference: approx. ±15mV).
- For reference: approx. V_{DD}/2 ± 15mV.

Differential swing requirements for clock ($\overline{CK/CK}$) and strobe ($\overline{DQS/DQS}$)

Symbol	Parameter	DDR3-800, 1066, & 1333		Units	Notes
		Min	Max		
V_{IHDIFF}	Differential input logic high	0.200	Note 3	V	1
V_{ILDIFF}	Differential input logic high	Note 3	-0.200	V	1
$V_{IHDIFF(AC)}$	AC input logic high	$2 * (V_{IH(AC)} - V_{REF})$	Note 3	V	2
$V_{ILDIFF(AC)}$	AC input logic low	Note 3	$2 * (V_{REF} - V_{IL(AC)})$	V	2

Notes:

- Used to define a differential signal slew-rate.
- For $\overline{CK/CK}$, use $V_{IH}/V_{IL(AC)}$ of ADD/CMD and V_{REFCA} ; for $\overline{DQS/DQS}$, use $V_{IH}/V_{IL(AC)}$ of DQs and V_{REFDQ} ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
- These values are not defined, however the single-ended signals \overline{CK} , \overline{CK} , \overline{DQS} , \overline{DQS} need to be within the respective limits ($V_{IH(DC)max}$, $V_{IL(DC)min}$) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-ended Input Slew Rate Definition

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{REF}	$V_{IL(AC)min}$	$\frac{V_{IH(AC)min} - V_{REF}}{\Delta TRS}$	Setup (t_{IS} , t_{DS})
Input slew rate for falling edge	V_{REF}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS}$	
Input slew rate for rising edge	$V_{IL(DC)max}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH}$	Hold (t_{IH} , t_{DH})
Input slew rate for falling edge	$V_{IL(DC)min}$	V_{REF}	$\frac{V_{IH(DC)min} - V_{REF}}{\Delta TRH}$	

Input/Output Capacitance

Speed Bin		DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
Parameter	Symbol	min	max	min	max	min	max		
Input/output capacitance (DQ, DM, \overline{DQS} , \overline{DQS} , TDQS, \overline{TDQS})	C_{IO}	1.5	3.0	1.5	2.7	1.5	2.5	pF	1, 2
Input/output capacitance delta, (DQ, DM, \overline{DQS} , \overline{DQS} , TDQS, \overline{TDQS})	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 10
Input/output capacitance delta (DQS and \overline{DQS})	C_{DDQS}	0	0.2	0	0.2	0	0.15	pF	2, 4
Input capacitance, (CK and \overline{CK})	C_{CK}	7.2	14.4	7.2	14.4	7.2	12.6	pF	2
Input capacitance delta, (CK and \overline{CK})	C_{DCK}	0	1.32	0	1.32	0	1.35	pF	2, 3
Input capacitance, (ADD, CMD, CTRL input-only pins)	$C_{I_ADD_CMD}$	6.75	13.5	6.75	13.5	6.75	11.7	pF	2, 5
Input capacitance delta, (All ADD/CMD input-only pins)	$C_{DI_ADD_CMD}$	-4.5	4.5	-4.5	4.5	-3.6	3.6	pF	2, 6, 7
Input capacitance delta, (All CTRL input-only pins)	C_{DI_CTRL}	-4.5	2.7	-4.5	2.7	-3.6	1.8	pF	2, 8, 9

Notes:

- Although the DM, TDQS and \overline{TDQS} pins have different functions, the loading matches DQ and DQS.
- This parameter is not subject to production test. It is verified by design and characterization.
- Absolute value of $C_{CK} - C_{\overline{CK}}$
- Absolute value of $C_{IO}(DQS) - C_{IO}(\overline{DQS})$
- C_I applies to ODT, \overline{CS} , CKE, A0-A15, BA0-BA2, \overline{RAS} , \overline{CAS} , \overline{WE} .
- $C_{DI_ADD_CMD}$ applies to A0-A15, BA0-BA2, \overline{RAS} , \overline{CAS} and \overline{WE}
- $C_{DI_ADD_CMD} = C_I(ADD_CMD) - 0.5 * (C_I(CK) + C_I(\overline{CK}))$
- C_{DI_CTRL} applies to ODT, \overline{CS} and CKE
- $C_{DI_CTRL} = C_I(CTRL) - 0.5 * (C_I(CK) + C_I(\overline{CK}))$
- $C_{DIO} = C_{IO}(DQ,DM) - 0.5 * (C_{IO}(DQS) + C_{IO}(\overline{DQS}))$

IDD Timing Parameters

Speed Bin	DDR3-800		DDR3-1066			DDR3-1333		Units
Parameter	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	8-8-8	9-9-9	
$t_{CKmin}(IDD)$	2.5		1.875			1.5		ns
CL(IDD)	5	6	6	7	8	8	9	
$t_{RCdmin}(IDD)$	12.5	15	11.25	13.125	15	12	13.5	ns
$t_{RCmin}(IDD)$	50	52.5	48.75	50.625	52.5	48	49.5	ns
$t_{RASmin}(IDD)$	37.5	37.5	37.5	37.5	37.5	36	36	ns
$t_{RPmin}(IDD)$	12.5	15	11.25	13.125	15	12	13.5	ns
$t_{FAW}(IDD)$	40	40	37.5	37.5	37.5	30	30	ns
$t_{RRD}(IDD)$	10	10	7.5	7.5	7.5	6	6	ns
$t_{RFC}(IDD)$	110	110	110	110	110	110	110	ns

Definitions for IDD Measurement Conditions

- LOW is defined as $V_{IN} \leq V_{ILAC(max)}$; HIGH is defined as $V_{IN} \geq V_{IHAC(max)}$.
- STABLE is defined as inputs are stable at a HIGH or LOW level.
- FLOATING is defined as inputs are $V_{REF} = V_{DDQ} / 2$.
- Read Data is defined as the output data switching every clock, and Write Data is defined as the input data switching every clock, which means that Read Data and Write Data are stable during one clock cycle.
- SWITCHING is defined by the following table:

SWITCHING for Address, Bank Address, Command Signals, Data (DQ) and Data Masking (DM)	
Address (Row, Column):	If not otherwise mentioned, the inputs are stable at HIGH or LOW during 4 clock cycles and then change to the opposite value (e.g. Ax Ax Ax Ax Ax Ax Ax Ax Ax Ax Ax Ax)
Bank Address:	If not otherwise mentioned, the bank addresses should be switched like the row/column addresses
Command (\overline{CS} , RAS, CAS, \overline{WE}):	Define $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{HIGH, LOW, LOW, LOW\}$ Define $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{HIGH, HIGH, HIGH, HIGH\}$ Define Command Background Pattern = $\overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \overline{D} \dots$ If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective \overline{CS} , RAS, CAS, \overline{WE} levels of the necessary command.
Data (DQ):	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock.
Data Masking (DM):	No Switching; DM must be driven LOW at all times.



IDD Measurement Conditions

Symbol	Description	Conditions
I_{DD0}	Operating Current 0 → One bank Activate → Precharge	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}(IDD)$; $t_{RC} = t_{RCmin}(IDD)$; $t_{RAS} = t_{RASmin}(IDD)$; \overline{CS} is HIGH between Activate and Precharge commands; Command Inputs are SWITCHING except during Activate and Precharge commands; Row Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Address is fixed (bank 0); Data I/O are SWITCHING; Output Buffer (DQ/DQS) is Off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; Bank 0 active in a ACT-PRE loop; All other banks idle.
I_{DD1}	Operating Current 1 → One bank Activate → Read → Precharge	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}(IDD)$; $t_{RC} = t_{RCmin}(IDD)$; $t_{RAS} = t_{RASmin}(IDD)$; $t_{RCD} = t_{RCDmin}(IDD)$; $CL = CL(IDE)$; \overline{CS} is HIGH between Activate, Read and Precharge commands; Command Inputs are SWITCHING except during Activate, Read and Precharge commands; Row Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Address is fixed (bank 0); Data I/O are in Read Data; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve $I_{OUT} = 0mA$; Data I/O should be FLOATING when there is no READ DATA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); Bank 0 active in a ACT-RD-PRE loop; All other banks idle.
$I_{DD2P(0)}$	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	CKE is LOW; External Clock is on; $t_{CK} = t_{CKmin}(IDD)$; \overline{CS} is STABLE; Bank Addresses, Row Addresses and Command Inputs are STABLE; Data inputs are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle; Slow Exit (RD and ODT commands must satisfy $t_{XPDLL-AL}$) (MR0 bit A12 = 0).
$I_{DD2P(1)}^1$	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	CKE is LOW; External Clock is on; $t_{CK} = t_{CKmin}(IDD)$; \overline{CS} is STABLE; Bank Addresses, Row Addresses and Command Inputs are STABLE; Data inputs are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle; Fast Exit (any valid command after t_{XP}^2) (MR0 bit A12 = 1).
I_{DD2N}	Precharge Standby Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}(IDD)$; \overline{CS} is HIGH; Bank Addresses, Row Addresses and Command Inputs are SWITCHING; Data inputs are SWITCHING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle.
I_{DD2Q}	Precharge Quiet Standby Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}(IDD)$; \overline{CS} is HIGH; Bank Addresses, Row Addresses and Command Inputs are STABLE; Data Input are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle.



IDD Measurement Conditions (Contd.)

Symbol	Description	Conditions
I _{DD3P}	Active Power Down Current ³ Always Fast Exit	CKE is LOW; External Clock is on; t _{CK} = t _{CKmin} (IDD); CS is STABLE; Address and Command Inputs are STABLE; Data I/O are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks active; Active power Down Mode is always "Fast Exit" with DLL on.
I _{DD3N}	Active Standby Current	CKE is HIGH; External Clock is on; t _{CK} = t _{CKmin} (IDD); CS is HIGH; Address and Command Inputs are SWITCHING; Data I/O are SWITCHING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks active.
I _{DD4R}	Operating Current Burst Read	CKE is HIGH; External Clock is on; t _{CK} = t _{CKmin} (IDD); CL = CL(IDD); CS is HIGH between valid commands; Command Inputs are SWITCHING except during Read commands; Column Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Addresses are cycling (0 → 1 → 2 → 3); Data I/O use Seamless Read Data Burst (BL8); Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I _{OUT} = 0mA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); All banks active.
I _{DD4W}	Operating Current Burst Write	CKE is HIGH; External Clock is on; t _{CK} = t _{CKmin} (IDD); CL = CL(IDD); CS is HIGH between valid commands; Command Inputs are SWITCHING except during Write commands; Column Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Addresses are cycling (0 → 1 → 2 → 3); Data I/O use Seamless Write Data Burst (BL8); Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I _{OUT} = 0mA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); All banks active.
I _{DD5B}	Burst Refresh Current	CKE is HIGH; External Clock is on; t _{CK} = t _{CKmin} (IDD); t _{RFC} = t _{RFCmin} (IDD); CS is HIGH between valid commands; Address and Command inputs are SWITCHING; Data I/O are SWITCHING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; Refresh command every t _{RFC} = t _{RFCmin} .
I _{DD6}	Self-Refresh Current Normal Temperature Range T _{CASE} = 0 to 85°C	T _{CASE} = 85°C; Normal Temperature Range (MR2 bit A6 = 0); CKE is LOW; External Clock is off; CK/CK are LOW; CS is FLOATING; Command Inputs are FLOATING; Row and Column Addresses are FLOATING; Bank Addresses are FLOATING; Data I/O are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks are active during Self-Refresh actions; All banks are idle between Self-Refresh actions.



IDD Measurement Conditions (Contd.)

Symbol	Description	Conditions
I _{DD6ET}	Self-Refresh Current Extended Temperature Range T _{CASE} = 85 to 95°C	T _{CASE} = 95°C; Extended Temperature Range (MR2 bit A6 = 1); CKE is LOW; External Clock is off; CK/ \overline{CK} are LOW; \overline{CS} is FLOATING; Command Inputs are FLOATING; Row and Column Addresses are FLOATING; Bank Addresses are FLOATING; Data I/O are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks are active during Self-Refresh actions; All banks are idle between Self-Refresh actions.
I _{DD7}	All Bank Interleave Read Current	CKE is HIGH; External Clock is on; t _{CK} = t _{CKmin} (IDD); t _{RC} = t _{RCmin} (IDD); t _{RAS} = t _{RASmin} (IDD); t _{RCD} = t _{RCDmin} (IDD); t _{RRD} = t _{RRDmin} (IDD); CL = CL(IDD); AL = t _{RCDmin} - 1 * t _{CK} ; \overline{CS} is HIGH between valid commands; For Command inputs, see device datasheet for test patterns; Row and Column Addresses are STABLE during DESELECTs; Bank Addresses are cycling (0 → 1 → 2 → 3); Data I/O use Read Data (BL8); DM is low at all times; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I _{OUT} = 0mA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); All banks active (rotational).

Notes:

1. The MR0 bit A12 defines DLL on/off behavior only for precharge power down. There are 2 different Precharge Power Down states possible: one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).
2. Because it is an exit after precharge power down, the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh.
3. DDR3 will offer only ONE active power down mode with DLL on (→ fast exit). MR0 bit A12 will not be used for active power down. Instead bit A12 will be used to switch between two different precharge power down modes.



IDD Specifications

Speed Bin	DDR3-800		DDR3-1066			DDR3-1333		Units	Notes
	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	8-8-8	9-9-9		
I _{DD0}	810	810	900	900	900	990	990	mA	
I _{DD1}	990	990	1080	1080	1080	1170	1170	mA	
I _{DD2P(0)}	96	96	96	96	96	96	96	mA	
I _{DD2P(1)}	270	270	315	315	315	360	360	mA	
I _{DD2N}	450	450	495	495	495	585	585	mA	
I _{DD2Q}	414	414	477	477	477	540	540	mA	
I _{DD3P}	270	270	315	315	315	360	360	mA	
I _{DD3N}	468	468	513	513	513	558	558	mA	
I _{DD4R}	1170	1170	1440	1440	1440	1800	1800	mA	
I _{DD4W}	1440	1440	1710	1710	1710	1980	1980	mA	
I _{DD5B}	1800	1800	1980	1980	1980	2160	2160	mA	
I _{DD6}	54	54	54	54	54	54	54	mA	
I _{DD6ET}	81	81	81	81	81	81	81	mA	
I _{DD7}	3150	3150	3510	3510	3510	4410	4410	mA	

Refresh Parameters

Parameter	Symbol	1Gb	Units
REF command to ACT or REF command time	t_{RFC}	110	ns
Average periodic refresh interval	t_{REFI}	$0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$	μs
		$85\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 95\text{ }^{\circ}\text{C}$	μs

Device Standard Speed Bins

DDR3-800 Speed Bins

Speed Bin		DDR3-800				Units	Notes	
CL - nRCD - nRP		5-5-5		6-6-6				
Parameter	Symbol	min	max	min	max			
Internal read command to first data	t_{AA}	12.5	20	15	20	ns		
ACT to internal read or write delay time	t_{RCD}	12.5	-	15	-	ns		
Pre command period	t_{RP}	12.5	-	15	-	ns		
ACT to ACT or REF command period	t_{RC}	50	-	52.5	-	ns		
ACT to PRE command period	t_{RAS}	37.5	$9 * t_{REFI}$	37.5	$9 * t_{REFI}$	ns		
CL = 5	CWL = 5	$t_{CK(avg)}$	2.5	3.3	Reserved		ns	1, 2, 3, 4
CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	2.5	3.3	ns	1, 2, 3
Supported CL Settings		5, 6		6		n_{CK}		
Supported CWL Settings		5		5		n_{CK}		

Device Standard Speed Bins (Contd.)
DDR3-1066 Speed Bins

Speed Bin		DDR3-1066						Units	Notes	
CL - nRCD - nRP		6-6-6		7-7-7		8-8-8				
Parameter	Symbol	min	max	min	max	min	max			
Internal read command to first data	t _{AA}	11.25	20	13.125	20	15	20	ns		
ACT to internal read or write delay time	t _{RCD}	11.25	-	13.125	-	15	-	ns		
Pre command period	t _{RP}	11.25	-	13.125	-	15	-	ns		
ACT to ACT or REF command period	t _{RC}	48.75	-	50.625	-	52.5	-	ns		
ACT to PRE command period	t _{RAS}	37.5	9 * t _{REFI}	37.5	9 * t _{REFI}	37.5	9 * t _{REFI}	ns		
CL = 5	CWL = 5	t _{CK(avg)}	2.5	3.3	Reserved		Reserved		ns	1, 2, 3, 4, 5
	CWL = 6	t _{CK(avg)}	Reserved		Reserved		Reserved		ns	4
CL = 6	CWL = 5	t _{CK(avg)}	2.5	3.3	2.5	3.3	2.5	3.3	ns	1, 2, 3, 5
	CWL = 6	t _{CK(avg)}	1.875	< 2.5	Reserved		Reserved		ns	1, 2, 3, 4
CL = 7	CWL = 5	t _{CK(avg)}	Reserved		Reserved		Reserved		ns	4
	CWL = 6	t _{CK(avg)}	1.875	< 2.5	1.875	< 2.5	Reserved		ns	1, 2, 3, 4
CL = 8	CWL = 5	t _{CK(avg)}	Reserved		Reserved		Reserved		ns	1, 2, 3, 4
	CWL = 6	t _{CK(avg)}	1.875	< 2.5	1.875	< 2.5	1.875	< 2.5	ns	1, 2, 3
Supported CL Settings		5, 6, 7, 8		6, 7, 8		6, 8		nCK		
Supported CWL Settings		5, 6		5, 6		5, 6		nCK		



Device Standard Speed Bins (Contd.)

DDR3-1333 Speed Bins

Speed Bin		DDR3-1333				Units	Notes	
CL - nRCD - nRP		8-8-8		9-9-9				
Parameter	Symbol	min	max	min	max			
Internal read command to first data	t _{AA}	12	20	13.5	20	ns		
ACT to internal read or write delay time	t _{RCD}	12	-	13.5	-	ns		
Pre command period	t _{RP}	12	-	13.5	-	ns		
ACT to ACT or REF command period	t _{RC}	48	-	49.5	-	ns		
ACT to PRE command period	t _{RAS}	36	9 * t _{REFI}	36	9 * t _{REFI}	ns		
CL = 5	CWL = 5	t _{CK(avg)}	2.5	3.3	Reserved		ns	1, 2, 3, 4, 6
	CWL = 6, 7		Reserved		Reserved		ns	4
CL = 6	CWL = 5	t _{CK(avg)}	2.5	3.3	2.5	3.3	ns	1, 2, 3, 6
	CWL = 6, 7		Reserved		Reserved		ns	4
CL = 7	CWL = 5	t _{CK(avg)}	Reserved		Reserved		ns	4
	CWL = 6		1.875	< 2.5	Reserved		ns	1, 2, 3, 4, 6
	CWL = 7		Reserved		Reserved		ns	4
CL = 8	CWL = 5	t _{CK(avg)}	Reserved		Reserved		ns	4
	CWL = 6		1.875	< 2.5	1.875	< 2.5	ns	1, 2, 3, 6
	CWL = 7		1.5	< 1.875	Reserved		ns	1, 2, 3, 4
CL = 9	CWL = 5, 6	t _{CK(avg)}	Reserved		Reserved		ns	4
	CWL = 7		1.5	< 1.875	1.5	< 1.875	ns	1, 2, 3
Supported CL Settings		5, 6, 7, 8, 9		6, 8, 9		n _{CK}		
Supported CWL Settings		5, 6, 7		5, 6, 7		n _{CK}		

Speed Bin Tables Notes

1. The CL setting and CWL setting result in $t_{CK(AVG)min}$ and $t_{CK(AVG)max}$ requirements. When making a selection of $t_{CK(AVG)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(AVG)min}$ limits: Since \overline{CAS} Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{CK(AVG)}$ value (2.5, 1.875, or 1.5) when calculating $CL [nCK] = t_{AA} [ns] / t_{CK(AVG)} [ns]$, rounding up to the next 'Supported CL'.
3. $t_{CK(AVG)max}$ limits: Calculate $t_{CK(AVG)} = t_{AAmax} / CL \text{ SELECTED}$ and round the resulting $t_{CK(AVG)}$ down to the next valid speed bin (i.e. 3.3ns, 2.5ns, or 1.875 ns). This result is $t_{CK(AVG)max}$ corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.



Device Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Minimum clock cycle time (DLL off mode)	t _{CK(DLL_OFF)}	8	-	8	-	8	-	t _{CK}	6
Average clock period	t _{CK(avg)}	Refer to Speed Bins on pages 28-30.						ps	
Average high pulse width	t _{CH(avg)}	0.47	0.53	0.47	0.53	0.47	0.53	t _{CK(avg)}	
Average low pulse width	t _{CL(avg)}	0.47	0.53	0.47	0.53	0.47	0.53	t _{CK(avg)}	
Absolute clock period	t _{CK(abs)}	t _{CK(avg) min} + t _{JIT(per) min}	t _{CK(avg) max} + t _{JIT(per) max}	t _{CK(avg) min} + t _{JIT(per) min}	t _{CK(avg) max} + t _{JIT(per) max}	t _{CK(avg) min} + t _{JIT(per) min}	t _{CK(avg) max} + t _{JIT(per) max}	ps	
Absolute clock high pulse width	t _{CH(abs)}	0.43	-	0.43	-	0.43	-	t _{CK(avg)}	25
Absolute clock low pulse width	t _{CL(abs)}	0.43	-	0.43	-	0.43	-	t _{CK(avg)}	26
Clock period jitter	t _{JIT(per)}	-100	100	-90	90	-80	80	ps	
Clock period jitter during DLL locking period	t _{JIT(per, lck)}	-90	90	-80	80	-70	70	ps	
Cycle to cycle period jitter	t _{JIT(CC)}	200		180		160		ps	
Cycle to cycle period jitter during DLL locking period	t _{JIT(CC, lck)}	180		160		140		ps	
Duty cycle jitter	t _{JIT(duty)}	-	-	-	-	-	-	ps	
Cumulative error across 2 cycles	t _{ERR(2per)}	-147	147	-132	132	-118	118	ps	
Cumulative error across 3 cycles	t _{ERR(3per)}	-175	175	-157	157	-140	140	ps	
Cumulative error across 4 cycles	t _{ERR(4per)}	-194	194	-175	175	-155	155	ps	
Cumulative error across 5 cycles	t _{ERR(5per)}	-209	209	-188	188	-168	168	ps	
Cumulative error across 6 cycles	t _{ERR(6per)}	-222	222	-200	200	-177	177	ps	
Cumulative error across 7 cycles	t _{ERR(7per)}	-232	232	-209	209	-186	186	ps	
Cumulative error across 8 cycles	t _{ERR(8per)}	-241	241	-217	217	-193	193	ps	
Cumulative error across 9 cycles	t _{ERR(9per)}	-249	249	-224	224	-200	200	ps	
Cumulative error across 10 cycles	t _{ERR(10per)}	-257	257	-231	231	-205	205	ps	
Cumulative error across 11 cycles	t _{ERR(11per)}	-263	263	-237	237	-210	210	ps	
Cumulative error across 12 cycles	t _{ERR(12per)}	-269	269	-242	242	-215	215	ps	
Cumulative error across n = 13-50 cycles	t _{ERR(nper)}	$t_{ERR(nper)min} = (1 + 0.68\ln(n)) * t_{JIT(per)min}$ $t_{ERR(nper)max} = (1 + 0.68\ln(n)) * t_{JIT(per)max}$						ps	24

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data Timing									
DQS, \overline{DQS} to DQ skew, per group, per access	t_{DQSQ}	-	200	-	150	-	125	ps	13
DQ output hold time from DQS, \overline{DQS}	t_{QH}	0.38	-	0.38	-	0.38	-	$t_{CK(ave)}$	13, b
DQ low-impedance from CK, \overline{CK}	$t_{LZ(DQ)}$	-800	400	-600	300	-500	250	ps	13, 14, a
DQ high-impedance from CK, \overline{CK}	$t_{HZ(DQ)}$	-	400	-	300	-	250	ps	13, 14, a
Data setup time to DQS, \overline{DQS} referenced to $V_{IH(AC)} / V_{IL(AC)}$ levels	$t_{DS(base)}$	75	-	25	-	TBD	-	ps	17, d
Data hold time from DQS, \overline{DQS} referenced to $V_{IH(DC)} / V_{IL(DC)}$ levels	$t_{DH(base)}$	150	-	100	-	TBD	-	ps	17, d
Data Strobe Timing									
DQS, \overline{DQS} differential READ preamble	t_{RPRE}	0.9	Note 19	0.9	Note 19	0.9	Note 19	$t_{CK(ave)}$	13, 19, b
DQS, \overline{DQS} differential READ postamble	t_{RPST}	0.3	Note 11	0.3	Note 11	0.3	Note 11	$t_{CK(ave)}$	11, 13, b
DQS, \overline{DQS} differential output high time	t_{QSH}	0.38	-	0.38	-	0.4	-	$t_{CK(ave)}$	13, b
DQS, \overline{DQS} differential output low time	t_{QSL}	0.38	-	0.38	-	0.4	-	$t_{CK(ave)}$	13, b
DQS, \overline{DQS} differential WRITE preamble	t_{WPRE}	0.9	-	0.9	-	0.9	-	$t_{CK(ave)}$	
DQS, \overline{DQS} differential WRITE postamble	t_{WPST}	0.3	-	0.3	-	0.3	-	$t_{CK(ave)}$	
DQS, \overline{DQS} rising edge output access time from rising CK, \overline{CK}	t_{DQSK}	-400	400	-300	300	-255	255	ps	13, a
DQS and \overline{DQS} low-impedance time (Referenced from RL - 1)	$t_{LZ(DQS)}$	-800	400	-600	300	-500	250	ps	13, 14, a
DQS and \overline{DQS} low-impedance time (Referenced from RL + BL / 2)	$t_{HZ(DQS)}$	-	400	-	300	-	250	ps	13, 14, a
DQS, \overline{DQS} differential input low pulse width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK(ave)}$	
DQS, \overline{DQS} differential input high pulse width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK(ave)}$	
DQS, \overline{DQS} rising edge to CK, \overline{CK} rising edge	t_{DQSS}	-0.25	0.25	-0.25	0.25	-0.25	0.25	$t_{CK(ave)}$	c
DQS, \overline{DQS} falling edge setup time to CK, \overline{CK} rising edge	t_{DSS}	0.2	-	0.2	-	0.2	-	$t_{CK(ave)}$	c
DQS, \overline{DQS} falling edge hold time from CK, \overline{CK} rising edge	t_{DSH}	0.2	-	0.2	-	0.2	-	$t_{CK(ave)}$	c

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Command and Address Timing									
DLL locking time	t_{DLLK}	512	-	512	-	512	-	nCK	
Internal READ command to PRECHARGE command delay	t_{RTP}	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal READ command	t_{WTR}	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		18, e
WRITE recovery time	t_{WR}	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	t_{MRD}	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	t_{MOD}	max (12nCK, 15ns)	-	max (12nCK, 15ns)	-	max (12nCK, 15ns)	-		
ACT to internal read or write delay time	t_{RCD}	Refer to Speed Bins on pages 28-30.							e
PRECHARGE command period	t_{RP}	Refer to Speed Bins on pages 28-30.							e
ACT to ACT or REF command period	t_{RC}	Refer to Speed Bins on pages 28-30.							e
CAS to CAS command delay	t_{CCD}	4	-	4	-	4	-	nCK	
Auto-precharge write recovery + precharge time	$t_{DAL(min)}$	WR + roundup ($t_{RP} / t_{CK(avg)}$)						nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	t_{RAS}	Refer to Speed Bins on pages 28-30.							e
ACTIVE to ACTIVE command period for 1KB page size	t_{RRD}	max (4nCK, 10ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 6ns)	-		e
Four activate window for 1KB page size	t_{FAW}	40	-	37.5	-	30	-	ns	e
Command and Address setup time to CK, CK referenced to $V_{IH(AC)} / V_{IL(AC)}$ levels	$t_{IS(base)}$	200	-	125	-	65	-	ps	16, b
Command and Address hold time to CK, CK referenced to $V_{IH(DC)} / V_{IL(DC)}$ levels	$t_{IH(base)}$	275	-	200	-	140	-	ps	16, b
Command and Address setup time to CK, CK referenced to $V_{IH(AC)} / V_{IL(AC)}$ levels	$t_{IS(base)} AC150$	-	-	-	-	65 + 125	-	ps	16, 27, b
Calibration Timing									
Power-up and RESET calibration time	t_{zQinit}	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	t_{zQoper}	256	-	256	-	256	-	nCK	
Normal operation Short calibration time	t_{zQCS}	64	-	64	-	64	-	nCK	23



Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Reset Timing									
Exit Reset from CKE HIGH to a valid command	t _{XPR}	max (5nCK, t _{RFC} (min) + 10ns)	-	max (5nCK, t _{RFC} (min) + 10ns)	-	max (5nCK, t _{RFC} (min) + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh from to commands not requiring a locked DLL	t _{XS}	max (5nCK, t _{RFC} (min) + 10ns)	-	max (5nCK, t _{RFC} (min) + 10ns)	-	max (5nCK, t _{RFC} (min) + 10ns)	-		
Exit Self Refresh from to commands requiring a locked DLL	t _{XSDLL}	t _{DLLK} (min)	-	t _{DLLK} (min)	-	t _{DLLK} (min)	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing	t _{CKESR}	t _{CKE} (min) + 1nCK	-	t _{CKE} (min) + 1nCK	-	t _{CKE} (min) + 1nCK	-		
Valid clock requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t _{CKSRE}	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-		
Valid clock requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t _{CKSRX}	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-	max (5nCK, 10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t _{XP}	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t _{XPDLL}	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
Command pass disable delay	t _{CPDED}	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	t _{PD}	t _{CKE} (min)	9 * t _{REFI}	t _{CKE} (min)	9 * t _{REFI}	t _{CKE} (min)	9 * t _{REFI}		15
Timing of ACT command to Power Down entry	t _{ACTPDEN}	1	-	1	-	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	t _{PRPDEN}	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	t _{RDPDEN}	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
CKE minimum pulse width	t _{CKE}	max (3nCK, 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-	nCK	



Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t _{WRPDEN}	WL + 4 + (t _{WR} / t _{CK(avg)})	-	WL + 4 + (t _{WR} / t _{CK(avg)})	-	WL + 4 + (t _{WR} / t _{CK(avg)})	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t _{WRAPDEN}	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	WL + 4 + WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	t _{WRPDEN}	WL + 2 + (t _{WR} / t _{CK(avg)})	-	WL + 2 + (t _{WR} / t _{CK(avg)})	-	WL + 2 + (t _{WR} / t _{CK(avg)})	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	t _{WRAPDEN}	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	t _{REFPDEN}	1	-	1	-	1	-	nCK	20, 21
Timing of MRS command to Power Down entry	t _{MRSPDEN}	t _{MOD} (min)	-	t _{MOD} (min)	-	t _{MOD} (min)	-		
ODT Timing									
ODT high time without Write command or with Write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t _{AONPD}	1	9	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t _{AOFPD}	1	9	1	9	1	9	ns	
RTT turn-on	t _{AON}	-400	400	-300	300	-250	250	ps	7, a
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t _{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	t _{CK(avg)}	8, a
RTT dynamic change skew	t _{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	t _{CK(avg)}	a
Write Leveling Timing									
First DQS/DQS rising edge after write leveling mode is programmed	t _{WLMRD}	40	-	40	-	40	-	nCK	3
DQS/DQS delay after write leveling mode is programmed	t _{WLDQSEN}	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	t _{WLS}	325	-	245	-	195	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	t _{WLH}	325	-	245	-	195	-	ps	
Write leveling output delay	t _{WLO}	0	9	0	9	0	9	ns	
Write leveling output error	t _{WLOE}	0	2	0	2	0	2	ns	



Device Timing Parameters Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in the Mode Register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI} .
7. Minimum RTT turn-on time (t_{AONmin}) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (t_{AONmax}) is the point in time when the ODT resistance is fully on. Both are measured from ODTL_{on}.
8. Minimum RTT turn-off time (t_{AOFmin}) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (t_{AOFmax}) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTL_{off}.
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR} / t_{CK} to the next integer.
10. WR is in clock cycles as programmed in MR0.
11. The maximum postamble is bound by $t_{HZDQS(max)}$.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34.
14. Single ended signal parameter.
15. t_{REFI} depends on T_{OPER} .
16. $t_{IS(base)}$ and $t_{IH(base)}$ values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, \overline{CK} differential slew rate. Note for DQ and DM signals, $V_{REF(DC)} = V_{REFDQ(DC)}$. For input only pins except \overline{RESET} , $V_{REF(DC)} = V_{REFCA(DC)}$.
17. $t_{DS(base)}$ and $t_{DH(base)}$ values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, \overline{DQS} differential slew rate. Note for DQ and DM signals, $V_{REF(DC)} = V_{REFDQ(DC)}$. For input only pins except \overline{RESET} , $V_{REF(DC)} = V_{REFCA(DC)}$.
18. Start of internal write transaction is defined as follows:
 For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by $t_{LZDQS(min)}$.
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN(min)}$ is satisfied, there are cases where additional time such as $t_{XPDLL(min)}$ is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
 One method for calculating the interval between ZQCS commands, given the temperature ($T_{driftrate}$) and voltage ($V_{driftrate}$) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where $TSens = \max(dRRTdT, dRONdTM)$ and $VSens = \max(dRTTdV, dRONdVM)$ define the SDRAM temperature and voltage sensitivities.

For example, if $TSens = 1.5\% / ^\circ C$, $VSens = 0.15\% / mV$, $Tdriftrate = 1 ^\circ C / sec$ and $Vdriftrate = 15 mV / sec$, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 + 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The $t_{IS(base)}$ AC150 specifications are adjusted from the $t_{IS(base)}$ specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

Jitter Notes

- a When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(mper)act}$ of the input clock, where $2 \leq m \leq 12$. (Output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has $t_{ERR(mper)act,min} = -172$ ps and $t_{ERR(mper)act,max} = +193$ ps, then $t_{DQSCkmin(derated)} = t_{DQSCkmin} - t_{ERR(mper)act,max} = -400$ ps - 193 ps = -593 ps and $t_{DQSCkmax(derated)} = t_{DQSCk,max} - t_{ERR(mper)act,min} = 400$ ps + 172 ps = +572 ps. Similarly, $t_{LZ(DQ)}$ for DDR3-800 derates to $t_{LZ(DQ)min(derated)} = -800$ ps - 193 ps = -993 ps and $t_{LZ(DQ)max(derated)} = 400$ ps + 172 ps = +572 ps. (Caution on the min/max usage!)

Note that $t_{ERR(mper)act,min}$ is the minimum measured value of $t_{ERR(nper)}$ where $2 \leq n \leq 12$, and $t_{ERR(mper)act,max}$ is the maximum measured value of $t_{ERR(nper)}$ where $2 \leq n \leq 12$.

- b When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per),act}$ of the input clock. (Output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has $t_{CK(avg)act} = 2500$ ps, $t_{JIT(per)act,min} = -72$ ps and $t_{JIT(per)act,max} = +93$ ps, then $t_{RPREmin(derated)} = t_{RPREmin} + t_{JIT(per)act,min} = 0.9 \times t_{CK(avg)act} + t_{JIT(per)act,min} = 0.9 \times 2500$ ps - 72 ps = +2178 ps. Similarly, $t_{QHmin(derated)} = t_{QHmin} + t_{JIT(per)act,min} = 0.38 \times t_{CK(avg)act} + t_{JIT(per)act,min} = 0.38 \times 2500$ ps - 72 ps = +878 ps. (Caution on the min/max usage!)

- c These parameters are measured from a data strobe signal (\overline{DQS} , \overline{DQS}) crossing to its respective clock signal (\overline{CK} , \overline{CK}) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT(per)}$, $t_{JIT(cc)}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- d These parameters are measured from a data signal (\overline{DM} , $\overline{DQ0}$, $\overline{DQ1}$, etc.) transition edge to its respective data strobe signal (\overline{DQS} , \overline{DQS}) crossing.
- e For these parameters, the DDR3 SDRAM device supports $t_{nPARAM} [nCK] = RU\{t_{PARAM} [ns] / t_{CK(avg)} [ns]\}$, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP} = RU\{t_{RP} / t_{CK(avg)}\}$, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which $t_{RP} = 15$ ns, the device will support $t_{nRP} = RU\{t_{RP} / t_{CK(avg)}\} = 6$, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at $Tm+6$ is valid even if $(Tm+6 - Tm)$ is less than 15 ns due to input clock jitter.

Part Number Decode

<u>S</u>	<u>G</u>	<u>5</u>	<u>72</u>	<u>28</u>	<u>8</u>	<u>F</u>	<u>H</u>	<u>8</u>	<u>D</u>	<u>W</u>	<u>U</u>	<u>U</u>	<u>1</u>
1	2	3	4	5	6	7	8	9	10	11	12	13	

- 1 SMART Modular Technologies**
- 2 Module Process Technology**
G: Green Module (RoHS Compliant)
- 3 Product Category**
5: SDRAM DIMM with Standard Testing
- 4 Module Data Bus Width**
72: x72
- 5 Module Address Depth**
28: 128M
- 6 Device Data Width**
8: x8
- 7 Special Device Feature**
F: Standard FBGA (8 Bank SDRAM)
- 8 Technology**
H: DDR3 SDRAM
- 9 Refresh/Power**
8: 8K Refresh/Standard Power
- 10 Module Configuration**
D: 204-pin SO-UDIMM Unbuffered, ECC
- 11 Device Physicals**
W: 1Gbit Device Based
- 12 CAS Latencies Supported**
6: 6
K: 5, 6
R: 5, 6, 7, 8
L: 6, 7, 8
M: 6, 8
N: 5, 6, 7, 8, 9
P: 6, 8, 9

- 13 Cycle Time (Clock Speed)**
A: 2.5ns (400MHz, PC3-6400, DDR3-800-555)
B: 2.5ns (400MHz, PC3-6400, DDR3-800-666)
C: 1.875ns (533MHz, PC3-8500, DDR3-1066-777)
D: 1.875ns (533MHz, PC3-8500, DDR3-1066-888)
E: 1.875ns (533MHz, PC3-8500, DDR3-1066-666)
G: 1.5ns (667MHz, PC3-10600, DDR3-1333-888)
H: 1.5ns (667MHz, PC3-10600, DDR3-1333-999)

Note: "UU" in the part number should be replaced by user specified option.

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