



**Ordering Information**

<b>Part Numbers</b>	<b>Description</b>	<b>Module Speed</b>
SG564128FG8NZDB	512Mx64 (4GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based, DDR2-400-333, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-3200 @ CL 3.0
SG564128FG8NZDG	512Mx64 (4GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based, DDR2-533-444, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-4200 @ CL 4.0
SG564128FG8NZIL	512Mx64 (4GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based, DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-5300 @ CL 5.0
SG564128FG8NZIR	512Mx64 (4GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based, DDR2-800-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-6400 @ CL 5.0
SG564128FG8NZKF	512Mx64 (4GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based, DDR2-800-666, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-6400 @ CL 6.0

(All specifications of this module are subject to change without notice.)



## Revision History

- **February 19, 2009**  
Datasheet released.



**4GByte (512Mx64) DDR2 SDRAM Module - 256Mx8 Based  
200-pin SO-DIMM, Unbuffered, Non-ECC**

**Features**

- Standard : JEDEC
- Configuration : Non-ECC
- Cycle Time : 5.0ns (DDR2-400)  
3.75ns (DDR2-533)  
3.0ns (DDR2-667)  
2.5ns (DDR2-800)
- CAS# Latency : 3.0, 4.0 (-DB/DG)  
4.0, 5.0 (-IL/IR)  
5.0, 6.0 (-KF)
- Posted CAS#/Additive Latency (AL) : 0, 1.0, 2.0, 3.0 & 4.0
- Write Latency (WL) : Read (CAS#) Latency - 1
- Burst Length : 4, 8
- Burst Type : Sequential/Interleave
- Module Ranks : 2 Ranks of x8 devices
- No. of Devices : 16
- No. of Internal Banks per SDRAM : 8
- Operating Voltage : 1.8V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 67.60mm x 30.00mm
- No. of sides : Double-sided
- Mating Connector (Examples)  
Horizontal : AMP - 1473150-4

**DDR2 200-pin SO-DIMM Pin List**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VREF	2	VSS	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	VSS	4	DQ4	53	VSS	54	VSS	103	VDD	104	VDD	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	VSS	156	VSS
7	DQ1	8	VSS	57	DQ19	58	DQ23	107	BA0	108	RAS#	157	DQ48	158	DQ52
9	VSS	10	DM0	59	VSS	60	VSS	109	WE#	110	CS0#	159	DQ49	160	DQ53
11	DQS0#	12	VSS	61	DQ24	62	DQ28	111	VDD	112	VDD	161	VSS	162	VSS
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	CAS#	114	ODT0	163	NC	164	CK1
15	VSS	16	DQ7	65	VSS	66	VSS	115	CS1#	116	A13	165	VSS	166	CK1#
17	DQ2	18	VSS	67	DM3	68	DQS3#	117	VDD	118	VDD	167	DQS6#	168	VSS
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	VSS	22	DQ13	71	VSS	72	VSS	121	VSS	122	VSS	171	VSS	172	VSS
23	DQ8	24	VSS	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	VSS	28	VSS	77	VSS	78	VSS	127	VSS	128	VSS	177	VSS	178	VSS
29	DQS1#	30	CK0	79	CKE0	80	CKE1	129	DQS4#	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	CK0#	81	VDD	82	VDD	131	DQS4	132	VSS	181	DQ57	182	DQ61
33	VSS	34	VSS	83	NC	84	A15 (NC)	133	VSS	134	DQ38	183	VSS	184	VSS
35	DQ10	36	DQ14	85	BA2	86	A14	135	DQ34	136	DQ39	185	DM7	186	DQS7#
37	DQ11	38	DQ15	87	VDD	88	VDD	137	DQ35	138	VSS	187	VSS	188	DQS7
39	VSS	40	VSS	89	A12	90	A11	139	VSS	140	DQ44	189	DQ58	190	VSS



**DDR2 200-pin SO-DIMM Pin List (Contd.)**

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
41	V <sub>SS</sub>	42	V <sub>SS</sub>	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V <sub>SS</sub>	193	V <sub>SS</sub>	194	DQ63
45	DQ17	46	DQ21	95	V <sub>DD</sub>	96	V <sub>DD</sub>	145	V <sub>SS</sub>	146	DQS5#	195	SDA	196	V <sub>SS</sub>
47	V <sub>SS</sub>	48	V <sub>SS</sub>	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	DQS2#	50	NC	99	A3	100	A2	149	V <sub>SS</sub>	150	V <sub>SS</sub>	199	V <sub>DDSPD</sub>	200	SA1

**Pin Description Table**

Symbol	Type	Polarity	Function
CK0, CK1	SSTL_18	Positive Edge	Positive line of the differential pair of system clock inputs. (All DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. Output data is referenced at the crossings of the clocks.)
CK0#, CK1#	SSTL_18	Negative Edge	Negative line of the differential pair of system clock inputs.
ODT0, ODT1	SSTL_18	Active High	On-Die Termination: ODT when high enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, and DM. The ODT input will be ignored if disabled in Extended Mode Register (EMRS).
CKE0, CKE1	SSTL_18	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	SSTL_18	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	SSTL_18	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0~BA2	SSTL_18	-	Bank Address define to which bank an Activate, Read, Write or Precharge command is being applied. Bank address also determines if the Mode Register or Extended Mode Register is to be accessed during a MRS or EMRS cycle.
A0~A9, A10/AP, A11~A14	SSTL_18	-	During a Bank Activate command cycle, A0-A14 defines the row address (RA0-RA14) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge. The address inputs also provide the op-code during Mode Register Set commands.

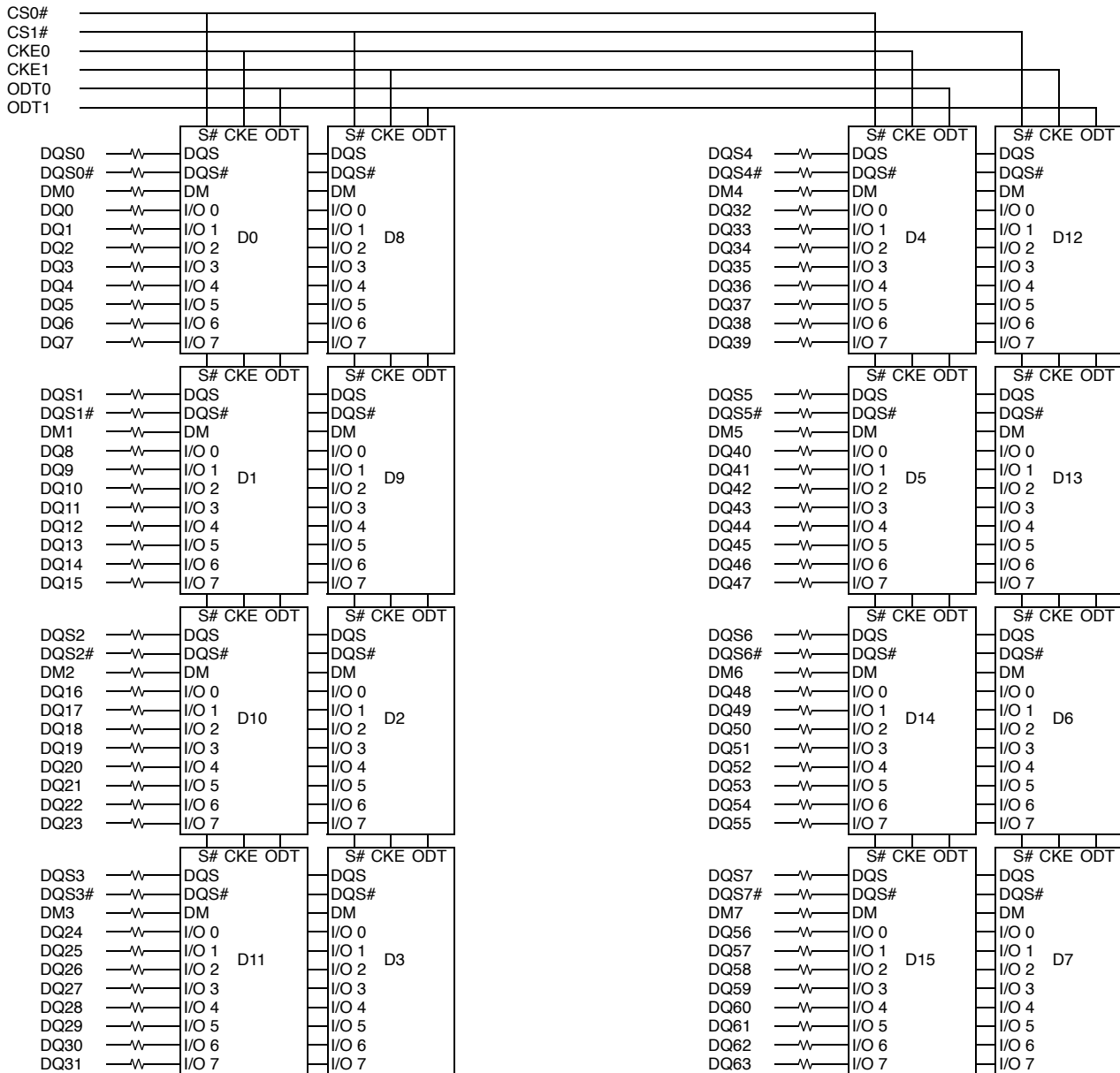


**Pin Description Table (Contd.)**

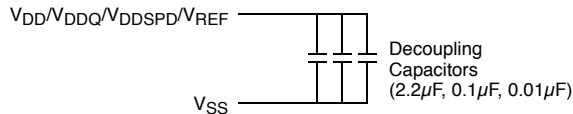
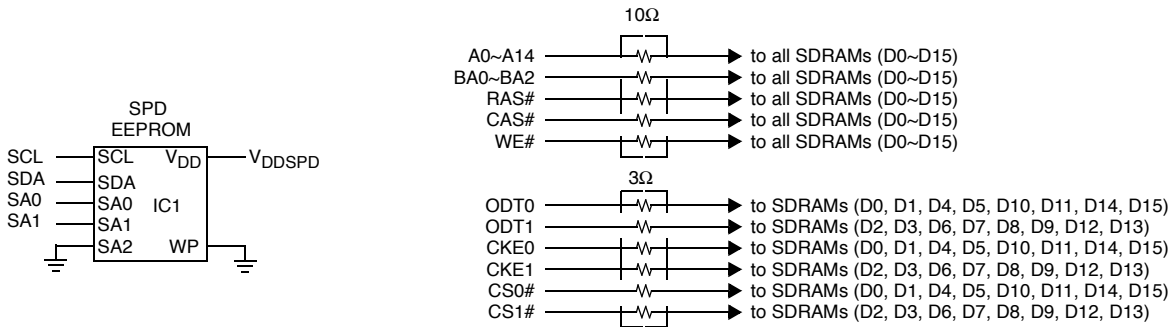
Symbol	Type	Polarity	Function
DQ0~DQ63	SSTL_18	-	Data Input/Output pins.
DQS0~DQS7	SSTL_18	Positive Edge	SDRAM differential data strobe for input and output data.
DQS0#~DQS7#	SSTL_18	Negative Edge	SDRAM differential data strobe for input and output data.
DM0~DM7	SSTL_18	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ/DQS loading.
SA0~SA1	LVTTTL	-	Slave Address Select for EEPROM. These pins are used to configure the presence-detect device.
SDA	LVTTTL	-	Serial Bus Data Line for EEPROM. SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. A resistor must be connected from the SDA bus line to V <sub>DDSPD</sub> to act as pull up on the system board.
SCL	LVTTTL	-	Serial Bus Clock for EEPROM. SCL is used to synchronize the presence-detect data transfer to and from the module. A resistor may be connected from the SCL bus line to V <sub>DDSPD</sub> to act as pull up on the system board.
V <sub>DD</sub>	Supply	-	SDRAM positive power supply. 1.8V±0.1V
V <sub>SS</sub>	Supply	-	Power supply return (ground).
V <sub>REF</sub>	Supply	-	SDRAM I/O reference supply.
V <sub>DDSPD</sub>	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports operation from 1.7V to 3.6V).
NC	-	-	No Connect.



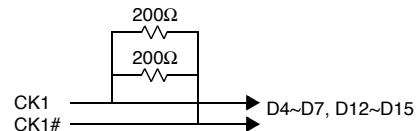
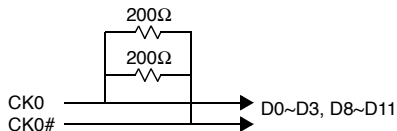
**Block Diagram**



Note: Unless otherwise noted, data resistor values are 22Ω ± 5%.



Clock Wiring	
CK0/CK0#	8 SDRAMs
CK1/CK1#	8 SDRAMs

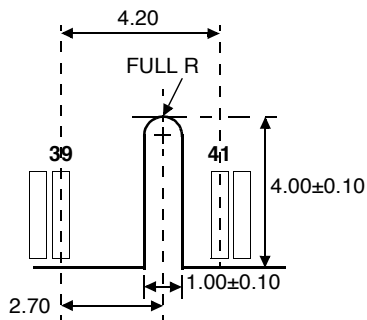
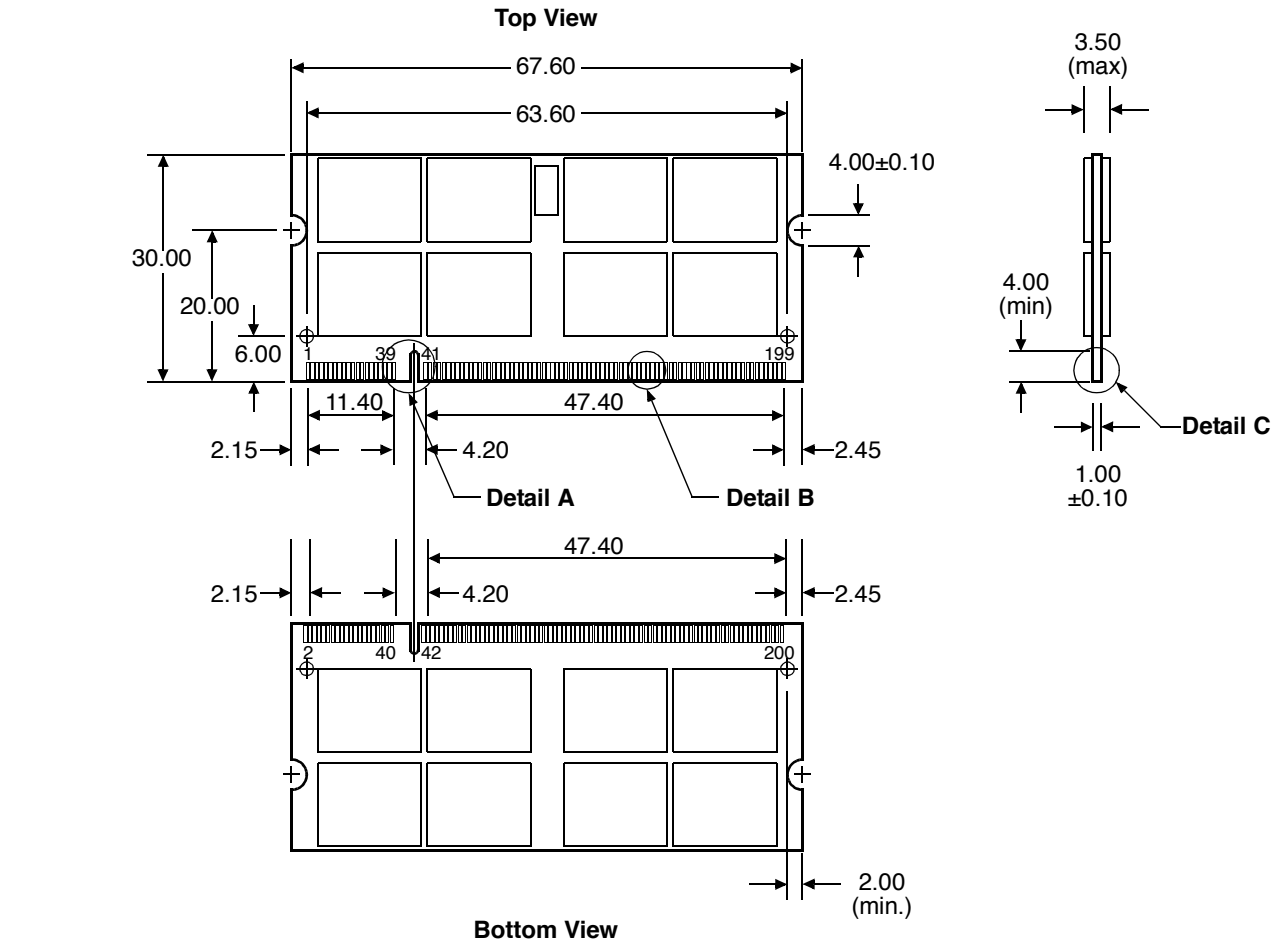

**Notes:**

1. Ax, BAx, RAS#, CAS#, WE# resistors: 10Ω±5%.
2. CS0#, CS1#, CKE0, CKE1, ODT0, ODT1 resistors: 3Ω±5%.

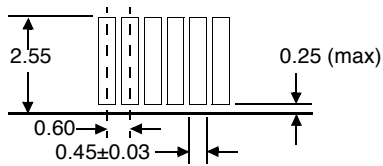


**Physical Dimensions**

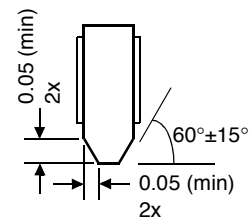
200-pin SO-DIMM Module



**Detail A:** Position of Voltage Notch



**Detail B:** Edge Connector



**Detail C**

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)





**Serial Presence Detect Table**

Byte No.	Byte Description	Speed	Value Supported	Hex Value
0	# of bytes written into serial memory at module manufacturer	All	128 Bytes	80h
1	Total # of bytes of SPD memory device	All	256 Bytes	08h
2	Fundamental memory type	All	SDRAM DDR2	08h
3	# of row address on this assembly	All	15	0Fh
4	# of column address on this assembly	All	10	0Ah
5	# of Ranks, Package and Height	All	2, Planar, 30.00mm	61h
6	Data width of this assembly	All	64	40h
7	Reserved	All	-	00h
8	Voltage interface standard of this assembly	All	SSTL_18	05h
9	SDRAM cycle time @ CAS latency of X	-DB -DG -IL -IR/KF	5.0ns 3.75ns 3.0ns 2.5ns	50h 3Dh 30h 25h
10	SDRAM access time @ CAS latency of X	-DB -DG -IL -IR/KF	0.60ns 0.50ns 0.45ns 0.40ns	60h 50h 45h 40h
11	DIMM configuration type	All	Non-ECC	00h
12	Refresh rate & type	All	SR, 7.8	82h
13	Primary SDRAM width	All	8	08h
14	Error checking SDRAM width	All	-	00h
15	Reserved	All	-	00h
16	SDRAM device attributes: Burst lengths supported	All	4, 8	0Ch
17	SDRAM device attributes: # of banks on SDRAM device	All	8	08h
18	SDRAM device attributes: CAS latency	-DB/DG -IL/IR -KF	3.0, 4.0 4.0, 5.0 5.0, 6.0	18h 30h 60h
19	DIMM Mechanical Characteristics	All	3.50mm	01h
20	DIMM type information	All	SO-DIMM	04h
21	SDRAM module attributes	All	None	00h
22	SDRAM device attributes: General	All	Weak Driver, 50Ω ODT	03h

**Serial Presence Detect Table (Contd.)**

Byte No.	Byte Description	Speed	Value Supported	Hex Value
23	SDRAM cycle time @ CAS latency of X-1	-DB/DG -IL/IR -KF	5.0ns 3.75ns 3.0ns	50h 3Dh 30h
24	SDRAM access time @ CAS latency of X-1	-DB/DG -IL/IR -KF	0.60ns 0.50ns 0.45ns	60h 50h 45h
25	SDRAM cycle time @ CAS latency of X-2	All	-	00h
26	SDRAM access time @ CAS latency of X-2	All	-	00h
27	Minimum row precharge time (=tRP)	-DB/DG/IL/KF -IR	15ns 12.5ns	3Ch 32h
28	Minimum row active to row active delay (=tRRD)	All	7.5ns	1Eh
29	Minimum RAS to CAS delay (=tRCD)	-DB/DG/IL/KF -IR	15ns 12.5ns	3Ch 32h
30	Minimum activate precharge time (=tRAS)	-DB -DG/IL/IR/KF	40ns 45ns	28h 2Dh
31	Module row density	All	2GB	02h
32	Command and Address signal input setup time	-DB -DG -IL -IR/KF	0.35ns 0.25ns 0.20ns 0.17ns	35h 25h 20h 17h
33	Command and Address signal input hold time	-DB -DG -IL -IR/KF	0.47ns 0.37ns 0.27ns 0.25ns	47h 37h 27h 25h
34	Data signal input setup time	-DB -DG/IL -IR/KF	0.15ns 0.10ns 0.05ns	15h 10h 05h
35	Data signal input hold time	-DB -DG -IL -IR/KF	0.27ns 0.22ns 0.17ns 0.12ns	27h 22h 17h 12h
36	Write recovery time (=tWR)	All	15ns	3Ch
37	Internal write to read command delay (=tWTR)	-DB -DG/IL/IR/KF	10.0ns 7.5ns	28h 1Eh
38	Internal read to precharge delay (=tRTP)	All	7.5ns	1Eh

**Serial Presence Detect Table (Contd.)**

Byte No.	Byte Description	Speed	Value Supported	Hex Value
39	Memory Analysis Probe Characteristics	All	-	00h
40	Extension of tRC and tRFC	-DB/DG/IL/KF -IR	- Extension of tRC	00h 30h
41	Device Minimum activate/auto-refresh time (=tRC)	-DB -DG/IL/KF -IR	55ns 60ns 57.5ns	37h 3Ch 39h
42	Device Minimum auto-refresh to active/ auto-refresh time (=tRFC)	All	195ns	C3h
43	Maximum device cycle time (=tCK max)	All	8ns	80h
44	Device DQS-DQ skew for DQS and asso- ciated DQ signals (=tDQSQ max)	-DB -DG -IL -IR/KF	0.35ns 0.30ns 0.24ns 0.20ns	23h 1Eh 18h 14h
45	Device read data hold skew factor (=tQHS)	-DB -DG -IL -IR/KF	0.45ns 0.40ns 0.34ns 0.30ns	2Dh 28h 22h 1Eh
46	PLL relock time	All	-	00h
47~61	Reserved	All	-	00h
62	SPD data revision code	All	1.3	13h
63	Checksum for bytes 0~62	-DB -DG -IL -IR -KF		44h EDh 9Eh 84h 83h
64	Manufacturer JEDEC ID code	All	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	All	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	All	Not Used	00h
72	Manufacturing location	All	See Note 2	01h
73~90	Manufacturer part #	-DB -DG -IL -IR -KF	SG564568FG8NWDB SG564568FG8NWDG SG564568FG8NWIL SG564568FG8NWIR SG564568FG8NWKF	P. No

**Serial Presence Detect Table (Contd.)**

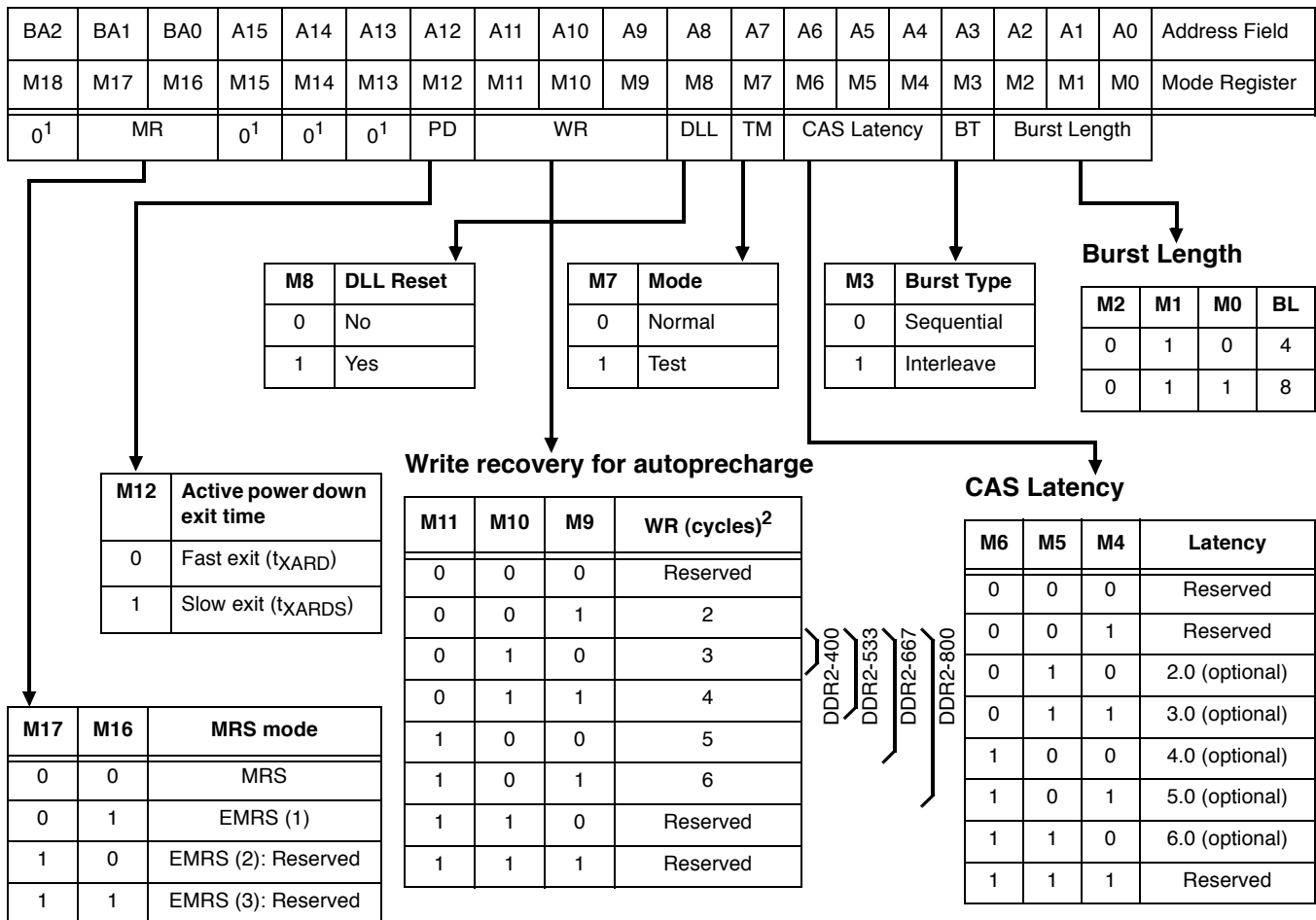
Byte No.	Byte Description	Speed	Value Supported	Hex Value
91	Manufacturer revision code	All	Rev. 0	00h
92	.....Manufacturer revision code	All	None	00h
93	Manufacturing data (Year)	All	Date	Date
94	Manufacturing data (Week)	All	Date	Date
95~98	Assembly serial #	All	Serial Number	S. No
99~125	Manufacturer specific data	All	SMART Modular Technologies	
126~255	Unused storage locations	All	-	00h

**Note:**

- X represents the maximum CAS Latency.  
 For DDR2-400-333, X = CL 4.0  
 For DDR2-533-444, X = CL 4.0  
 For DDR2-667-555, X = CL 5.0  
 For DDR2-800-555, X = CL 5.0  
 For DDR2-800-666, X = CL 6.0
- Manufacturing Location:  
 00h - Undefined,  
 01h - Fremont, USA,  
 02h - Aguada, Puerto Rico,  
 03h - East Kilbride, Scotland,  
 04h - Penang, Malaysia,  
 05h - Bangalore, India,  
 06h - Sao Paulo, Brazil,  
 07h - Aguadilla, Puerto Rico,  
 08h - Mayaguez, Puerto Rico,  
 09h - Santo Domingo, Dominican Republic,  
 0Ah - Dongguan, China,

## Mode Register Table Definition

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset,  $t_{WR}$  and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time ( $t_{MRD}$ ) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0~A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4~A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time  $t_{WR}$  is defined by A9~A11.



Notes:

- BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
- WR min is determined by  $t_{CK}$  max and WR max is determined by  $t_{CK}$  min. WR in clock cycles is calculated by dividing  $t_{WR}$  (in ns) by  $t_{CK}$  (in ns) and rounding up to the next integer. The mode register must be programmed to this value.

## Extended Mode Register Table Definition

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT ( $R_{TT}$ ), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT enable/disable. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time  $t_{MRD}$  before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

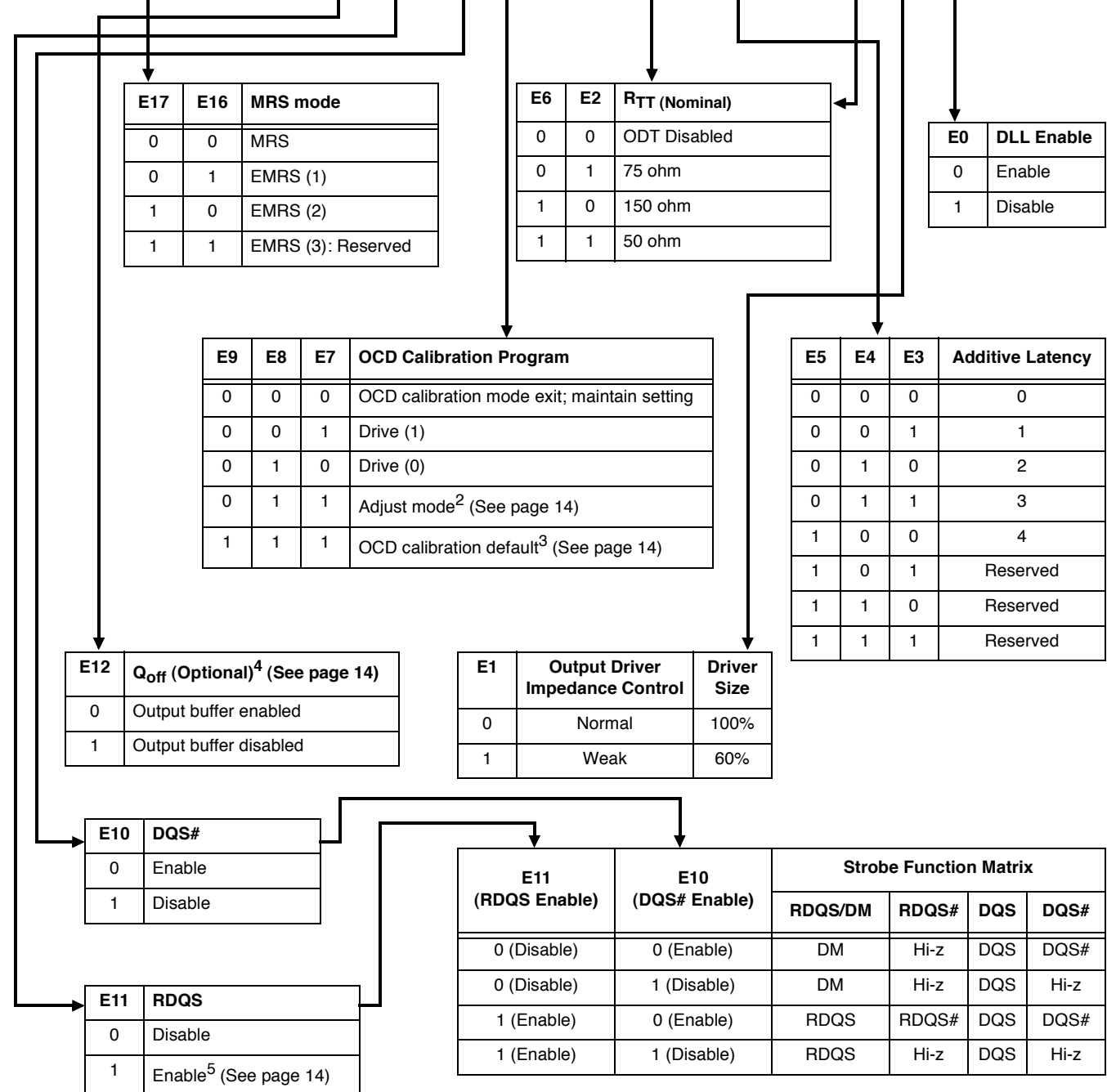
### Notes:

1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. When the adjust mode of the OCD Calibration Program is issued, AL from previously set value must be applied.
3. After setting the OCD Calibration Program to default, OCD mode needs to be exited by setting A9-A7 to 000.
4. Outputs disabled - DQs, DQSs, DQS#s, RDQSs, RDQS#s. This feature is used in conjunction with DIMM  $I_{DDQ}$  measurements when  $I_{DDQ}$  is not desired to be included.
5. If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.



**Extended Mode Register Table**

BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	Extended Mode Register
0 <sup>1</sup>	EMR		0 <sup>1</sup>	0 <sup>1</sup>	0 <sup>1</sup>	Q <sub>off</sub>	RDQS	DQS#	OCD Program			R <sub>TT</sub>	AL		R <sub>TT</sub>	D.I.C	DLL		



## Commands

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Function	CKE		CS#	RAS#	CAS#	WE#	BA0~ BA <sub>n</sub> <sup>9</sup>	An <sup>8</sup> ~A11	A10	A9~A0	Notes
	Previous cycle	Current cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Refresh	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge All Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

### Notes:

- All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.
- Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
- Burst reads or writes at BL = 4 cannot be terminated or interrupted.
- The Power Down Mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
- "X" means "H or L (but a defined logic level)".
- Self Refresh Exit is asynchronous.
- An = A12 for 256Mb, A13 for 512Mb & 1Gb, A14 for 2Gb.
- BAn = BA1 for up to 512Mb, BA2 for 1Gb & 2Gb.



## DC Characteristics

### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Notes
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-1.0 ~ 2.3	V	
Voltage on $V_{DDQ}$ relative to $V_{SS}$	$V_{DDQ}$	-0.5 ~ 2.3	V	
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 ~ 2.3	V	
Voltage on $V_{DDSPD}$ relative to $V_{SS}$	$V_{DDSPD}$	1.7 ~ 3.6	V	
Operating Temperature (Ambient)	$T_{OPR}$	0 to +65	°C	
Operating Temperature (Case)	$T_{CASE}$	0 to +85	°C	1, 2
Storage Temperature	$T_{STG}$	-55 to +100	°C	

#### Notes:

- It is possible to operate the DRAM, Register & PLL up to 95°C.
- Above 85°C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9\mu s$ .

### Recommended DC Operating Conditions ( $T_A = 0$ to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	
I/O Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V	
I/O Reference Voltage	$V_{REF}$	$0.49 \cdot V_{DDQ}$	$0.50 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	mV	1, 2
I/O Termination Voltage	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$	V	3
SPD Voltage	$V_{DDSPD}$	1.7	-	3.6	V	
Input High Voltage	$V_{IH(DC)}$	$V_{REF} + 0.125$	-	$V_{DDQ} + 0.3$	V	
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	$V_{REF} - 0.125$	V	
Input Voltage Level, CK/CK#	$V_{IN(DC)}$	-0.3	-	$V_{DDQ} + 0.3$	V	
Input Differential Voltage, CK/CK#	$V_{ID(DC)}$	0.25	-	$V_{DDQ} + 0.6$	V	
Ground	$V_{SS}$	0	0	0	V	

#### Notes:

- $V_{REF}$  is expected to track variation in  $V_{DDQ}$ .
- Peak to peak noise (non-common mode) on  $V_{REF}$  may not exceed  $\pm 1\%$  of the DC value. Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\%$  of  $V_{REF}$  (DC). This measurement is to be taken at the nearest  $V_{REF}$  bypass capacitor.
- $V_{TT}$  is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of  $V_{REF}$ .

**Capacitance**
**(V<sub>DD</sub> = 1.8V±0.1V, T<sub>Case</sub> = +25°C)**

Parameter	Symbol	Min	Max	Unit
Input Capacitance (CKn, CKn#)	C <sub>CK</sub>	8.0	16.0	pF
Input Capacitance delta (CKn, CKn#)	C <sub>DCK</sub>	-	2.0	pF
Input Capacitance (all other input-only pins)	C <sub>I</sub>	16.0	32.0	pF
Input Capacitance delta (all other input-only pins)	C <sub>DI</sub>	-	4.0	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#)	C <sub>IO1</sub>	5.0	8.0	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#)	C <sub>IO2</sub>	5.0	7.0	pF
Input/Output Capacitance delta (DQ, DM, DQS, DQS#)	C <sub>DIO</sub>	-	1.0	pF

**Notes:**

1. C<sub>IO1</sub> is for DDR2-400 and DDR2-533.
2. C<sub>IO2</sub> is for DDR2-667 and DDR2-800.

**AC Operating Conditions**
**(V<sub>DD</sub> = 1.8V±0.1V, V<sub>SS</sub> = 0V)**

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	V <sub>IH(AC)</sub>	V <sub>REF</sub> + 0.250	-	V	1, 2
Input Low Logic Voltage	V <sub>IL(AC)</sub>	-	V <sub>REF</sub> - 0.250	V	1, 2
Input differential voltage, CK and CK# inputs	V <sub>ID(AC)</sub>	0.5	V <sub>DDQ</sub> + 0.6	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	V <sub>IX(AC)</sub>	0.5*V <sub>DDQ</sub> - 0.175	0.5*V <sub>DDQ</sub> + 0.175	V	1, 2, 3
AC differential crossing point voltage	V <sub>OX(AC)</sub>	0.5*V <sub>DDQ</sub> - 0.125	0.5*V <sub>DDQ</sub> + 0.125	V	3

**Notes:**

1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until V<sub>REF</sub> stabilizes.
3. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of V<sub>IX</sub>/V<sub>OX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the DC level of the same.

**ODT DC Electrical Characteristics**

Parameter	Symbol	Min	Nom	Max	Unit	Notes
R <sub>TT</sub> effective impedance value for 75Ω setting EMR (A6, A2) = 0, 1	R <sub>TT1</sub> (EFF)	60	75	90	Ω	1
R <sub>TT</sub> effective impedance value for 150Ω setting EMR (A6, A2) = 1, 0	R <sub>TT2</sub> (EFF)	120	150	180	Ω	1
R <sub>TT</sub> effective impedance value for 50Ω setting EMR (A6, A2) = 1, 1	R <sub>TT3</sub> (EFF)	40	50	60	Ω	1
Deviation of VM with respect to V <sub>DDQ</sub> /2	ΔVM	-6		+6	%	2

**Notes:**

1. R<sub>TT1</sub>(EFF) and R<sub>TT2</sub>(EFF) are determined by applying V<sub>IH(AC)</sub> and V<sub>IL(AC)</sub> to pin under test separately, then

$$\text{measure current } I(V_{IH(AC)}) \text{ and } I(V_{IL(AC)}) \text{ respectively. } R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$$

2. Measured voltage (VM) at tested pin with no load.

$$\Delta VM = \left( \frac{2 \times VM}{V_{DDQ}} - 1 \right) \times 100 \%$$

**Output DC Current Drive**

Parameter	Symbol	Min	Max	Unit	Notes
Output Minimum Source DC Current	I <sub>OH</sub>	-13.4	-	mA	1, 3, 4
Output Minimum Sink DC Current	I <sub>OL</sub>	13.4	-	mA	2, 3, 4

**Notes:**

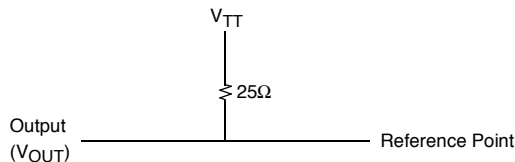
1. For I<sub>OH</sub> (DC); V<sub>DDQ</sub> = 1.7V, V<sub>OUT</sub> = 1420mV. (V<sub>OUT</sub> - V<sub>DDQ</sub>)/I<sub>OH</sub> must be less than 21Ω for values of V<sub>OUT</sub> between V<sub>DDQ</sub> and V<sub>DDQ</sub> - 280mV.
2. For I<sub>OL</sub> (DC); V<sub>DDQ</sub> = 1.7V, V<sub>OUT</sub> = 280mV. V<sub>OUT</sub>/I<sub>OL</sub> must be less than 21Ω for values of V<sub>OUT</sub> between 0V and 280mV.
3. The DC value of V<sub>REF</sub> applied to the receiving device is set to V<sub>TT</sub>.
4. The values of I<sub>OH</sub> (DC) and I<sub>OL</sub> (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V<sub>IH</sub> min plus a noise margin and V<sub>IL</sub> max minus a noise margin are delivered to an SSTL\_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

**OCD Default Output Characteristics**  
 ( $V_{DD} = 1.8V \pm 0.1V$ ,  $V_{SS} = 0V$ ,  $T_A = 0$  to  $+65^\circ C$ )

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Output Impedance		12.6	18	23.4	$\Omega$	1, 2
Pull-up and Pull-down mismatch		0		4	$\Omega$	1, 2, 3
Output Slew Rate	$S_{OUT}$	1.5		5	V/ns	1, 4, 5, 7
Output Step Size for Calibration		0		1.5	$\Omega$	6

**Notes:**

1. Absolute specifications:  $0^\circ C \leq T_{case} \leq +85^\circ C$ ;  $V_{DDQ} = +1.8V \pm 0.1V$ ,  $V_{DD} = +1.8V \pm 0.1V$ .
2. Impedance measurement condition for output source DC current:  $V_{DDQ} = 1.7V$ ;  $V_{OUT} = 1420mV$ ;  $(V_{OUT} - V_{DDQ})/I_{OH}$  must be less than  $23.4\Omega$  for values of  $V_{OUT}$  between  $V_{DDQ}$  and  $V_{DDQ} - 280mV$ . Impedance measurement condition for output sink DC current:  $V_{DDQ} = 1.7V$ ;  $V_{OUT} = 280mV$ ;  $V_{OUT}/I_{OL}$  must be less than  $23.4\Omega$  for values of  $V_{OUT}$  between  $0V$  and  $280mV$ .
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between  $V_{TT} - 250mV$  and  $V_{TT} + 250mV$  for single ended signals. For differential signals output slew rate is measured between  $DQS - DQS\# = -500mV$  and  $DQS\# - DQS = +500mV$ . Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from  $V_{IL}$  (DC) max to  $V_{IH}$  (DC) min is equal to or greater than the slew rate as measured from  $V_{IL}$  (AC) max to  $V_{IH}$  (AC) min. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near  $18\Omega$  at nominal conditions across all process and represent only the DRAM uncertainty.
7. Timing skew due to DRAM output slew rate mis-match between  $DQS/DQS\#$  and associated  $DQs$  is included in  $t_{DQSQ}$  and  $t_{QHS}$  specification.

**Output Slew Rate Load Diagram**


**IDD Specification Parameters and Test Conditions**  
**( $V_{DD} = 1.8V \pm 0.1V$ ,  $V_{SS} = 0V$ ,  $T_A = 0$  to  $+65^\circ C$ )**

Symbol	Parameter	5.0ns CL 3.0	3.75ns CL 4.0	3.0ns CL 5.0	2.5ns CL 5.0	2.5ns CL 6.0	Unit	
IDD0	<b>Operating one bank active–precharge current;</b> $t_{CK} = t_{CK(IDD)}$ , $t_{RC} = t_{RC(IDD)}$ , $t_{RAS} = t_{RASmin(IDD)}$ ; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1280	1280	1280	1400	1400	mA	
IDD1	<b>Operating one bank active–read–precharge current;</b> $I_{OUT} = 0mA$ ; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$ , $t_{RC} = t_{RC(IDD)}$ , $t_{RAS} = t_{RASmin(IDD)}$ , $t_{RCD} = t_{RCD(IDD)}$ ; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	1360	1360	1360	1480	1480	mA	
IDD2P	<b>Precharge power–down current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	192	192	192	192	192	mA	
IDD2Q	<b>Precharge quiet standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	720	720	720	800	800	mA	
IDD2N	<b>Precharge standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	800	800	800	880	880	mA	
IDD3P	<b>Active power–down current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	840	840	840	920	920	mA
		Slow PDN Exit MRS(12) = 1	704	704	704	784	784	mA
IDD3N	<b>Active standby current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ , $t_{RAS} = t_{RASmax(IDD)}$ , $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	1120	1120	1120	1280	1280	mA	
IDD4W	<b>Operating burst write current;</b> All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$ , $t_{RAS} = t_{RASmax(IDD)}$ , $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2160	2160	2160	2560	2560	mA	
IDD4R	<b>Operating burst read current;</b> All banks open, Continuous burst reads, $I_{OUT} = 0mA$ ; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$ , $t_{RAS} = t_{RASmax(IDD)}$ , $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	2040	2040	2040	2400	2400	mA	
IDD5B	<b>Burst refresh current;</b> $t_{CK} = t_{CK(IDD)}$ ; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	2320	2320	2320	2480	2480	mA	
IDD6	<b>Self refresh current;</b> CK and CS# at 0V; CKE $\leq 0.2V$ ; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	240	240	240	240	240	mA	
IDD7	<b>Operating bank interleave read current;</b> All bank interleaving reads, $I_{OUT} = 0mA$ ; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$ ; $t_{CK} = t_{CK(IDD)}$ , $t_{RC} = t_{RC(IDD)}$ , $t_{RRD} = t_{RRD(IDD)}$ , $t_{RCD} = 1 * t_{CK(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTS; Data pattern is same as IDD4R	2800	2800	2800	3080	3080	mA	

**IDD Specification Parameters and Test Conditions (Contd.)**
**Notes:**

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of ERMS bits 10 and 11.
5. Definitions for IDD
  - LOW =  $V_{in} \leq V_{IL(AC)}(max)$
  - HIGH =  $V_{in} \geq V_{IH(AC)}(min)$
  - STABLE = inputs stable at a HIGH or LOW level
  - FLOATING = inputs at  $V_{REF} = V_{DDQ}/2$
  - SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks of strobes.

**IDD Testing Parameters**

	<b>DDR2-400</b>	<b>DDR2-533</b>	<b>DDR2-667</b>	<b>DDR2-800</b>	<b>DDR2-800</b>	
<b>Parameter</b>	<b>3-3-3</b>	<b>4-4-4</b>	<b>5-5-5</b>	<b>5-5-5</b>	<b>6-6-6</b>	<b>Units</b>
CL(IDD)	3	4	5	5	6	t <sub>CK</sub>
t <sub>RCD</sub> (IDD)	15	15	15	12.5	15	ns
t <sub>RC</sub> (IDD)	55	60	60	57.5	60	ns
t <sub>RRD</sub> (IDD)	7.5	7.5	7.5	7.5	7.5	ns
t <sub>CK</sub> (IDD)	5	3.75	3	2.5	2.5	ns
t <sub>RASmin</sub> (IDD)	40	45	45	45	45	ns
t <sub>RASmax</sub> (IDD)	70000	70000	70000	70000	70000	ns
t <sub>RP</sub> (IDD)	15	15	15	12.5	15	ns
t <sub>RFC</sub> (IDD)	195	195	195	195	195	ns



**Device AC Operating Conditions**

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400-333		3.75ns @ CL 4.0 DDR2-533-444		3.0ns @ CL 5.0 DDR2-667-555		2.5ns @ CL 5.0 DDR2-800-555		2.5ns @ CL 5.0 DDR2-800-666		Unit	Notes	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
Clock cycle time	CL=6.0	t <sub>CK</sub>	-	-	-	-	-	-	-	2500	8000	ps	12, 20	
	CL=5.0	t <sub>CK</sub>	-	-	-	-	3000	8000	2500	8000	3000	8000	ps	12, 20
	CL=4.0	t <sub>CK</sub>	5000	8000	3750	8000	3750	8000	3750	8000	-	-	ps	12, 20
	CL=3.0	t <sub>CK</sub>	5000	8000	5000	8000	-	-	-	-	-	-	ps	12, 20
Clock high-level width	t <sub>CH</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	14	
Clock low-level width	t <sub>CL</sub>	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>	14	
Clock half period	t <sub>HP</sub>	Min (t <sub>CL</sub> , t <sub>CH</sub> )	-	Min (t <sub>CL</sub> , t <sub>CH</sub> )	-	Min (t <sub>CL</sub> , t <sub>CH</sub> )	-	Min (t <sub>CL</sub> , t <sub>CH</sub> )	-	Min (t <sub>CL</sub> , t <sub>CH</sub> )	-	ps	15	
DQ output access time from CK/CK#	CL=6.0	t <sub>AC</sub>	-	-	-	-	-	-	-	-400	+400	ps		
	CL=5.0	t <sub>AC</sub>	-	-	-	-	-450	+450	-400	+400	-450	+450	ps	
	CL=4.0	t <sub>AC</sub>	-600	+600	-500	+500	-450	+450	-500	+500	-	-	ps	
	CL=3.0	t <sub>AC</sub>	-600	+600	-500	+500	-	-	-	-	-	-	ps	
Data-out high-impedance window from CK/CK#	t <sub>HZ</sub>	-	t <sub>AC</sub> (max)	-	t <sub>AC</sub> (max)	-	t <sub>AC</sub> (max)	-	t <sub>AC</sub> (max)	-	t <sub>AC</sub> (max)	ps	4, 5	
Data-out low-impedance window from CK/CK#	t <sub>LZ</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	t <sub>AC</sub> (min)	t <sub>AC</sub> (max)	ps	4, 6	
DQ & DM input setup time relative to DQS	t <sub>DS</sub>	150	-	100	-	100	-	50	-	50	-	ps	3, 11, 17	
DQ & DM input hold time relative to DQS	t <sub>DH</sub>	275	-	225	-	175	-	125	-	125	-	ps	3, 11, 17	
DQ & DM input pulse width (for each input)	t <sub>DIPW</sub>	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	t <sub>CK</sub>		
Data hold skew factor	t <sub>QHS</sub>	-	450	-	400	-	340	-	300	-	300	ps		
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t <sub>QH</sub>	t <sub>HP</sub> - t <sub>QHS</sub>	-	t <sub>HP</sub> - t <sub>QHS</sub>	-	t <sub>HP</sub> - t <sub>QHS</sub>	-	t <sub>HP</sub> - t <sub>QHS</sub>	-	t <sub>HP</sub> - t <sub>QHS</sub>	-	ps	11,13	
DQS input high pulse width	t <sub>DQSH</sub>	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	t <sub>CK</sub>		
DQS input low pulse width	t <sub>DQSL</sub>	0.35	-	0.35	-	0.35	-	0.35	-	0.35	-	t <sub>CK</sub>		
DQS output access time from CK/CK#	t <sub>DQSCK</sub>	-500	+500	-450	+450	-400	+400	-350	+350	-350	+350	ps		
DQS falling edge to CK rising - setup time	t <sub>DSS</sub>	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t <sub>CK</sub>		
DQS falling edge from CK rising - hold time	t <sub>DSH</sub>	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t <sub>CK</sub>		
DQS-DQ skew, DQS to last DQ valid, per group, per access	t <sub>DQSQ</sub>	-	350	-	300	-	240	-	200	-	200	ps	11,13	



**Device AC Operating Conditions (Contd.)**

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400-333		3.75ns @ CL 4.0 DDR2-533-444		3.0ns @ CL 5.0 DDR2-667-555		2.5ns @ CL 5.0 DDR2-800-555		2.5ns @ CL 5.0 DDR2-800-666		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS read preamble	t <sub>RPRE</sub>	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>	18
DQS read postamble	t <sub>RPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
DQS write preamble setup time	t <sub>WPRES</sub>	0	-	0	-	0	-	0	-	0	-	ps	8, 9
DQS write preamble	t <sub>WPRE</sub>	0.25	-	0.25	-	0.35	-	0.35	-	0.35	-	t <sub>CK</sub>	
DQS write postamble	t <sub>WPST</sub>	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	7
Write command to first DQS latching transition	t <sub>DQSS</sub>	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t <sub>CK</sub>	
Address & control input pulse width for each input	t <sub>IPW</sub>	0.6	-	0.6	-	0.6	-	0.6	-	0.6	-	t <sub>CK</sub>	
Address and control input setup time	t <sub>IS</sub>	350	-	250	-	200	-	175	-	175	-	ps	2, 17
Address and control input hold time	t <sub>IH</sub>	475	-	375	-	275	-	250	-	250	-	ps	2, 17
CAS# to CAS# command delay	t <sub>CCD</sub>	2	-	2	-	2	-	2	-	2	-	t <sub>CK</sub>	
OCD Drive mode delay	t <sub>OIT</sub>	0	12	0	12	0	12	0	12	0	12	ns	
CKE low to CK, CK# uncertainty	t <sub>DELAY</sub>	5.825	5.825	4.375	4.375	3.475	3.475	2.925	2.925	2.925	2.925	ns	24
ACTIVE to ACTIVE (same bank) command	t <sub>RC</sub>	55	-	60	-	60	-	57.5	-	60	-	t <sub>CK</sub>	
ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	t <sub>CK</sub>	
ACTIVE to READ or WRITE delay	t <sub>RCD</sub>	15	-	15	-	15	-	12.5	-	15	-	ps	11,13
ACTIVE to PRE-CHARGE command	t <sub>RAS</sub>	40	70000	45	70000	45	70000	45	70000	45	70000	t <sub>CK</sub>	18
Internal READ to pre-charge command delay	t <sub>RTP</sub>	7.5	-	7.5	-	7.5	-	7.5	-	7.5	-	t <sub>CK</sub>	
Write recovery time	t <sub>WR</sub>	15	-	15	-	15	-	15	-	15	-	ps	8, 9
Auto precharge write recovery + Precharge time	t <sub>DAL</sub>	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>WR</sub> + t <sub>RP</sub>	-	t <sub>CK</sub>	
Internal WRITE to READ command delay	t <sub>WTR</sub>	10	-	7.5	-	7.5	-	7.5	-	7.5	-	t <sub>CK</sub>	7
PRECHARGE command period	t <sub>RP</sub>	15	-	15	-	15	-	12.5	-	15	-	t <sub>CK</sub>	
LOAD MODE command cycle time	t <sub>MRD</sub>	2	-	2	-	2	-	2	-	2	-	t <sub>CK</sub>	





**Device AC Operating Conditions (Contd.)**

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400-333		3.75ns @ CL 4.0 DDR2-533-444		3.0ns @ CL 5.0 DDR2-667-555		2.5ns @ CL 5.0 DDR2-800-555		2.5ns @ CL 5.0 DDR2-800-666		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
REFRESH to REFRESH command interval	t <sub>RFC</sub>	195	-	195	-	195	-	195	-	195	-	ps	2, 17
Average periodic refresh Interval	t <sub>REFI</sub>	-	7.8	-	7.8	-	7.8	-	7.8	-	7.8	ps	2, 17
Exit self refresh to non-READ command	t <sub>XSNR</sub>	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	t <sub>RFC</sub> (min) + 10	-	t <sub>CK</sub>	
Exit self refresh to READ command	t <sub>XSRD</sub>	200	-	200	-	200	-	200	-	200	-	ns	
ODT turn-on delay	t <sub>AOND</sub>	2	2	2	2	2	2	2	2	2	2	t <sub>CK</sub>	
ODT turn-on	t <sub>AON</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 700	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 700	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 700	t <sub>CK</sub>	
ODT turn-off delay	t <sub>AOFD</sub>	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	ps	11, 13
ODT turn-off	t <sub>AOF</sub>	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	t <sub>AC</sub> (min)	t <sub>AC</sub> (max) + 600	t <sub>CK</sub>	18
ODT turn-on (power-down mode)	t <sub>AONPD</sub>	t <sub>AC</sub> (min) + 2000	2*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>CK</sub>	
ODT turn-off (power-down mode)	t <sub>AOFPD</sub>	t <sub>AC</sub> (min) + 2000	2.5*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2.5*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2.5*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2.5*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	t <sub>AC</sub> (min) + 2000	2.5*t <sub>CK</sub> + t <sub>AC</sub> (max) + 1000	ps	8, 9
ODT to power-down entry latency	t <sub>ANPD</sub>	3	-	3	-	3	-	3	-	3	-	t <sub>CK</sub>	
ODT power-down exit latency	t <sub>AXPD</sub>	8	-	8	-	8	-	8	-	8	-	t <sub>CK</sub>	7
Exit active power-down to READ command, MR[bit12=0]	t <sub>XARD</sub>	2	-	2	-	2	-	2	-	2	-	t <sub>CK</sub>	
Exit active power-down to READ command, MR[bit12=1]	t <sub>XARDS</sub>	6 - AL	-	6 - AL	-	7 - AL	-	8 - AL	-	8 - AL	-	t <sub>CK</sub>	
Exit precharge power down to any non-read command	t <sub>XP</sub>	2	-	2	-	2	-	2	-	2	-	ps	2, 17
CKE minimum pulse width (high and low pulse width)	t <sub>CKE</sub>	3	-	3	-	3	-	3	-	3	-	ps	2, 17



**Notes:**

1. The AC and DC input level specifications are as defined in the SSTL\_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level.
2. Command/Address minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of CK/CK#.  $t_{1S}$  timing is referenced to  $V_{IH(AC)}$  for a rising signal and  $V_{IL(AC)}$  for a falling signal.  $t_{1H}$  timing is referenced to  $V_{IH(DC)}$  for a rising signal and  $V_{IL(DC)}$  for a falling signal. Derating values for Command/Address input signal slew rates < 1.0V/ns are TBD.
3. Data minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of DQS/DQS# if differential strobe feature is enabled.  $t_{DS}$  timing is referenced to  $V_{IH(AC)}$  for a rising signal and  $V_{IL(AC)}$  for a falling signal.  $t_{DH}$  timing is referenced to  $V_{IH(DC)}$  for a rising signal and  $V_{IL(DC)}$  for a falling signal. Derating values for Data input signal slew rates < 1.0V/ns are TBD.
4.  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving ( $t_{HZ}$ ) or begins driving ( $t_{LZ}$ ).
5. This maximum value is derived from the reference test load.  $t_{HZ(MAX)}$  will prevail over a  $t_{DQSCK(MAX)} + t_{RPST(MAX)}$  condition.
6.  $t_{LZ(MIN)}$  will prevail over a  $t_{DQSCK(MIN)} + t_{RPRE(MAX)}$  condition.
7. The intent of the Don't Care state after completion of the postamble is the DQS driven signal should be high, low or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high [above  $V_{IHDC(MIN)}$ ] then it must not transition low (below  $V_{IHDC}$ ) prior to  $t_{DQSH(min)}$ .
8. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
9. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during his time depending on  $t_{DQSS}$ .
10. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 $\mu$ s. However, an REFRESH command must be asserted at least once every 70.3 $\mu$ s or  $t_{RFC(MAX)}$ ; issuing more than eight REFRESH commands back to back at  $t_{RFC(min)}$  is not allowed.
11. Each byte lane has a corresponding DQS.
12. CK and CK# input slew rate must be  $\geq 1$  V/ns ( $\geq 2$  V/ns if measured differentially).
13. The data valid window is derived by achieving other specifications:  $t_{HP}$ , ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
14.  $\text{Min}(t_{CL}, t_{CH})$  refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for  $t_{CL}$  and  $t_{CH}$ ).
15.  $t_{HP(MIN)}$  is the lesser of  $t_{CL}$  minimum and  $t_{CH}$  minimum actually applied to the device CK and CK# inputs.
16. READs and WRITEs with no auto precharge are allowed to be issued before  $t_{RAS(MIN)}$  is satisfied since  $t_{RAS}$  lockout feature is supported in DDR2 SDRAM.
17.  $V_{IL}/V_{IH}$  DDR2 overshoot/undershoot. Refer to 256MB, 512MB, or 1GB DDR2 SDRAM component data sheet for more detailed information.
18.  $t_{DAL} = (n_{WR}) + (t_{RP}/t_{CK})$ : For each of the terms above, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period;  $n_{WR}$  refers to the  $t_{WR}$  parameter stored in the MR[11,10,9].
19. This is a minimum requirement. Minimum READ to internal PRECHARGE timing is  $AL + BL/2$  providing the  $t_{RTP}$  and  $t_{RAS(MIN)}$  have been satisfied. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until  $t_{RAS(MIN)}$  has been satisfied.
20. Operating frequency is only allowed to change during self refresh mode or precharge power-down mode. Anytime the operating frequency is changed, not including jitter, the DLL is required to be reset followed by 200 clock cycles.
21. ODT turn-on time  $t_{AON(MIN)}$  is when the device leaves high impedance and ODT resistance begins to turn-on. ODT turn-on time  $t_{AON(MAX)}$  is when the resistance is fully on. Both are measured from  $t_{AOND}$ .
22. ODT turn-off time  $t_{AOF(MIN)}$  is when the device starts to turn-off ODT resistance. ODT turn-off time  $t_{AOF(MAX)}$  is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ .
23. This parameter has a two clock minimum requirement at any  $t_{CK}$ .
24.  $t_{DELAY}$  is calculated from  $t_{1S} + t_{CK} + t_{1H}$  so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system reset condition.

**Part Number Decode**

<u>S</u>	<u>G</u>	<u>5</u>	<u>64</u>	<u>12</u>	<u>8</u>	<u>F</u>	<u>G</u>	<u>8</u>	<u>N</u>	<u>Z</u>	<u>U</u>	<u>U</u>
1	2	3	4	5	6	7	8	9	10	11	12	13

- 1 SMART Modular Technologies**
- 2 Module Process Technology**  
G: Green Module (RoHS Compliant)
- 3 Product Category**  
5: SDRAM DIMM
- 4 Module Data Bus Width**  
64: x64
- 5 Module Address Depth**  
12: 512M
- 6 Device Data Width**  
8: x8
- 7 Special Device Feature**  
F: Standard FBGA (8 Bank SDRAM)
- 8 Technology**  
G: DDR2 SDRAM
- 9 Refresh/Power**  
8: 8K Refresh/Standard Power
- 10 Module Configuration**  
N: 200-pin SO-DIMM Unbuffered, Non-ECC
- 11 Device Physicals**  
Z: 2Gbit Device Based
- 12 CAS Latency**  
D: 3.0, 4.0  
I: 4.0, 5.0  
K: 5.0, 6.0
- 13 Cycle Time (Clock Speed)**  
B: 5.0ns (200MHz, PC2-3200, DDR2-400-333)  
G: 3.75ns (267MHz, PC2-4200, DDR2-533-444)  
L: 3.0ns (333MHz, PC2-5300, DDR2-667-555)  
R: 2.5ns (400MHz, PC2-6400, DDR2-800-555)  
F: 2.5ns (400MHz, PC2-6400, DDR2-800-666)

Note: "U" in the part number should be replaced by user specified option.

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