Ordering Information		
Part Numbers	**Description**	**Module Speed**
SG564568FG8NRDB	256Mx64 (2GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based (Stacked - two 128Mx8), DDR2-400-333, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-3200 @ CL 3.0
SG564568FG8NRDG	256Mx64 (2GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based (Stacked - two 128Mx8), DDR2-533-444, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-4200 @ CL 4.0
SG564568FG8NRIL	256Mx64 (2GB), DDR2, 200-pin SO-DIMM, Unbuffered, Non-ECC, 256Mx8 Based (Stacked - two 128Mx8), DDR2-667-555, 30.00mm, 22Ω DQ termination, Green Module (RoHS Compliant).	PC2-5300 @ CL 5.0

Revision History

- **May 30, 2006**
  Corrected the OCD Program in the EMRS on page 14.
  Changed the Ambient Operating temperature to 0 to +65°C on page 16.
  Added the Case Operating temperature on page 16.

- **September 9, 2005**
  Corrected the DLL Enable in the EMRS on page 14.

- **August 16, 2005**
  Removed Mating Connector from page 3 because the connector does not support stacked modules.

- **June 28, 2005**
  Changed datasheet part number from SG564568FG8NRDU to SG564568FG8NRUU because of the addition of a DDR2-667 part number with different CAS Latencies.
  Added SG564568FG8NRIL to the Ordering Information on page 1.

- **June 2, 2005**
  Corrected the position of the voltage notch on page 8.

- **May 23, 2005**
  Datasheet released.

2GByte (256Mx64) DDR2 SDRAM Module - 256Mx8 Based (Stacked - two 128Mx8) 200-pin SO-DIMM, Unbuffered, Non-ECC

Features

- Standard : JEDEC
- Configuration : Non-ECC
- Cycle Time : 5.0ns (DDR2-400)
  3.75ns (DDR2-533)
  3.0ns (DDR2-667)
- CAS# Latency : 3.0, 4.0 (DDR2-400/533)
  4.0, 5.0 (DDR2-667)
- Posted CAS#/Additive Latency (AL) : 0, 1.0, 2.0, 3.0 & 4.0
- Write Latency (WL) : Read (CAS#) Latency - 1
- Burst Length : 4, 8
- Burst Type : Sequential/Interleave
- No. of Internal Banks per SDRAM : 8
- Operating Voltage : 1.8V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 67.60mm x 30.00mm
- No. of sides : Double-sided

200-pin DDR2 SO-DIMM Pin List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{REF}	2	V_{SS}	51	DQS2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10/AP	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	RAS#	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	WE#	110	CS0#	159	DQ49	160	DQ53
11	DQS0#	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	CAS#	114	ODT0	163	NC	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	CS1#	116	A13	165	V_{SS}	166	CK1#
17	DQ2	18	V_{SS}	67	DM3	68	DQS3#	117	V_{DD}	118	V_{DD}	167	DQS6#	168	V_{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	DQS1#	30	CK0	79	CKE0	80	CKE1	129	DQS4#	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	CK0#	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	NC	84	A15 (NC)	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	BA2	86	A14 (NC)	135	DQ34	136	DQ39	185	DM7	186	DQS7#
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}

200-pin DDR2 SO-DIMM Pin List (Contd.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	DQS5#	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	DQS2#	50	NC	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DDSPD}	200	SA1

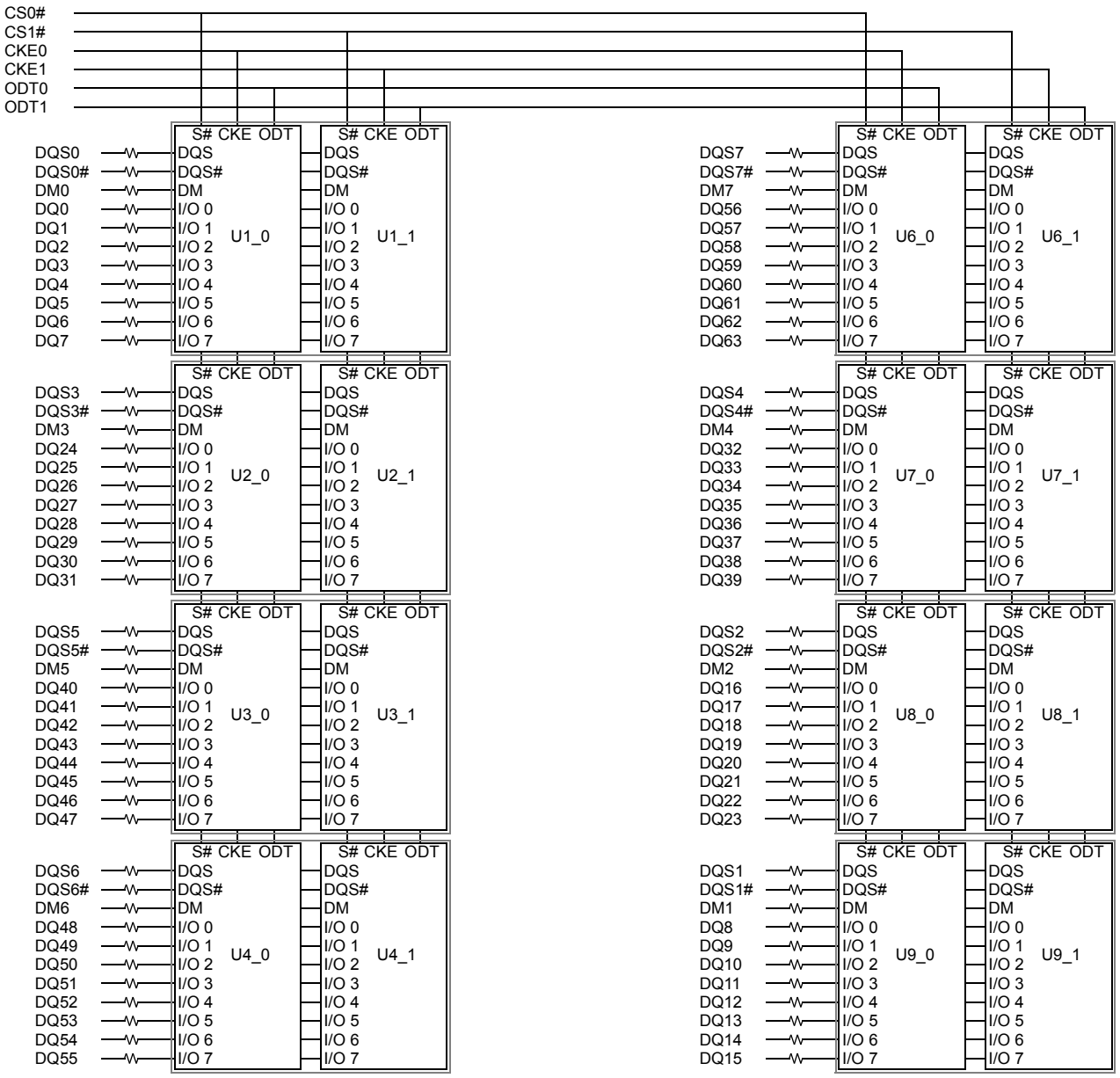
Pin Description Table

Symbol	Type	Polarity	Function
CK0, CK1	SSTL_18	Positive Edge	Positive line of the differential pair of system clock inputs. (All DDR2 SDRAM address and control inputs are sampled on the rising edge of their associated clocks. Output data is referenced at the crossings of the clocks.)
CK0#, CK1#	SSTL_18	Negative Edge	Negative line of the differential pair of system clock inputs.
ODT0, ODT1	SSTL_18	Active High	On-Die Termination: ODT when high enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, and DM. The ODT input will be ignored if disabled in Extended Mode Register (EMRS).
CKE0, CKE1	SSTL_18	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	SSTL_18	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	SSTL_18	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0~BA2	SSTL_18	-	Bank Address define to which bank an Activate, Read, Write or Precharge command is being applied. Bank address also determines if the Mode Register or Extended Mode Register is to be accessed during a MRS or EMRS cycle.
A0~A9, A10/AP, A11~A13	SSTL_18	-	During a Bank Activate command cycle, A0-A13 defines the row address (RA0-RA13) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0~BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0~BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0~BA2. If AP is low, BA0~BA2 are used to define which bank to precharge. The address inputs also provide the op-code during Mode Register Set commands.

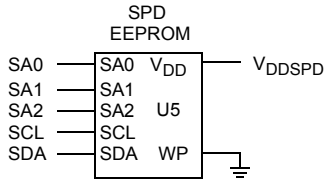
Pin Description Table (Contd.)

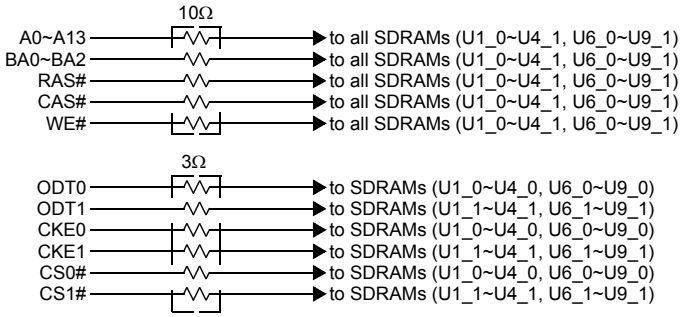
Symbol	Type	Polarity	Function
DQ0~DQ63	SSTL_18	-	Data Input/Output pins.
DQS0~DQS7	SSTL_18	Positive Edge	SDRAM differential data strobe for input and output data.
DQS0#~DQS7#	SSTL_18	Negative Edge	SDRAM differential data strobe for input and output data.
DM0~DM7	SSTL_18	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ/DQS loading.
SA0~SA2	LVTTL	-	Slave Address Select for EEPROM. These pins are used to configure the presence-detect device.
SDA	LVTTL	-	Serial Bus Data Line for EEPROM. SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module. A resistor must be connected from the SDA bus line to V_{DD} to act as pull up on the system board.
SCL	LVTTL	-	Serial Bus Clock for EEPROM. SCL is used to synchronize the presence-detect data transfer to and from the module. A resistor may be connected from the SCL bus line to V_{DD} to act as pull up on the system board.
V_{DD}	Supply	-	SDRAM positive power supply. 1.8V±0.1V
V_{SS}	Supply	-	Power supply return (ground).
V_{REF}	Supply	-	SDRAM I/O reference supply.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports operation from 1.7V to 3.6V.
NC	-	-	No Connect

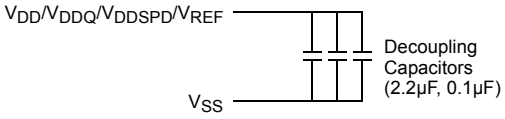
Block Diagram



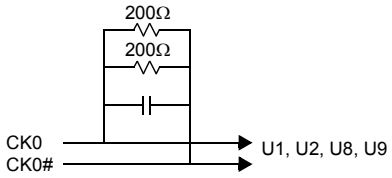
Note: Unless otherwise noted, data resistor values are 22Ω ± 5%.

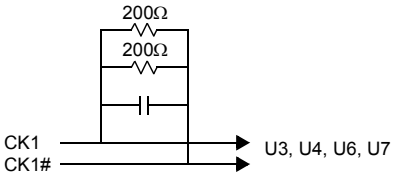






Clock Wiring	
CK0/CK0#	8 SDRAMs
CK1/CK1#	8 SDRAMs

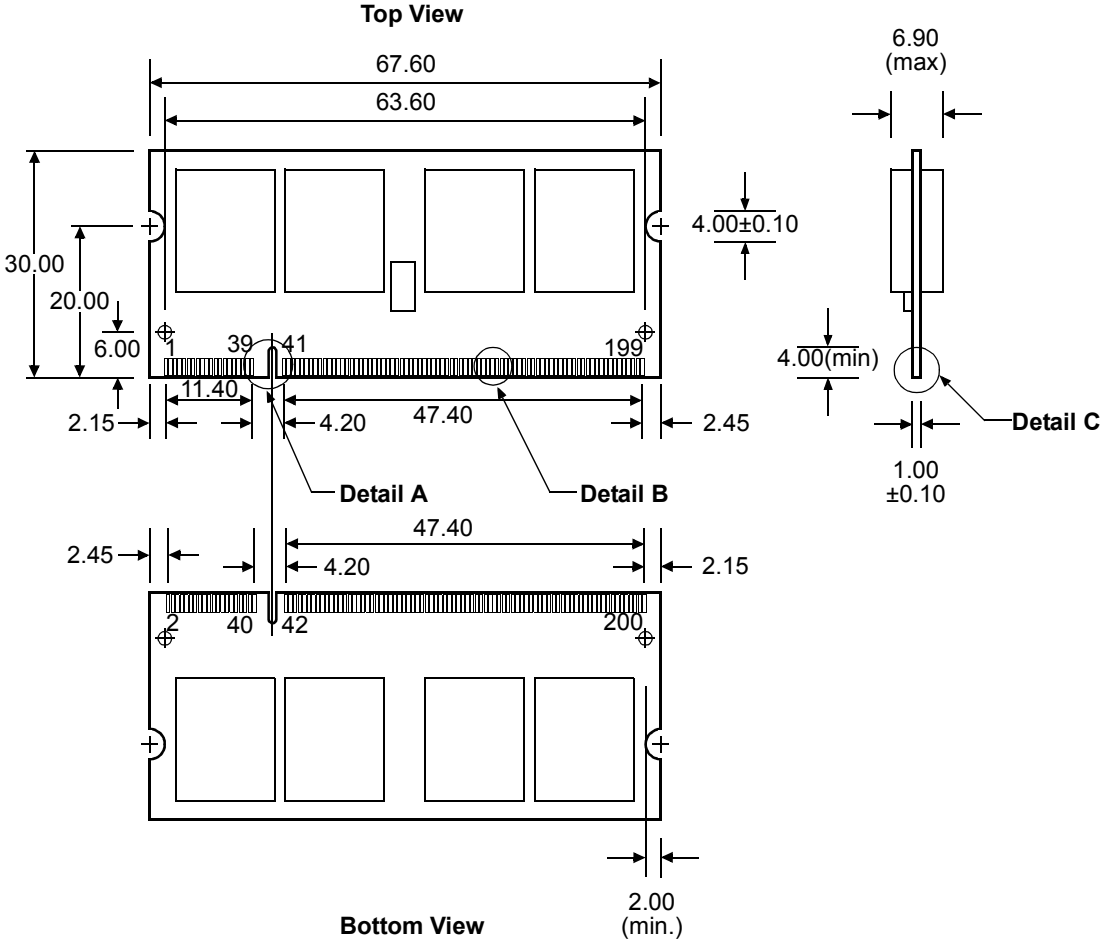


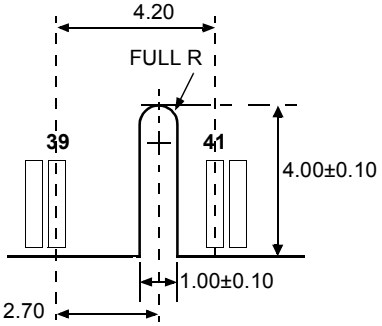


Notes:
1. Ax, BAx, RAS#, CAS#, WE# resistors: 10Ω±5%.
2. CS0#, CS1#, CKE0, CKE1, ODT0, ODT1 resistors: 3Ω±5%.

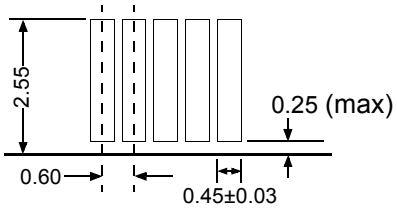
Physical Dimensions

200-pin SO-DIMM Module

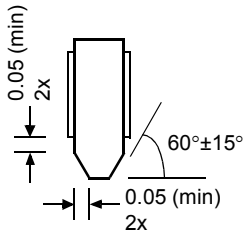




Detail A : Position of Voltage Notch



Detail B : Edge Connector



Detail C

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Serial Presence Detect Table (SG564568FG8NRDB/DG/IL)

Byte No.	Byte Description	Value Supported			Value in Hex		
		DDR2-400	DDR2-533	DDR2-667	DDR2-400	DDR2-533	DDR2-667
0	# of bytes written into serial memory at module manufacturer	128 Bytes			80h		
1	Total # of bytes of SPD memory device	256 Bytes			08h		
2	Fundamental memory type	SDRAM DDR2			08h		
3	# of row address on this assembly	14			0Eh		
4	# of column address on this assembly	10			0Ah		
5	# of Ranks, Package and Height	2, Stacked, 30.00mm			71h		
6	Data width of this assembly	64			40h		
7	Reserved	-			00h		
8	Voltage interface standard of this assembly	SSTL_18			05h		
9	SDRAM cycle time @ CAS latency of X	5.0ns	3.75ns	3.0ns	50h	3Dh	30h
10	SDRAM access time @ CAS latency of X	0.60ns	0.50ns	0.45ns	60h	50h	45h
11	DIMM configuration type	Non-ECC			00h		
12	Refresh rate & type	SR, 7.8			82h		
13	Primary SDRAM width	8			08h		
14	Error checking SDRAM width	-			00h		
15	Reserved	-			00h		
16	SDRAM device attributes : Burst lengths supported	4, 8			0Ch		
17	SDRAM device attributes : # of banks on SDRAM device	8			08h		
18	SDRAM device attributes : CAS latency	3, 4		4, 5	18h		30h
19	Reserved	-			00h		
20	DIMM type information	SO-DIMM			04h		
21	SDRAM module attributes	None			00h		
22	SDRAM device attributes : General	Weak Driver			01h		
23	SDRAM cycle time @ CAS latency of X-1	5.0ns		3.75ns	50h		3Dh
24	SDRAM access time @ CAS latency of X-1	0.60ns	0.50ns	0.45ns	60h	50h	45h
25	SDRAM cycle time @ CAS latency of X-2	-			00h		
26	SDRAM access time @ CAS latency of X-2	-			00h		

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported			Value in Hex		
		DDR2-400	DDR2-533	DDR2-667	DDR2-400	DDR2-533	DDR2-667
27	Minimum row precharge time (=tRP)	15ns			3Ch		
28	Minimum row active to row active delay (=tRRD)	7.5ns			1Eh		
29	Minimum RAS to CAS delay (=tRCD)	15ns			3Ch		
30	Minimum activate precharge time (=tRAS)	40ns	45ns		28h	2Dh	
31	Module row density	1GB			01h		
32	Command and Address signal input setup time	0.35ns	0.25ns	0.20ns	35h	25h	20h
33	Command and Address signal input hold time	0.47ns	0.37ns	0.27ns	47h	37h	27h
34	Data signal input setup time	0.15ns	0.10ns		15h	10h	
35	Data signal input hold time	0.27ns	0.22ns	0.17ns	27h	22h	17h
36	Write recovery time (=tWR)	15ns			3Ch		
37	Internal write to read command delay (=tWTR)	10.0ns	7.5ns		28h	1Eh	
38	Internal read to precharge delay (=tRTP)	7.5ns			1Eh		
39	Memory Analysis Probe Characteristics	-			00h		
40	Extension of tRC and tRFC	Extension of tRFC			06h		
41	Device Minimum activate/auto-refresh time (=tRC)	55ns	60ns		37h	3Ch	
42	Device Minimum auto-refresh to active/ auto-refresh time (=tRFC)	127.5ns			7Fh		
43	Maximum device cycle time (=tCK max)	8ns			80h		
44	Device DQS-DQ skew for DQS and associated DQ signals (=tDQSQ max)	0.35ns	0.30ns	0.24ns	23h	1Eh	18h
45	Device read data hold skew factor (=tQHS)	0.45ns	0.40ns	0.34ns	2Dh	28h	22h
46	PLL relock time	-			00h		
47~61	Superset Information (reserved for future use)	-			00h		
62	SPD data revision code	1.0			10h		
63	Checksum for bytes 0~62				0Eh	A7h	5Dh

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported			Value in Hex		
		DDR2-400	DDR2-533	DDR2-667	DDR2-400	DDR2-533	DDR2-667
64	Manufacturer JEDEC ID code	Continuation Code			7Fh		
65	.....Manufacturer JEDEC ID code	SMART's ID			94h		
66~71	.....Manufacturer JEDEC ID code	Not Used			FFh		
72	Manufacturing location	See Note 1			01h		
73~90	Manufacturer part #	SG564568FG8NRUU			P. No		
91	Manufacturer revision code	Rev. 0			00h		
92	.....Manufacturer revision code	None			FFh		
93	Manufacturing data (Year)	Date			Date		
94	Manufacturing data (Week)	Date			Date		
95~98	Assembly serial #	Serial Number			S. No		
99~125	Manufacturer specific data	SMART Modular Technologies					
126~127	Unused storage locations	-			00h		
128~255	Unused storage locations	-			FFh		

Note:

1. X represents the maximum CAS Latency.
   For DDR2-400/533, X = CL 4.0
   For DDR2-667, X = CL 5.0
2. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

Mode Register Table Definition

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It controls CAS latency, burst length, burst sequence, test mode, DLL reset, t_{WR} and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on CS#, RAS#, CAS#, WE#, BA0 and BA1, while controlling the state of address pins A0~A15. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register. The mode register set command cycle time (t_{MRD}) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0~A2 with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4~A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to low for normal MRS operation. Write recovery time t_{WR} is defined by A9~A11.

BA2	BA1	BA0	A15~A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
M18	M17	M16	M15~M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0	Mode Register
0	MR		0[1]	0	PD	WR			DLL	TM	CAS Latency			BT	Burst Length			

M8	DLL Reset
0	No
1	Yes

M7	Mode
0	Normal
1	Test

M3	Burst Type
0	Sequential
1	Interleave

Burst Length

M2	M1	M0	BL
0	1	0	4
0	1	1	8

M12	Active power down exit time
0	Fast exit (t_{XARD})
1	Slow exit (t_{XARDS})

M17	M16	MRS mode
0	0	MRS
0	1	EMRS (1)
1	0	EMRS (2): Reserved
1	1	EMRS (3): Reserved

Write recovery for autoprecharge

M11	M10	M9	WR (cycles)[2]
0	0	0	Reserved
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	Reserved
1	1	1	Reserved

DDR2-400, DDR2-533, DDR2-667, DDR2-800

CAS Latency

M6	M5	M4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2.0 (optional)
0	1	1	3.0
1	0	0	4.0
1	0	1	5.0 (optional)
1	1	0	Reserved
1	1	1	Reserved

Notes:
1. A14~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. WR min is determinedby t_{CK} max and WR max is determined by t_{CK} min. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer. The mode register must be programmed to this value.

Extended Mode Register Table Definition

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, output drive strength, ODT (R_{TT}), Posted CAS additive latency (AL), off-chip driver impedance calibration (OCD), DQS# enable/disable, RDQS/RDQS# enable/disable, and OUTPUT enable/disable. The extended mode register is programmed via the LOAD MODE (LM) command and will retain the stored information until it is programmed again or the device loses power. Reprogramming the extended mode register will not alter the contents of the memory array, provided it is performed correctly.

The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time t_{MRD} before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

Notes:
1. A14~A15 are reserved for future use and must be programmed to 0 when setting the mode register.
2. When the adjust mode of the OCD Calibration Program is issued, AL from previously set value must be applied.
3. After setting the OCD Calibration Program to default, OCD mode needs to be exited by setting A9-A7 to 000.
4. Outputs disabled - DQs, DQSs, DQS#s, RDQSs, RDQS#s. This feature is used in conjunction with DIMM I_{DD} measurements when I_{DDQ} is not desired to be included.
5. If RDQS is enabled, the DM function is disabled. RDQS is active for reads and don't care for writes.
6. Supported for DDR2-667 speed only.

Extended Mode Register Table

BA2	BA1	BA0	A15~A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address Field
E18	E17	E16	E15~E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0	Extended Mode Register
0	EMR		0^1	0	Q_{off}	RDQS	DQS#	OCD Program			R_{TT}	Additive latency			R_{TT}	D.I.C	DLL	

E17	E16	MRS mode
0	0	MRS
0	1	EMRS (1)
1	0	EMRS (2)
1	1	EMRS (3): Reserved

E6	E2	R_{TT} (Nominal)
0	0	ODT Disabled
0	1	75 ohm
1	0	150 ohm
1	1	50 ohm[6] (See page 13)

E0	DLL Enable
0	Enable
1	Disable

E9	E8	E7	OCD Calibration Program
0	0	0	OCD calibration mode exit; maintain setting
0	0	1	Drive (1)
0	1	0	Drive (0)
0	1	1	Adjust mode[2] (See page 13)
1	1	1	OCD calibration default[3] (See page 13)

E5	E4	E3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

E12	Q_{off} (Optional)[4] (See page 13)
0	Output buffer enabled
1	Output buffer disabled

E1	Output Driver Impedence Control	Driver Size
0	Normal	100%
1	Weak	60%

E10	DQS#
0	Enable
1	Disable

E11	RDQS
0	Disable
1	Enable[5] (See page 13)

E11 (RDQS Enable)	E10 (DQS# Enable)	Strobe Function Matrix			
		RDQS/DM	RDQS#	DQS	DQS#
0 (Disable)	0 (Enable)	DM	Hi-z	DQS	DQS#
0 (Disable)	1 (Disable)	DM	Hi-z	DQS	Hi-z
1 (Enable)	0 (Enable)	RDQS	RDQS#	DQS	DQS#
1 (Enable)	1 (Disable)	RDQS	Hi-z	DQS	Hi-z

Commands

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Function	CKE		CS#	RAS#	CAS#	WE#	BA0~BAn[9]	An[8]~A11	A10	A9~A0	Notes
	Previous cycle	Current cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1, 2
Refresh	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1, 7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1, 2
Precharge All Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1, 2
Write	H	H	L	H	L	L	BA	Column	L	Column	1, 2, 3
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	1, 2, 3
Read	H	H	L	H	L	H	BA	Column	L	Column	1, 2, 3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1, 2, 3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1, 4
			L	H	H	H					

Notes:

1. All DDR2 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock.
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 cannot be terminated or interrupted.
4. The Power Down Mode does not perform any refresh operations. The duration of power down is therefore limited by the refresh requirements.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6. “X” means “H or L (but a defined logic level)”.
7. Self Refresh Exit is asynchronous.
8. An = A12 for 256Mb, A13 for 512Mb & 1 Gb, A14 for 2Gb.
9. BAn = BA1 for upto 512Mb , BA2 for 1 Gb & 2Gb.

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Notes
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 2.3	V	
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.3	V	
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.3	V	
Voltage on V_{DDSPD} relative to V_{SS}	V_{DDSPD}	1.7 ~ 3.6	V	
Operating Temperature (Ambient)	T_{OPR}	0 to +65	°C	
Operating Temperature (Case)	T_{CASE}	0 to +85	°C	1, 2
Storage Temperature	T_{STG}	-55 to +100	°C	

Notes:

1. It is possible to operate the DRAM above Case Temperature up to 95ºC.
2. Above 85°C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to t_{REFI} = 3.9µs

Recommended DC Operating Conditions (T_A = 0 to +65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
I/O Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	
I/O Reference Voltage	V_{REF}	0.49*V_{DDQ}	0.50*V_{DDQ}	0.51*V_{DDQ}	mV	1, 2
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V	3
SPD Voltage	V_{DDSPD}	1.7	-	3.6	V	
Input High Voltage	$V_{IH(DC)}$	V_{REF} + 0.125	-	V_{DDQ} + 0.3	V	
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	V_{REF} - 0.125	V	
Input Voltage Level, CK/CK#	$V_{IN(DC)}$	-0.3	-	V_{DDQ} + 0.3	V	
Input Differential Voltage, CK/CK#	$V_{ID(DC)}$	0.25	-	V_{DDQ} + 0.6	V	
Ground	V_{SS}	0	0	0	V	

Notes:

1. V_{REF} is expected to track variation in V_{DDQ}.
2. Peak to peak noise (non-common mode) on V_{REF} may not exceed ±1% of the DC value. Peak to peak AC noise on V_{REF} may not exceed ±2% of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of V_{REF}.

Capacitance
(V_{DD} = 1.8V±0.1V, T_{Case} = +25°C)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (CKn, CKn#)	C_{CK}	8.0	16.0	pF
Input Capacitance delta (CKn, CKn#)	C_{DCK}	-	2.0	pF
Input Capacitance (all other input-only pins)	C_{I}	16.0	32.0	pF
Input Capacitance delta (all other input-only pins)	C_{DI}	-	4.0	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#)	C_{I01}	5.0	8.0	pF
Input/Output Capacitance (DQ, DM, DQS, DQS#)	C_{I02}	5.0	7.0	pF
Input/Output Capacitance delta (DQ, DM, DQS, DQS#)	C_{DI0}	-	1.0	pF

Notes:
1. C_{IO1} is for DDR2-400 and DDR2-533.
2. C_{IO2} is for DDR2-667.

AC Operating Conditions
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V)

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	$V_{IH(AC)}$	V_{REF} + 0.250	-	V	1, 2
Input Low Logic Voltage	$V_{IL(AC)}$	-	V_{REF} - 0.250	V	1, 2
Input differential voltage, CK and CK# inputs	$V_{ID(AC)}$	0.5	V_{DDQ} + 0.6	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	$V_{IX(AC)}$	0.5*V_{DDQ} - 0.175	0.5*V_{DDQ} + 0.175	V	1, 2, 3
AC differential crossing point voltage	$V_{OX(AC)}$	0.5*V_{DDQ} - 0.125	0.5*V_{DDQ} + 0.125	V	3

Notes:
1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of V_{IX}/V_{OX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

ODT DC Electrical Characteristics

Parameter	Symbol	Min	Nom	Max	Unit	Notes
R_{TT} effective impedence value for 75Ω setting EMR (A6, A2) = 0, 1	$R_{TT1(EFF)}$	60	75	90	Ω	1
R_{TT} effective impedence value for 150Ω setting EMR (A6, A2) = 1, 0	$R_{TT2(EFF)}$	120	150	180	Ω	1
R_{TT} effective impedence value for 50Ω setting EMR (A6, A2) = 1, 1	$R_{TT3(EFF)}$	40	50	60	Ω	1, 3
Deviation of VM with respect to $V_{DDQ}/2$	ΔVM	-6		+6	%	2

Notes:

1. $R_{TT1(EFF)}$ and $R_{TT2(EFF)}$ are determined by applying $V_{IH(AC)}$ and $V_{IL(AC)}$ to pin under test separately, then measure current $I(V_{IH(AC)})$ and $I(V_{IL(AC)})$ respectively. $R_{TT(EFF)} = \frac{V_{IH(AC)} - V_{IL(AC)}}{I(V_{IH(AC)}) - I(V_{IL(AC)})}$
2. Measured voltage (VM) at tested pin with no load.
$$\Delta VM = \left(\frac{2 \times VM}{V_{DDQ}} - 1\right) \times 100\,\%$$
3. Supported on DDR2-667 module only.

Output DC Current Drive

Parameter	Symbol	Min	Max	Unit	Notes
Output Minimum Source DC Current	I_{OH}	-13.4	-	mA	1, 3, 4
Output Minimum Sink DC Current	I_{OL}	13.4	-	mA	2, 3, 4

Notes:

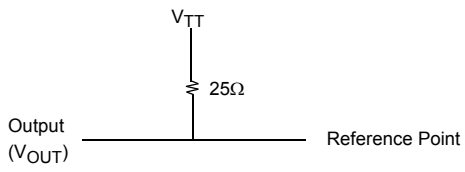
1. For I_{OH} (DC); V_{DDQ} = 1.7V, V_{OUT} = 1420mV. (V_{OUT} - V_{DDQ})/I_{OH} must be less than 21Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV.
2. For I_{OL} (DC); V_{DDQ} = 1.7V, V_{OUT} = 280mV. V_{OUT}/I_{OL} must be less than 21Ω for values of V_{OUT} between 0V and 280mV.
3. The DC value of V_{REF} applied to the receiving device is set to V_{TT}.
4. The values of I_{OH} (DC) and I_{OL} (DC) are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure V_{IH} min plus a noise margin and V_{IL} max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point along a 21Ω load line to define a convenient driver current for measurement.

OCD Default Output Characteristics
(V_{DD} = 1.8V±0.1V, V_{SS} = 0V, T_A = 0 to +65°C)

Parameter	Symbol	Min	Nom	Max	Unit	Notes
Output Impedance		12.6	18	23.4	Ω	1, 2
Pull-up and Pull-down mismatch		0		4	Ω	1, 2, 3
Output Slew Rate	S_{OUT}	1.5		5	V/ns	1, 4, 5, 7
Output Step Size for Calibration		0		1.5	Ω	6

Notes:
1. Absolute specifications: 0°C ≤ T_{case} ≤ +85°C; V_{DDQ} = +1.8V±0.1V, V_{DD} = +1.8V±0.1V.
2. Impedance measurement condition for output source DC current: V_{DDQ} = 1.7V; V_{OUT} = 1420mV; (V_{OUT} - V_{DDQ})/I_{OH} must be less than 23.4Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} - 280mV. Impedance measurement condition for output sink DC current: V_{DDQ} = 1.7V; V_{OUT} = 280mV; V_{OUT}/I_{OL} must be less than 23.4Ω for values of V_{OUT} between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4. Output slew rate for falling and rising edges is measured between V_{TT} - 250mV and V_{TT} + 250mV for single ended signals. For differential signals output slew rate is measured between DQS - DQS# = -500mV and DQS# - DQS = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
5. The absolute value of the slew rate as measured from V_{IL} (DC) max to V_{IH} (DC) min is equal to or greater than the slew rate as measured from V_{IL} (AC) max to V_{IH} (AC) min. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18Ω at nominal conditions across all process and represent only the DRAM uncertainty.
7. Timing skew due to DRAM output slew rate mis-match between DQS/DQS# and associated DQs is included in t_{DQSQ} and t_{QHS} specification.

Output Slew Rate Load Diagram



IDD Specification Parameters and Test Conditions (V_{DD} = 1.8V±0.1V, V_{SS} = 0V, T_A = 0 to +65°C)

Symbol	Parameter		5.0ns CL 3.0	3.75ns CL 4.0	3.0ns CL 5.0	Unit
IDD0	**Operating one bank active–precharge current;** $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		960	1040	1360	mA
IDD1	**Operating one bank active–read–precharge current;** I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE and CS# are HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		1080	1160	1720	mA
IDD2P	**Precharge power–down current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		80	80	112	mA
IDD2Q	**Precharge quiet standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		560	656	960	mA
IDD2N	**Precharge standby current;** All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		560	720	1040	mA
IDD3P	**Active power–down current;** All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	520	640	880	mA
		Slow PDN Exit MRS(12) = 1	360	440	600	mA
IDD3N	**Active standby current;** All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		640	800	1120	mA
IDD4W	**Operating burst write current;** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		1280	1440	2000	mA
IDD4R	**Operating burst read current;** All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		1400	1560	2200	mA
IDD5B	**Burst refresh current;** $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING		2240	2400	2720	mA
IDD6	**Self refresh current;** CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING		80	80	112	mA
IDD7	**Operating bank interleave read current;** All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R		2680	2760	3280	mA

IDD Specification Parameters and Test Conditions (Contd.)

Notes:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, DQS#. IDD values must be met with all combinations of ERMS bits 10 and 11.
5. Definitions for IDD

LOW	=	$V_{in} \leq V_{IL(AC)}$(max)
HIGH	=	$V_{in} \geq V_{IH(AC)}$(min)
STABLE	=	inputs stable at a HIGH or LOW level
FLOATING	=	inputs at $V_{REF} = V_{DDQ}/2$
SWITCHING	=	inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks of strobes.

IDD Testing Parameters

	DDR2-400	DDR2-533	DDR2-667	
Parameter	**3-3-3**	**4-4-4**	**5-5-5**	**Units**
CL(IDD)	3	4	5	t_{CK}
$t_{RCD(IDD)}$	15	15	15	ns
$t_{RC(IDD)}$	55	60	60	ns
$t_{RRD(IDD)}$	7.5	7.5	7.5	ns
$t_{CK(IDD)}$	5	3.75	3	ns
$t_{RASmin(IDD)}$	40	45	45	ns
$t_{RASmax(IDD)}$	70000	70000	70000	ns
$t_{RP(IDD)}$	15	15	15	ns
$t_{RFC(IDD)}$	127.5	127.5	127.5	ns

Device AC Operating Conditions

Parameter		Symbol	5.0ns @ CL 3.0 DDR2-400		3.75ns @ CL 4.0 DDR2-533		3.0ns @ CL 5.0 DDR2-667		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Clock cycle time	CL=5.0	t_{CK}	-	-	-	-	3000	8000	ps	12, 20
	CL=4.0		5000	8000	3750	8000	3750	8000	ps	12, 20
	CL=3.0		5000	8000	5000	8000	-	-	ps	12, 20
Clock high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	14
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	14
Clock half period		t_{HP}	Min (t_{CL}, t_{CH})	-	Min (t_{CL}, t_{CH})	-	Min (t_{CL}, t_{CH})	-	ps	15
DQ output access time from CK/CK#		t_{AC}	-600	+600	-500	+500	-450	+450	ps	
Data-out high-impedence window from CK/CK#		t_{HZ}	-	t_{AC}(max)	-	t_{AC}(max)	-	t_{AC}(max)	ps	4, 5
Data-out low-impedence window from CK/CK#		t_{LZ}	t_{AC}(min)	t_{AC}(max)	t_{AC}(min)	t_{AC}(max)	t_{AC}(min)	t_{AC}(max)	ps	4, 6
DQ & DM input setup time relative to DQS		t_{DS}	150	-	100	-	100	-	ps	3, 11, 17
DQ & DM input hold time relative to DQS		t_{DH}	275	-	225	-	175	-	ps	3, 11, 17
DQ & DM input pulse width (for each input)		t_{DIPW}	0.35	-	0.35	-	0.35	-	t_{CK}	
Data hold skew factor		t_{QHS}	-	450	-	400	-	340	ps	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	ps	11,13
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	0.35	-	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	0.35	-	t_{CK}	
DQS output access time from CK/CK#		t_{DQSCK}	-500	+500	-450	+450	-400	+400	ps	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2	-	0.2	-	0.2	-	t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2	-	0.2	-	0.2	-	t_{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	350	-	300	-	240	ps	11,13
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	18
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS write preamble setup time		t_{WPRES}	0	-	0	-	0	-	ps	8, 9
DQS write preamble		t_{WPRE}	0.25	-	0.25	-	0.35	-	t_{CK}	
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	7

Device AC Operating Conditions (Contd.)

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400		3.75ns @ CL 4.0 DDR2-533		3.0ns @ CL 5.0 DDR2-667		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command to first DQS latching transition	t_{DQSS}	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	WL - 0.25	WL + 0.25	t_{CK}	
Address & control input pulse width for each input	t_{IPW}	0.6	-	0.6	-	0.6	-	t_{CK}	
Address and control input setup time	t_{IS}	350	-	250	-	200	-	ps	2, 17
Address and control input hold time	t_{IH}	475	-	375	-	275	-	ps	2, 17
CAS# to CAS# command delay	t_{CCD}	2	-	2	-	2	-	t_{CK}	
OCD Drive mode delay	t_{OIT}	0	12	0	12	0	12	ns	
CKE low to CK, CK# uncertainity	t_{DELAY}	5.825	5.825	4.375	4.375	3.475	3.475	ns	24
ACTIVE to ACTIVE (same bank) command	t_{RC}	55	-	60	-	60	-	ns	
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	7.5	-	7.5	-	ns	23
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	15	-	15	-	ns	
ACTIVE to PRECHARGE command	t_{RAS}	40	70000	45	70000	45	70000	ns	16
Internal READ to precharge command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	ns	19, 23
Write recovery time	t_{WR}	15	-	15	-	15	-	ns	23
Auto precharge write recovery + Precharge time	t_{DAL}	$t_{WR} + t_{RP}$	-	$t_{WR} + t_{RP}$	-	$t_{WR} + t_{RP}$	-	t_{CK}	18
Internal WRITE to READ command delay	t_{WTR}	10	-	7.5	-	7.5	-	ns	23
PRECHARGE command period	t_{RP}	15	-	15	-	15	-	ns	
LOAD MODE command cycle time	t_{MRD}	2	-	2	-	2	-	t_{CK}	
REFRESH to REFRESH command interval	t_{RFC}	127.5	-	127.5	-	127.5	-	ns	10
Average periodic refresh Interval	t_{REFI}	-	7.8	-	7.8	-	7.8	µs	10
Exit self refresh to non-READ command	t_{XSNR}	t_{RFC}(min) + 10	-	t_{RFC}(min) + 10	-	t_{RFC}(min) + 10	-	ns	
Exit self refresh to READ command	t_{XSRD}	200	-	200	-	200	-	t_{CK}	

Device AC Operating Conditions (Contd.)

Parameter	Symbol	5.0ns @ CL 3.0 DDR2-400		3.75ns @ CL 4.0 DDR2-533		3.0ns @ CL 5.0 DDR2-667		Unit	Notes
		Min	Max	Min	Max	Min	Max		
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}	
ODT turn-on	t_{AON}	t_{AC}(min)	t_{AC}(max) + 1000	t_{AC}(min)	t_{AC}(max) + 1000	t_{AC}(min)	t_{AC}(max) + 1000	ps	21
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}	
ODT turn-off	t_{AOF}	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	t_{AC}(min)	t_{AC}(max) + 600	ps	22
ODT turn-on (power-down mode)	t_{AONPD}	t_{AC}(min) + 2000	2*t_{CK} + t_{AC}(max) + 1000	t_{AC}(min) + 2000	2*t_{CK} + t_{AC}(max) + 1000	t_{AC}(min) + 2000	2*t_{CK} + t_{AC}(max) + 1000	ps	
ODT turn-off (power-down mode)	t_{AOFPD}	t_{AC}(min) + 2000	2.5*t_{CK} + t_{AC}(max) + 1000	t_{AC}(min) + 2000	2.5*t_{CK} + t_{AC}(max) + 1000	t_{AC}(min) + 2000	2.5*t_{CK} + t_{AC}(max) + 1000	ps	
ODT to power-down entry latency	t_{ANPD}	3		3		3		t_{CK}	
ODT power-down exit latency	t_{AXPD}	8		8		8		t_{CK}	
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	2	-	2	-	t_{CK}	
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	6 - AL	-	6 - AL	-	7 - AL	-	t_{CK}	
Exit precharge power down to any non-read command	t_{XP}	2	-	2	-	2	-	t_{CK}	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	-	3	-	3	-	t_{CK}	

Notes:

1. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level.
2. Command/Address minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of CK/CK#. t_{IS} timing is referenced to $V_{IH\ (AC)}$ for a rising signal and $V_{IL\ (AC)}$ for a fallng signal. t_{IH} timing is referenced to $V_{IH\ (DC)}$ for a rising signal and $V_{IL\ (DC)}$ for a fallng signal. Derating values for Command/Address input signal slew rates < 1.0V/ns are TBD.
3. Data minimum input slew rate = 1.0V/ns and is referenced to the crosspoint of DQS/DQS# if differential strobe feature is enabled. t_{DS} timing is referenced to $V_{IH\ (AC)}$ for a rising signal and $V_{IL\ (AC)}$ for a fallng signal. t_{DH} timing is referenced to $V_{IH\ (DC)}$ for a rising signal and $V_{IL\ (DC)}$ for a fallng signal. Derating values for Data input signal slew rates < 1.0V/ns are TBD.
4. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (t_{HZ}) or begins driving (t_{LZ}).
5. This maximum value is derived from the reference test load. $t_{HZ\ (MAX)}$ will prevail over a $t_{DQSCK\ (MAX)} + t_{RPST\ (MAX)}$ condition.
6. $t_{LZ\ (MIN)}$ will prevail over a $t_{DQSCK\ (MIN)} + t_{RPRE\ (MAX)}$ condition.
7. The intent of the Don't Care state after completion of the postamble is the DQS driven signal should be high, low or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high [above $V_{IH\ DC\ (MIN)}$] then it must not transition low (below $V_{IH\ DC}$) prior to $t_{DQSH(min)}$.
8. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
9. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during his time depending on t_{DQSS}.
10. The refresh period is 64ms. This equates to an average refresh rate of 7.8125µs. However, an REFRESH comand must be asserted at least once every 70.3µs or $t_{RFC\ (MAX)}$; issuing more than eight REFRESH commands back to back at $t_{RFC\ (min)}$ is not allowed.
11. Each byte lane has a corresponding DQS.
12. CK and CK# input slew rate must be ≥ 1 V/ns (≥ 2 V/ns if measured differentially).
13. The data valid window is derived by achieving other specifications: t_{HP}, ($t_{CK}/2$), t_{DQSQ}, and t_{QH} ($t_{QH} = t_{HP} - t_{QHS}$). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
14. MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
15. $t_{HP\ (MIN)}$ is the lesser of t_{CL} minimum and t_{CH} minimum actually applied to the device CK and CK# inputs.
16. READs and WRITEs with no auto precharge are allowed to be issued before $t_{RAS\ (MIN)}$ is satisfied since t_{RAS} lockout feature is supported in DDR2 SDRAM.
17. V_{IL}/V_{IH} DDR2 overshoot/undershoot. Refer to 256MB, 512MB, or 1GB DDR2 SDRAM component data sheet for more detailed information.
18. $t_{DAL} = (n_{WR}) + (t_{RP}/t_{CK})$: For each of the terms above, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period; n_{WR} refers to the t_{WR} parameter stored in the MR[11,10,9].
19. This is a minimum requirement. Minimum READ to internal PRECHARGE timing is AL + BL/2 providing the t_{RTP} and $t_{RAS\ (MIN)}$ have been satisfied. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until $t_{RAS\ (MIN)}$ has been satisfied.
20. Operating frequency is only allowed to change during self refresh mode or precharge power-down mode. Anytime the operating frequency is changed, not including jitter, the DLL is required to be reset followed by 200 clock cycles.
21. ODT turn-on time $t_{AON\ (MIN)}$ is when the device leaves high impedence and ODT resistance begins to turn-on. ODT turn-on time $t_{AON\ (MAX)}$ is when the resistance is fully on. Both are measured from t_{AOND}.
22. ODT turn-off time $t_{AOF\ (MIN)}$ is when the device starts to turn-off ODT resistance. ODT turn-off time $t_{AOF\ (MAX)}$ is when the bus is in high impedence. Both are measured from t_{AOFD}.
23. This parameter has a two clock minimum requirement at any t_{CK}.
24. t_{DELAY} is calculated from $t_{IS} + t_{CK} + t_{IH}$ so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system reset condition.

Part Number Decode

S	G	5	64	56	8	F	G	8	N	R	U	U
1	2	3	4	5	6	7	8	9	10	11	12	13

1 **SMART Modular Technologies**

2 **Module Process Technology**
G: Green Module (RoHS Compliant)

3 **Product Category**
5: SDRAM/DRAM SIMM/DIMM

4 **Module Data Bus Width**
64: x64

5 **Module Address Depth**
56: 256M

6 **Device Data Width**
8: x8

7 **Special Device Feature**
F: Staktek Stacked (8 Bank SDRAM) FBGA

8 **Voltage/Mode**
G: DDR2 SDRAM

9 **Refresh/Power**
8: 8K Refresh/Standard Power

10 **Module Configuration**
N: 200-pin SO-DIMM Unbuffered, Non-ECC

11 **Device Physicals**
R: Depth Stacked Device Based

12 **CAS Latency**
D: 3.0, 4.0
I: 4.0, 5.0

13 **Cycle Time (Clock Speed)**
B: 5.0ns (200MHz, PC2-3200, DDR2-400-333)
G: 3.75ns (267MHz, PC2-4200, DDR2-533-444)
L: 3.0ns (333MHz, PC2-5300, DDR2-667-555)

Note : “U” in the part number should be replaced by user specified option.

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