



<b>Ordering Information</b>	
<b>Part Numbers</b>	<b>Description</b>
SG572288578DR3R	128Mx72 (1GB), SDRAM, 144-pin SODIMM, Unbuffered, PLL, ECC, 128Mx8 Based (Stacked - two 64Mx8), PC133, CL 3.0, 36.32mm, Green Module (RoHS Compliant).

## Revision History

- **December 12, 2006**  
Datasheet released.

## 1GByte (128Mx72) SDRAM Module - 128Mx8 Based (Stacked - two 64Mx8) 144-pin SODIMM, Unbuffered, PLL, ECC

**Features**

- Standard : PC133
- Configuration : ECC
- Cycle Time : 7.5ns
- CAS# Latency : 3.0 only
- Burst Length : 1, 2, 4, 8 or Page
- Burst Type : Linear/Interleave
- No. of Internal Banks per SDRAM : 4
- Operating Voltage : 3.3V
- Refresh : 8K/64ms
- Device Physicals : 400mil TSOP
- Lead Finish : Gold
- Length x Height : 67.60mm x 36.32mm
- No. of sides : Double-sided
- Mating Connector (Examples)  
Horizontal : AMP - 390113-1

**144-pin SDRAM SODIMM Pin List**

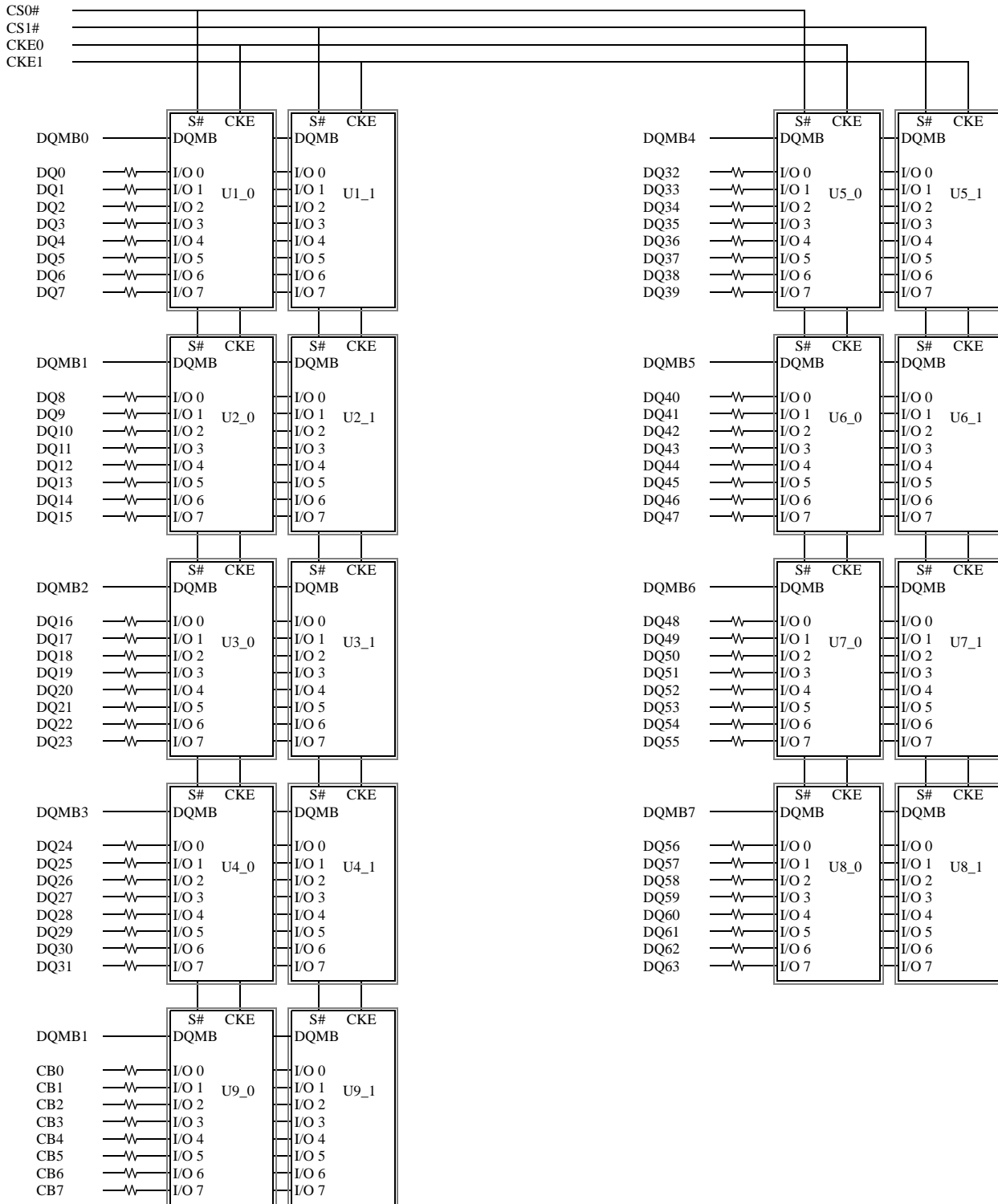
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V <sub>SS</sub>	2	V <sub>SS</sub>	37	DQ8	38	DQ40	73	NC	74	CLK1	109	A9	110	BA1
3	DQ0	4	DQ32	39	DQ9	40	DQ41	75	V <sub>SS</sub>	76	V <sub>SS</sub>	111	A10/AP	112	A11
5	DQ1	6	DQ33	41	DQ10	42	DQ42	77	CB2	78	CB6	113	V <sub>DD</sub>	114	V <sub>DD</sub>
7	DQ2	8	DQ34	43	DQ11	44	DQ43	79	CB3	80	CB7	115	DQMB2	116	DQMB6
9	DQ3	10	DQ35	45	V <sub>DD</sub>	46	V <sub>DD</sub>	81	V <sub>DD</sub>	82	V <sub>DD</sub>	117	DQMB3	118	DQMB7
11	V <sub>DD</sub>	12	V <sub>DD</sub>	47	DQ12	48	DQ44	83	DQ16	84	DQ48	119	V <sub>SS</sub>	120	V <sub>SS</sub>
13	DQ4	14	DQ36	49	DQ13	50	DQ45	85	DQ17	86	DQ49	121	DQ24	122	DQ56
15	DQ5	16	DQ37	51	DQ14	52	DQ46	87	DQ18	88	DQ50	123	DQ25	124	DQ57
17	DQ6	18	DQ38	53	DQ15	54	DQ47	89	DQ19	90	DQ51	125	DQ26	126	DQ58
19	DQ7	20	DQ39	55	V <sub>SS</sub>	56	V <sub>SS</sub>	91	V <sub>SS</sub>	92	V <sub>SS</sub>	127	DQ27	128	DQ59
21	V <sub>SS</sub>	22	V <sub>SS</sub>	57	CB0	58	CB4	93	DQ20	94	DQ52	129	V <sub>DD</sub>	130	V <sub>DD</sub>
23	DQMB0	24	DQMB4	59	CB1	60	CB5	95	DQ21	96	DQ53	131	DQ28	132	DQ60
25	DQMB1	26	DQMB5	61	CLK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
27	V <sub>DD</sub>	28	V <sub>DD</sub>	63	V <sub>DD</sub>	64	V <sub>DD</sub>	99	DQ23	100	DQ55	135	DQ30	136	DQ62
29	A0	30	A3	65	RAS#	66	CAS#	101	V <sub>DD</sub>	102	V <sub>DD</sub>	137	DQ31	138	DQ63
31	A1	32	A4	67	WE#	68	NC	103	A6	104	A7	139	V <sub>SS</sub>	140	V <sub>SS</sub>
33	A2	34	A5	69	CS0#	70	A12	105	A8	106	BA0	141	SDA	142	SCL
35	V <sub>SS</sub>	36	V <sub>SS</sub>	71	NC	72	NC	107	V <sub>SS</sub>	108	V <sub>SS</sub>	143	V <sub>DD</sub>	144	V <sub>DD</sub>

(All specifications of this device are subject to change without notice.)

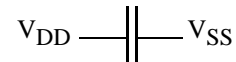
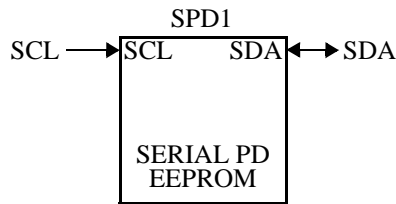
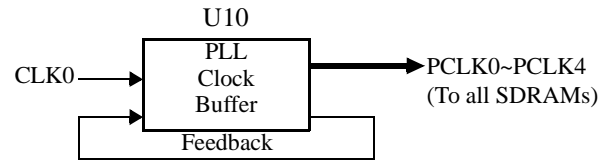
**Pin Description Table**

Symbol	Type	Polarity	Function
CLK0, CLK1	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0	Input	Active High	Activates the SDRAM CLK signal when high and deactivates the CLK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0, BA1	Input	-	Selects which of the four internal SDRAM banks is activated.
A0~A9, A10/AP, A11~A12	Input	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA9, CA11) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke auto-precharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0~DQ63 CB0~CB7	Input-Output	-	Data and Check Bit Input/Output pins.
DQMB0~DQMB7	Input	Active High	Data strobe for input and output data.
SDA	Input-Output	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected on the system board from the SDA bus line to V <sub>DD</sub> to act as a pullup.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected on the system board from the SCL bus line to V <sub>DD</sub> to act as a pullup.
V <sub>DD</sub> , V <sub>SS</sub>	Supply	-	Power and ground for the SDRAM input buffers and core logic.
NC	Supply	-	No Connect.

**Block Diagram**



- A0~A12 → to all SDRAMs (U1~U9)
- BA0, BA1 → to all SDRAMs (U1~U9)
- RAS# → to all SDRAMs (U1~U9)
- CAS# → to all SDRAMs (U1~U9)
- WE# → to all SDRAMs (U1~U9)
- CKE0 → to SDRAMs (U1\_0~U9\_0)
- CKE1 → to SDRAMs (U1\_1~U9\_1)
- CS0# → to SDRAMs (U1\_0~U9\_0)
- CS1# → to SDRAMs (U1\_1~U9\_1)



Decoupling capacitors  
to all devices.

**Notes:**

1. U<sub>x\_0</sub> and U<sub>x\_1</sub> represent the lower and upper devices in the stack U<sub>x</sub>. For example, U1\_0 and U1\_1 represent lower and upper devices in the stack U1.
2. CLK1 is terminated on the module into a 10Ω/10pF combination.
3. Data signals are terminated using 47Ω series resistors.
4. A0~A2 of serial PD EEPROM are grounded.

## DC Characteristics

### Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-1.0 ~ 4.6	V
Voltage on supply pins relative to $V_{SS}$	$V_{DDT}$	-1.0 ~ 4.6	V
Power Dissipation	$P_T$	18	W
Operating Temperature	$T_{opr}$	0 to +70	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Short Circuit Output Current	$I_{OS}$	50	mA

### Recommended DC Operating Conditions

( $T_A = 0$  to  $+70^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{DD}$	3.0	3.3	3.6	V
Ground	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	-	$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V

### DC Characteristics (Cont'd)

#### Capacitance

( $V_{DD} = 3.3V \pm 0.3V$ ,  $T_A = +25^\circ C$ )

Parameter	Symbol	Max	Unit
Input Capacitance (Address, RAS#, CAS#, WE#)	$C_{I1}$	68.4	pF
Input Capacitance (CKE0, CKE1, CS0#, CS1#)	$C_{I2}$	34.2	pF
Input Capacitance (CLK0, CLK1)	$C_{I3}$	3.5	pF
Input Capacitance (DQMB1)	$C_{I4}$	7.6	pF
Input Capacitance (DQMB0, DQMB2~DQMB7)	$C_{I5}$	3.8	pF
Input/Output Capacitance (DQ0~DQ63)	$C_{I/O}$	12	pF

**Notes :** Capacitance is sampled per Mil-Std-883.

#### Leakage Currents

( $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{SS} = 0V$ )

Parameter	Symbol	Test conditions	Min	Max	Unit
Input Leakage Current	$I_{LI}$	$0V \leq V_{in} \leq V_{DD} + 0.3$	-180	180	$\mu A$
Output Leakage Current	$I_{OZ}$	$0V \leq V_{out} \leq V_{DD}$ $D_{out} = \text{Disable}$	-20	20	$\mu A$
Output High Voltage	$V_{OH}$	High $I_{out} = -2mA$	2.4	-	mA
Output Low Voltage	$V_{OL}$	Low $I_{out} = 2mA$	-	0.4	mA



### DC Characteristics (Cont'd)

( $V_{DD} = 3.3V \pm 0.3V$ ,  $V_{SS} = 0V$ ,  $T_A = 0$  to  $+70^\circ C$ )

Parameter	Symbol	Test Conditions	Max	Unit	Notes
<b>Operating Current:</b> (One Bank Active)	$I_{CC1}$	Burst Length = 1, $t_{RC} \geq t_{RC(min.)}$ , $I_{OL} = 0mA$	1395	mA	1
<b>Precharge Standby Current In Power-Down Mode:</b>	$I_{CC2}$	$CKE \leq V_{IL(max.)}$ , $t_{CK} = 1 CLK$	63	mA	
		$CKE \& CLK \leq V_{IL max.}$ , $t_{CK} = \infty$	63	mA	
<b>Precharge Standby Current In Non Power-Down Mode:</b>	$I_{CC3}$	$CKE \geq V_{IH(min.)}$ , $CS\# \geq V_{IH(min.)}$ , $t_{CK} = 1 CLK$ , Input signals are changed one time during 2 CLKs	810	mA	
		$CKE \geq V_{IH(min.)}$ , $CLK \leq V_{IL (max.)}$ , $t_{CK} = \infty$ , Input signals are stable	810	mA	
<b>Active Standby Current In Power-Down Mode:</b>	$I_{CC4}$	$CKE \leq V_{IL(max.)}$ , $t_{CK} = 1 CLK$	63	mA	
		$CKE \& CLK \leq V_{IL(max.)}$ , $t_{CK} = \infty$	63	mA	
<b>Active Standby Current In Non Power-Down Mode:</b>	$I_{CC5}$	$CKE \geq V_{IH(min.)}$ , $CS\# \geq V_{IH(min.)}$ , $t_{CK} = 1 CLK$ , Input signals are changed one time during 2 CLKs	810	mA	
		$CKE \geq V_{IH(min.)}$ , $CLK \leq V_{IL (max.)}$ , $t_{CK} = \infty$ , Input signals are stable	810	mA	
<b>Operating Current:</b> (One Bank Active)	$I_{CC6}$	$I_{OL} = 0mA$ , Page Burst, $t_{CCD} = 2$ CLKs	1440	mA	1
<b>Auto Refresh Current:</b>	$I_{CC7}$	$t_{RC} \geq t_{RC min.}$	2700	mA	2
<b>Self Refresh Current:</b>	$I_{CC8}$	$CKE \leq 0.2 V$	108	mA	

**Notes:**

1. Measured with outputs open.
2. Refresh period is 64ms.

### AC Characteristics

Parameter	CAS Latency	Symbol	Min	Max	Units	Notes
Clock Cycle Time	CL = 3	$t_{CK}$	7.5	-	ns	
	CL = 2		10.0	-	ns	
CLK High Pulse Width		$t_{CH}$	2.5	-	ns	
CLK Low Pulse Width		$t_{CL}$	2.5	-	ns	
Access time from CLK	CL = 3	$t_{AC}$	-	5.4	ns	
	CL = 2		-	6.0	ns	
CKE setup time		$t_{CKS}$	1.5	-	ns	
CKE hold time		$t_{CKH}$	0.8	-	ns	
Address setup time		$t_{AS}$	1.5	-	ns	
Address hold time		$t_{AH}$	0.8	-	ns	
Command setup time		$t_{CSS}$	1.5	-	ns	
Command hold time		$t_{CSH}$	0.8	-	ns	
Data In setup time		$t_{DS}$	1.5	-	ns	
Data In hold time		$t_{DH}$	0.8	-	ns	
Data Out to Hi-Z time	CL = 3	$t_{HZ}$	-	5.4	ns	
	CL = 2		-	6.0	ns	
Data Out to Lo-Z time		$t_{LZ}$	1.0	-	ns	
Data Out hold time		$t_{OH}$	3.0	-	ns	
Active to Precharge Period		$t_{RAS}$	45	100000	ns	
Active to Active Command time		$t_{RC}$	65	-	ns	
Active to Read/Write time		$t_{RCD}$	20	-	ns	
Bank to bank active time		$t_{RRD}$	15	-	ns	
Precharge to Active Period		$t_{RP}$	20	-	ns	
Refresh Period		$t_{REF}$	-	64	ms	
Self Refresh Exit to Active time		$t_{XSR}$	75	-	ns	
Data In to Precharge Period		$t_{DPL}$	2	-	ns	
CAS# to CAS# delay time		$t_{CCD}$	1	-	cycle	
CKE to clock disable/enable		$t_{CKE}$	1	-	cycle	
DQM to input data delay		$t_{DID}$	0	-	cycle	
DQM to data out disable delay		$t_{DOD}$	0	-	cycle	
Write command to data delay		$t_{DWD}$	5	-	cycle	
Data in to Active Command		$t_{DAL}$	2	-	cycle	
MRS command to Active delay		$t_{MRD}$	2	-	cycle	

**Notes:**

1. AC measurement assumes  $t_T = 1$  ns. Reference level for timing of input signals is 1.4V.
2. Load condition is  $CL = 50$  pF.
3. Maximum value is a reference value and a device may work at a slower untested clock rate.
4.  $t_{OH}$ ,  $t_{LZ}$ , and  $t_{HZ}$  define the times at which the output level achieves  $\pm 200$ mV.
5. All the latency timings are measured in terms of clock period  $t_{CLK}$ .

**Table 1: Command Truth Table**

Function	CKE		CS#	RAS#	CAS#	WE#	DQM	BA	A10 (AP)	ADDR	Notes
	Previous	Current									
Mode Register Set	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	L	H	H	X	X	X	X	X	X	X	
			L	H	H	H					
Single Bank Precharge	H	X	L	L	H	L	X	BA	L	X	2
Precharge all Banks	H	X	L	L	H	L	X	X	H	X	
Bank Activate	H	X	L	L	H	H	X	BA	Row Address		2
Write	H	X	L	H	L	L	X	BA	L	Column	2
Write with Auto-Precharge	H	X	L	H	L	L	X	BA	H	Column	2
Read	H	X	L	H	L	H	X	BA	L	Column	2
Read with Auto-Precharge	H	X	L	H	L	H	X	BA	H	Column	2
Burst Termination	H	X	L	H	H	L	X	X	X	X	3, 8
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	L	H	H	X	X	X	X	X	X	X	4
Data Write/Output Enable	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	H	X	X	X	X	X	H	X	X	X	5
Power Down Mode Entry	H	L	H	X	X	X	X	X	X	X	6, 7
			L	H	H	X					
Power Down ModeExit	L	H	H	X	X	X	X	X	X	X	6, 7
			L	H	H	X					

**Notes:**

1. All of the SDRAM operations are defined by states of CS#, WE#, RAS#, CAS#, and DQM at the positive rising edge of the clock.
2. Bank Select (BA0, BA1): BA0, BA1 = 0,0 selects banks 0; BA0, BA1 = 0,1 selects bank 1; BA0, BA1 = 1,0 selects bank 2; BA0, BA1 = 1,1 selects bank 3.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS# latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. (If this command is issued during a burst operation, the device state will be clock suspend mode.) The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t<sub>REF</sub>) of the device. One clock delay is required for mode entry and exit.
7. If CS# is low, then when CKE returns high, no command is registered into the chip for one clock cycle. A No Operation (NOP) or Device Deselect command is required on the next edge following CKE going high.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

**Table 2: Mode Register Table**

Address	BA0,1	An~A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	Operation Mode			CAS Latency			BT	Burst Length		

Operation Mode				CAS Latency				Burst Type		Burst Length				
A9	A8	A7	Mode	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	0	Prog. Burst length	0	0	0	Rsvd.	0	Sequential	0	0	0	1	1
1	0	0	Burst Read/Single Write	0	0	1	Rsvd.	1	Interleave	0	0	1	2	2
				0	1	0	2			0	1	0	4	4
				0	1	1	3			0	1	1	8	8
				1	0	0	Rsvd.			1	0	0	Rsvd.	Rsvd.
				1	0	1	Rsvd.			1	0	1	Rsvd.	Rsvd.
				1	1	0	Rsvd.			1	1	0	Rsvd.	Rsvd.
				1	1	1	Rsvd.			1	1	1	Full Page	Rsvd.

**Note:**

1. RFU (Reserved for future use) should stay "0" during MRS cycle.

**Serial Presence Detect Table**

Byte No.	Byte Description	Value Supported	Value in Hex
0	# of bytes written into serial memory at module manufacturer	128 Bytes	80h
1	Total # of bytes of SPD memory device	256 Bytes	08h
2	Fundamental memory type	SDRAM	04h
3	# of row address on this assembly	13	0Dh
4	# of column address on this assembly	11	0Bh
5	# of module rows on this assembly	2	02h
6	Data width of this assembly	72	48h
7	.....Data width of this assembly	-	00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM cycle time from clock @ CAS latency of 3.0	7.5ns	75h
10	SDRAM access time from clock @ CAS latency of 3.0	5.4ns	54h
11	DIMM configuration type	ECC	02h
12	Refresh rate & type	SR, 7.8	82h
13	Primary SDRAM width	8	08h
14	Error checking SDRAM width	8	08h
15	Minimum clock delay for back-to-back random column address	1	01h
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8, Full	8Fh
17	SDRAM device attributes : # of banks on SDRAM device	4	04h
18	SDRAM device attributes : CAS latency	2.0, 3.0	06h
19	SDRAM device attributes : CS latency	CS# Latency = 0	01h
20	SDRAM device attributes : Write latency	WE# Latency = 0	01h
21	SDRAM module attributes	Non-registered/non-buffered DQM, address & control, PLL	04h

**Serial Presence Detect Table (Contd.)**

Byte No.	Byte Description	Value Supported	Value in Hex
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto pre- charge	0Eh
23	SDRAM cycle time from clock @ CAS latency of 2.0	10.0ns	A0h
24	SDRAM access time from clock @ CAS latency of 2.0	6.0ns	60h
25	SDRAM cycle time from clock @ CAS latency of 1.0	-	00h
26	SDRAM access time from clock @ CAS latency of 1.0	-	00h
27	Minimum row precharge time (=tRP)	20ns	14h
28	Minimum row active to row active delay (=tRRD)	15ns	0Fh
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h
30	Minimum activate precharge time (=tRAS)	45ns	2Dh
31	Module row density	512MB	80h
32	Command and Address signal input setup time	1.5ns	15h
33	Command and Address signal input hold time	0.8ns	08h
34	Data signal input setup time	1.5ns	15h
35	Data signal input hold time	0.8ns	08h
36~61	Superset information (may be used in future)	Not used	00h
62	SPD data revision code	1.2	12h
63	Checksum for bytes 0~62		AAh
64	Manufacturer JEDEC ID code	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	Not Used	FFh
72	Manufacturing location	See Note 1	xxh
73~90	Manufacturer part #	SG572288578DR3R	P. No
91	Manufacturer revision code	Rev. 0	00h
92	.....Manufacturer revision code	None	FFh

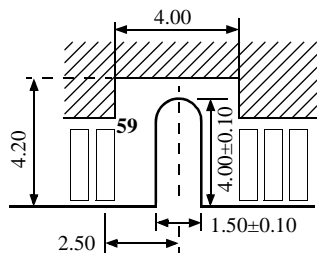
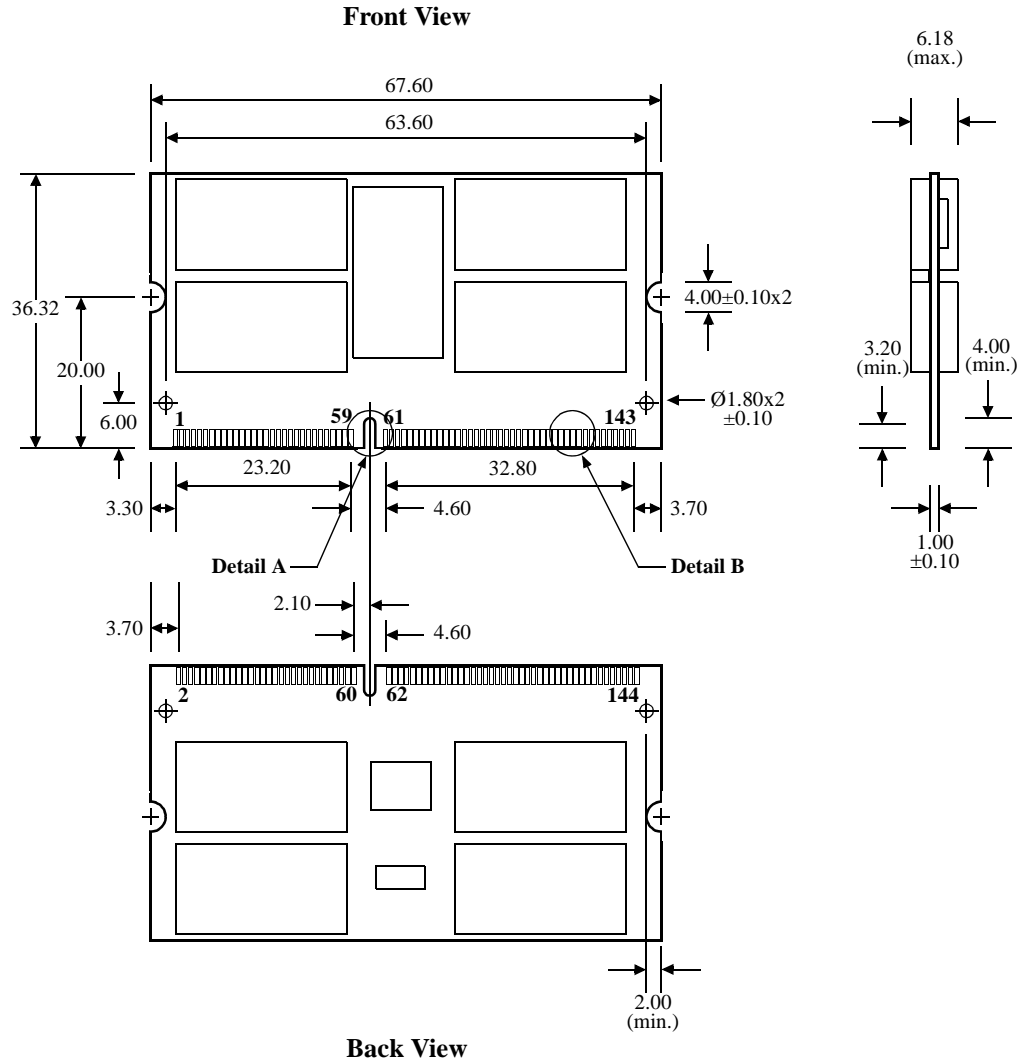
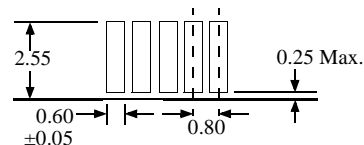
**Serial Presence Detect Table (Contd.)**

Byte No.	Byte Description	Value Supported	Value in Hex
93	Manufacturing data (Year)	Date	Date
94	Manufacturing data (Week)	Date	Date
95~98	Assembly serial #	Serial Number	S. No
99~125	Manufacturer specific data	SMART Modular Technologies	
126	System frequency for 100MHz	100MHz	64h
127	Intel Specification details	2, 3	87h
128~255	Unused storage locations		FFh

**Note:**

- Manufacturing Location:
  - 00h - Undefined,
  - 01h - Fremont, USA,
  - 02h - Aguada, Puerto Rico,
  - 03h - East Kilbride, Scotland,
  - 04h - Penang, Malaysia,
  - 05h - Bangalore, India,
  - 06h - Sao Paulo, Brazil,
  - 07h - Aguadilla, Puerto Rico,
  - 08h - Mayaguez, Puerto Rico,
  - 09h - Santo Domingo, Dominican Republic,
  - 0Ah - Dongguan, China,

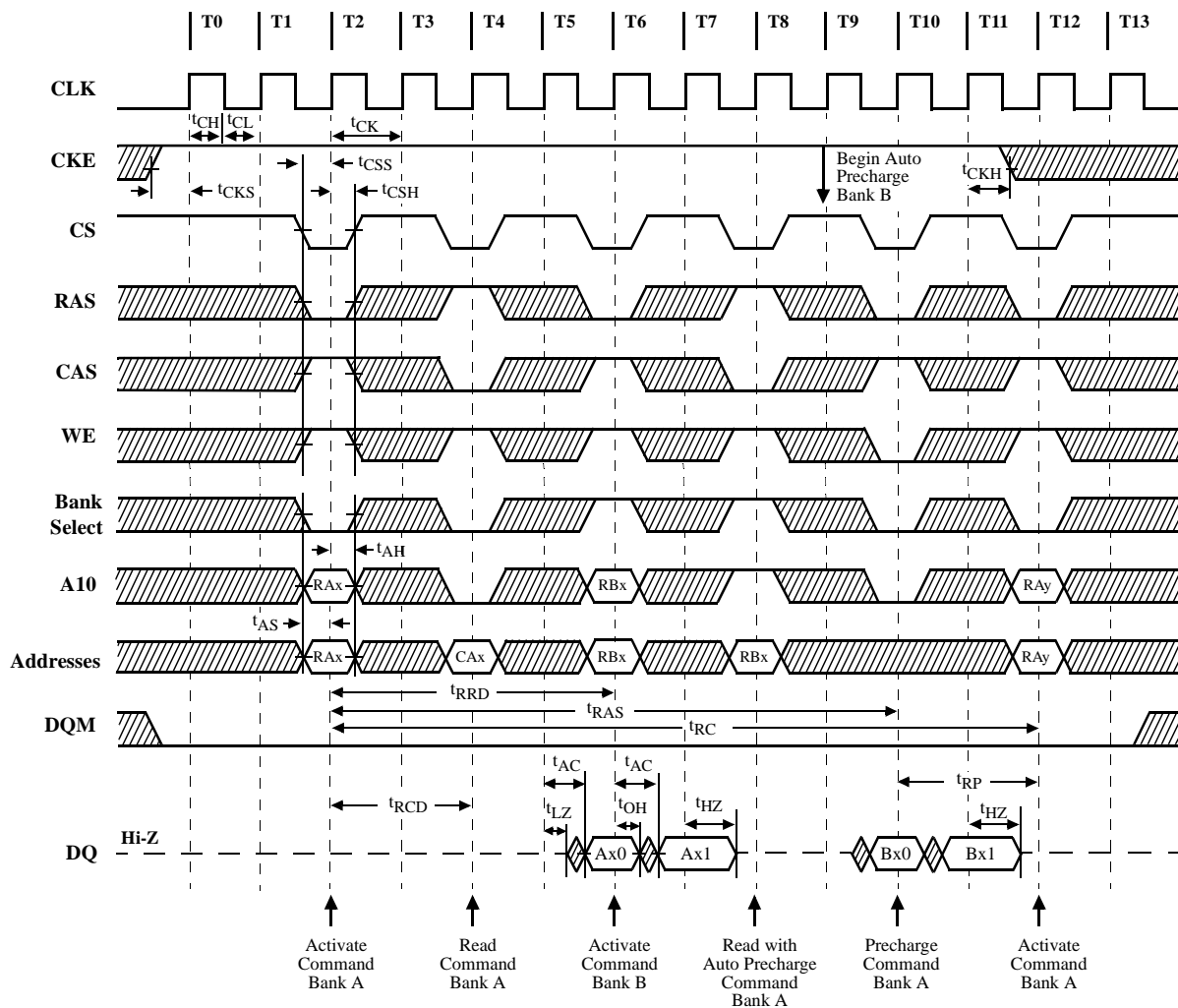


**Physical Dimensions**
144-pin 3.3V SODIMM Module

**Detail A : Position of Voltage Notch**

**Detail B : Edge Connector**

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

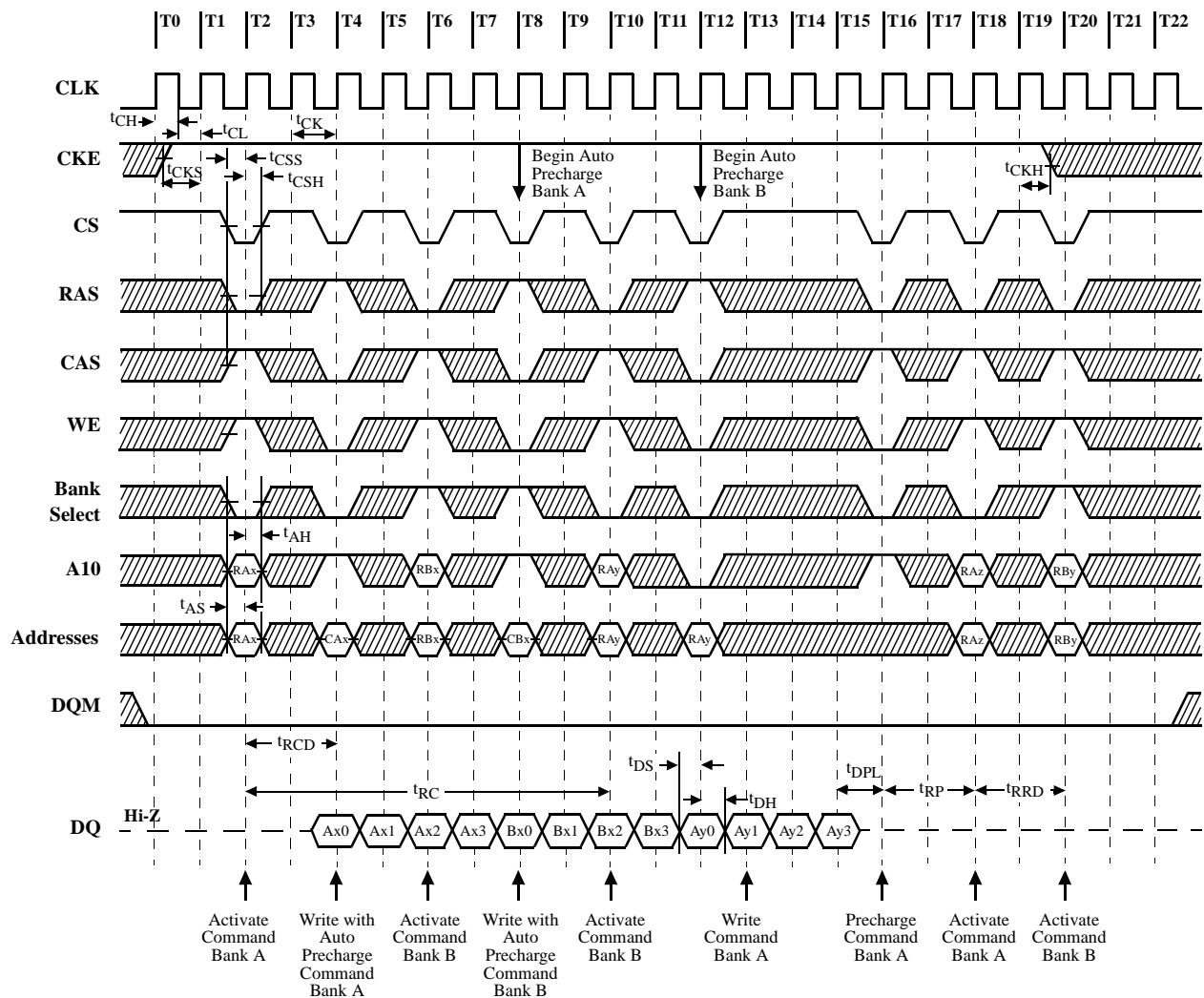
## Timing Waveforms

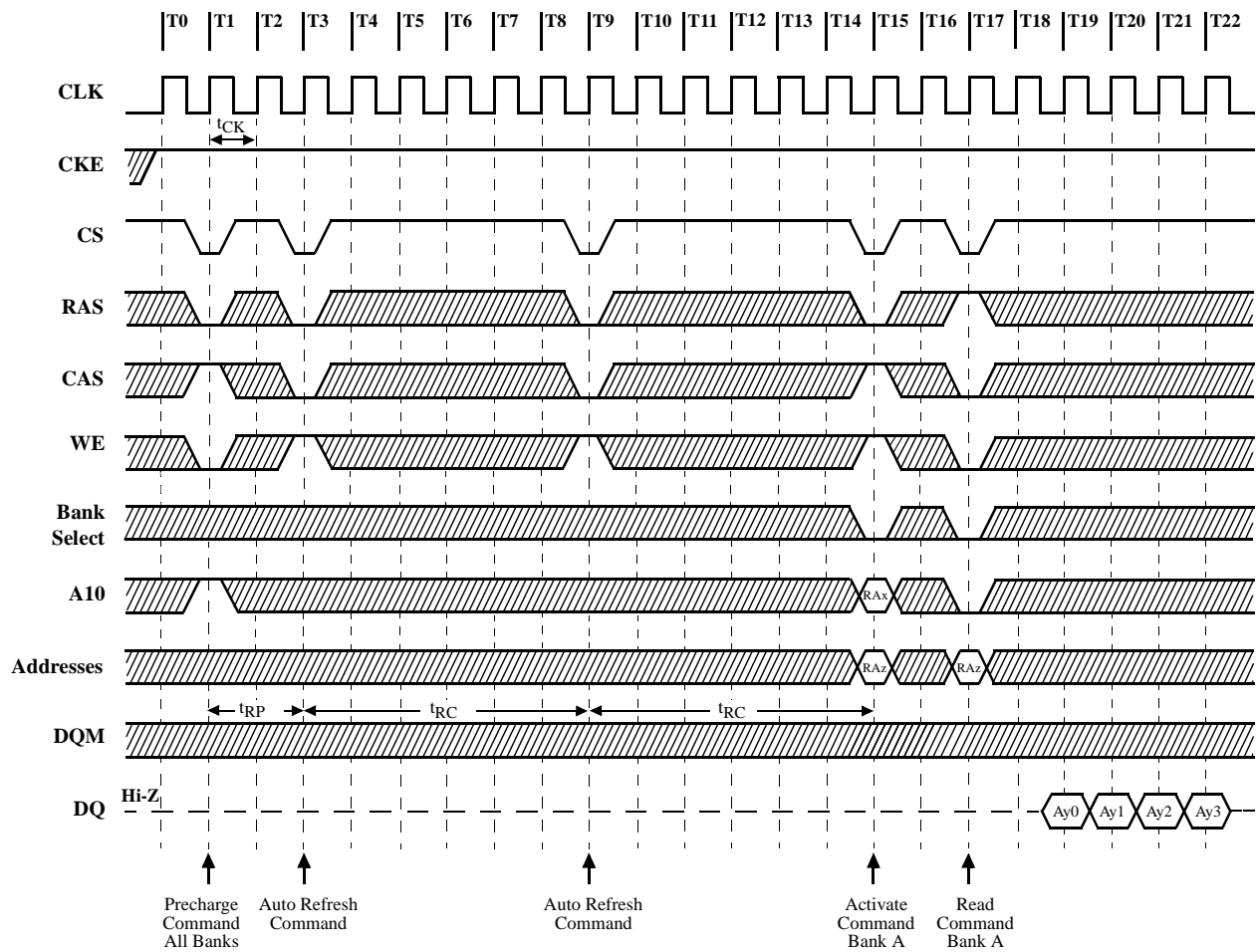
### Read Cycle

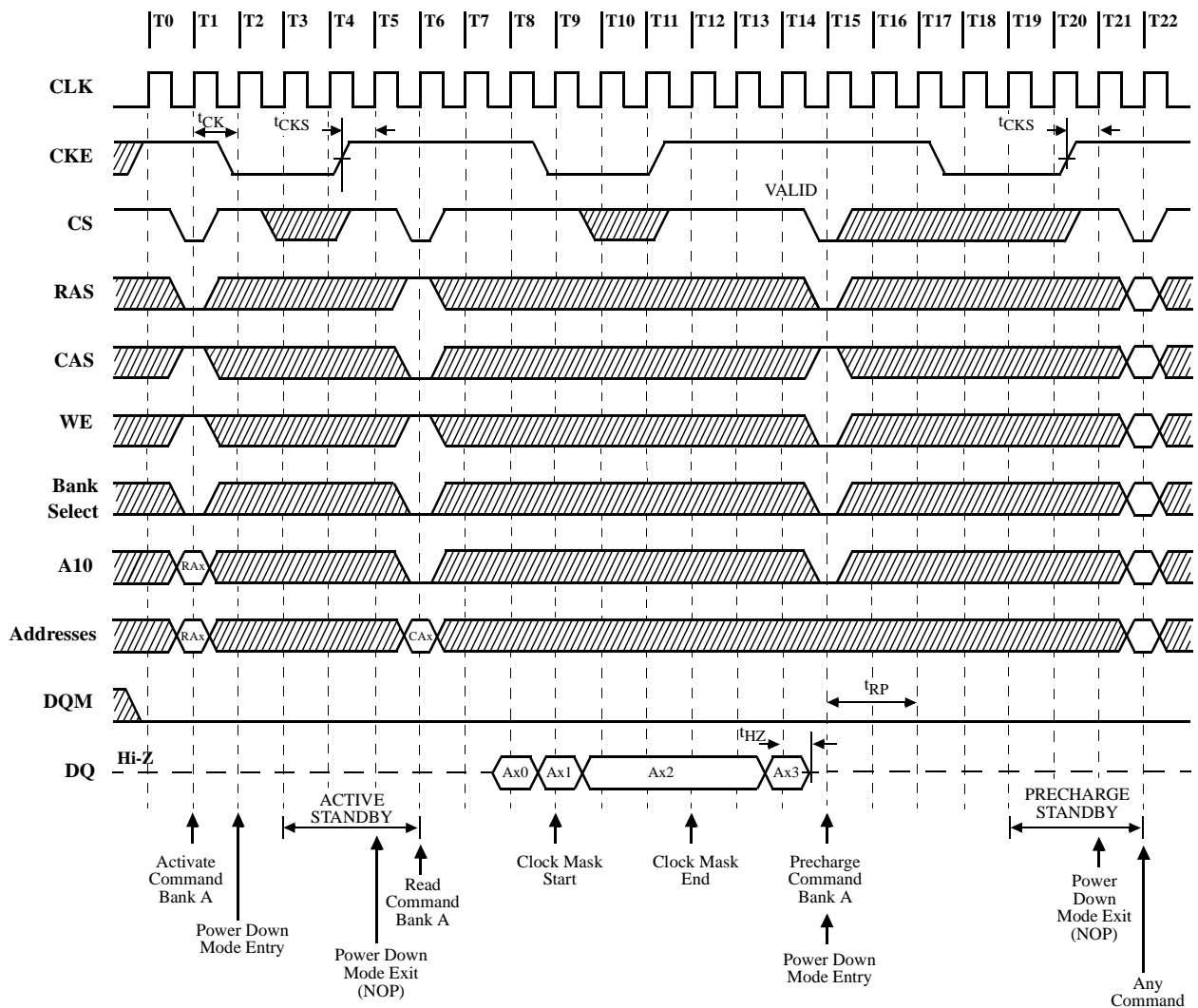




**Write Cycle**



**Auto Refresh (CBR) Cycle**


**Power Down Mode and Clock Mask**


**Part Number Decode**

S   G   5   72   28   8   5   7   8   D   R   3   R  
 (1)   (2)   (3)   (4)   (5)   (6)   (7)   (8)   (9)   (10)   (11)   (12)   (13)

- (1) **SMART Modular Technologies**
- (2) **Module Process Technology**  
G : Green Module (RoHS Compliant)
- (3) **Product Category**  
5 : SDRAM SIMM/DIMM
- (4) **Module Data Bus Width**  
72 : x72
- (5) **Module Address Depth**  
28 : 128M
- (6) **Device Data Width**  
8 : x8
- (7) **Special Device Feature**  
5 : Standard (4 Bank SDRAM)
- (8) **Voltage/Mode**  
7 : 3.3V, Synchronous DRAM
- (9) **Refresh/Power**  
8 : 8K Ref./Standard Power
- (10) **Module Configuration**  
D : 144 pin SODIMM Unbuffered, ECC
- (11) **Device Physicals**  
R : Depth Stacked Device Based
- (12) **CAS Latency**  
3 : CL = 3.0 only
- (13) **Cycle Time (Clock Speed)**  
R : 7.5ns (Intel PC133/133 MHz)  
tRP = 3, tRCD = 3

Note : "U" in the part number should be replaced by user specified option.

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