Ordering Information		
Part Numbers	**Description**	**Module Speed**
SM572288FD8DZFO1	128Mx72 (1GB), DDR, 200-pin SO-DIMM, Unbuffered, PLL, ECC, 64Mx8 Based, PC3200, DDR400B, 31.75mm, 22Ω DQ termination.	PC3200 @ CL 3.0
SG572288FD8DZFO1	128Mx72 (1GB), DDR, 200-pin SO-DIMM, Unbuffered, PLL, ECC, 64Mx8 Based, PC3200, DDR400B, 31.75mm, 22Ω DQ termination, Green Module.	PC3200 @ CL 3.0

Revision History

- **March 24, 2005**
  Datasheet released.

1GByte (128Mx72) DDR SDRAM Module - 64Mx8 based 200-pin SO-DIMM, Unbuffered, PLL, ECC

Features

- Standard : JEDEC Pinout
- Configuration : ECC
- Cycle Time : 5.0ns
- CAS# Latency : 2.5, 3.0
- Burst Length : 2, 4, 8
- Burst Type : Sequential/Interleave
- No. of Internal Banks per SDRAM : 4
- Operating Voltage : 2.6V
- Refresh : 8K/64ms
- Device Physicals : FBGA
- Lead Finish : Gold
- Length x Height : 67.60mm x 31.75mm
- No. of sides : Double-sided
- Mating Connector (Examples)
  Horizontal : AMP-1376408-1

200-pin DDR SO-DIMM Pin List

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{REF}	2	V_{REF}	51	V_{SS}	52	V_{SS}	101	A9	102	A8	151	DQ42	152	DQ46
3	V_{SS}	4	V_{SS}	53	DQ19	54	DQ23	103	V_{SS}	104	V_{SS}	153	DQ43	154	DQ47
5	DQ0	6	DQ4	55	DQ24	56	DQ28	105	A7	106	A6	155	V_{DD}	156	V_{DD}
7	DQ1	8	DQ5	57	V_{DD}	58	V_{DD}	107	A5	108	A4	157	V_{DD}	158	CLK1#
9	V_{DD}	10	V_{DD}	59	DQ25	60	DQ29	109	A3	110	A2	159	V_{SS}	160	CLK1
11	DQS0	12	DM0	61	DQS3	62	DM3	111	A1	112	A0	161	V_{SS}	162	V_{SS}
13	DQ2	14	DQ6	63	V_{SS}	64	V_{SS}	113	V_{DD}	114	V_{DD}	163	DQ48	164	DQ52
15	V_{SS}	16	V_{SS}	65	DQ26	66	DQ30	115	A10/AP	116	BA1	165	DQ49	166	DQ53
17	DQ3	18	DQ7	67	DQ27	68	DQ31	117	BA0	118	RAS#	167	V_{DD}	168	V_{DD}
19	DQ8	20	DQ12	69	V_{DD}	70	V_{DD}	119	WE#	120	CAS#	169	DQS6	170	DM6
21	V_{DD}	22	V_{DD}	71	CB0	72	CB4	121	CS0#	122	CS1#	171	DQ50	172	DQ54
23	DQ9	24	DQ13	73	CB1	74	CB5	123	DU	124	DU	173	V_{SS}	174	V_{SS}
25	DQS1	26	DM1	75	V_{SS}	76	V_{SS}	125	V_{SS}	126	V_{SS}	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	DQS8	78	DM8	127	DQ32	128	DQ36	177	DQ56	178	DQ60
29	DQ10	30	DQ14	79	CB2	80	CB6	129	DQ33	130	DQ37	179	V_{DD}	180	V_{DD}
31	DQ11	32	DQ15	81	V_{DD}	82	V_{DD}	131	V_{DD}	132	V_{DD}	181	DQ57	182	DQ61
33	V_{DD}	34	V_{DD}	83	CB3	84	CB7	133	DQS4	134	DM4	183	DQS7	184	DM7
35	CLK0	36	V_{DD}	85	DU	86	DU	135	DQ34	136	DQ38	185	V_{SS}	186	V_{SS}
37	CLK0#	38	V_{SS}	87	V_{SS}	88	V_{SS}	137	V_{SS}	138	V_{SS}	187	DQ58	188	DQ62
39	V_{SS}	40	V_{SS}	89	CLK2	90	V_{SS}	139	DQ35	140	DQ39	189	DQ59	190	DQ63
41	DQ16	42	DQ20	91	CLK2#	92	V_{DD}	141	DQ40	142	DQ44	191	V_{DD}	192	V_{DD}

(All specifications of this module are subject to change without notice.)

200-pin DDR SO-DIMM Pin List (contd.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
43	DQ17	44	DQ21	93	V_{DD}	94	V_{DD}	143	V_{DD}	144	V_{DD}	193	SDA	194	SA0
45	V_{DD}	46	V_{DD}	95	CKE1	96	CKE0	145	DQ41	146	DQ45	195	SCL	196	SA1
47	DQS2	48	DM2	97	NC	98	NC	147	DQS5	148	DM5	197	V_{DDSPD}	198	SA2
49	DQ18	50	DQ22	99	A12	100	A11	149	V_{SS}	150	V_{SS}	199	V_{DDID} [1]	200	DU

Note:
1. Pin 199 (V_{DDID}) is not connected on this module. Therefore V_{DDQ} of all the DDR devices is same as V_{DD}.

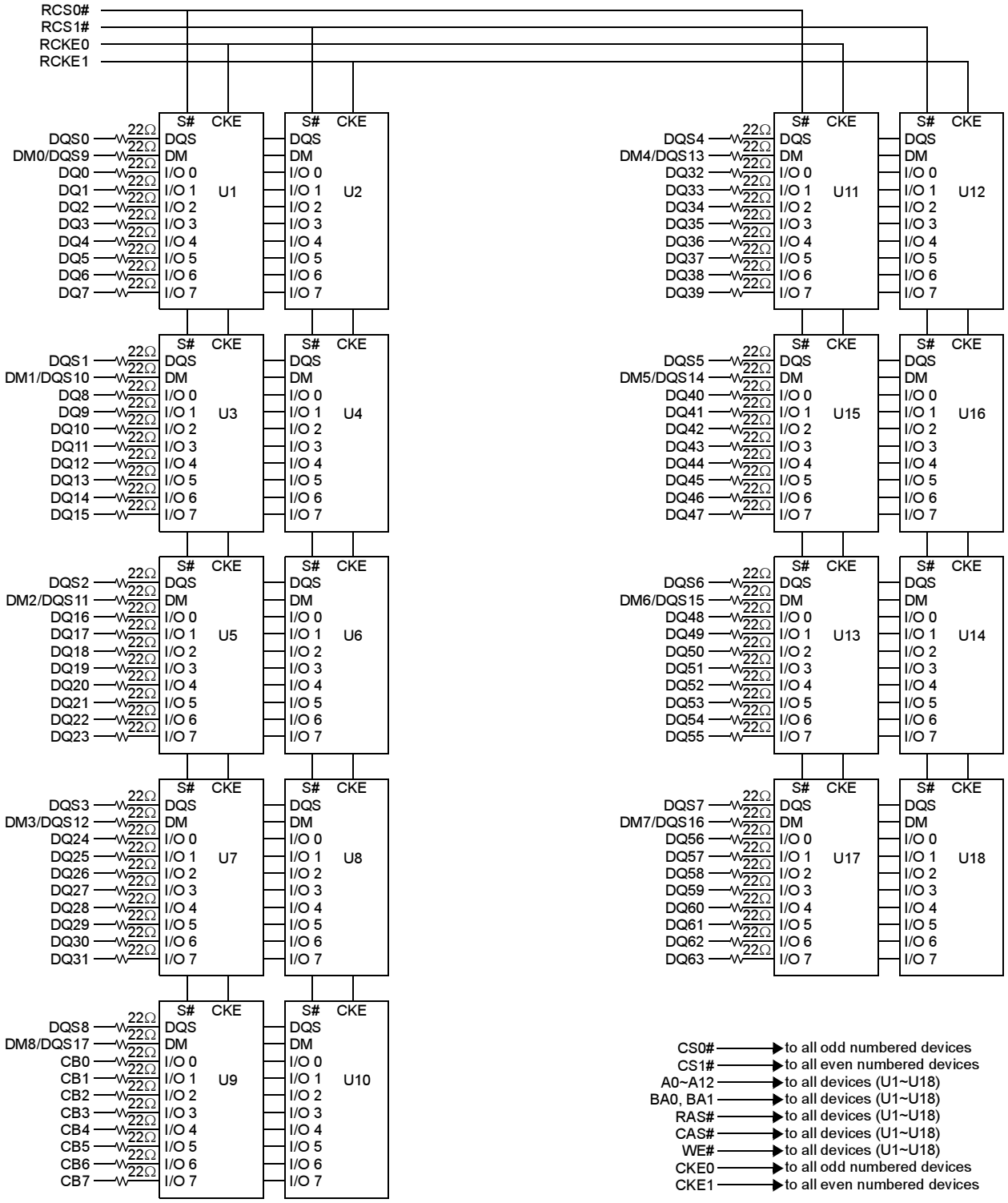
Pin Description Table

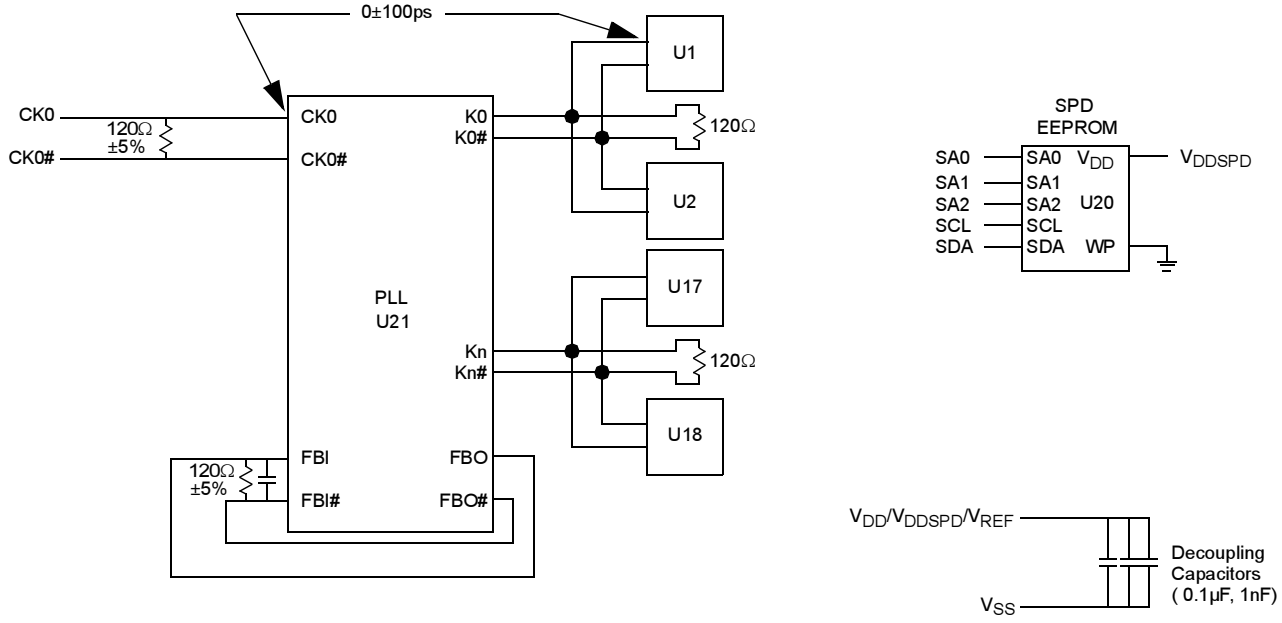
Symbol	Type	Polarity	Function
CLK0, CLK0# CLK1, CLK1# CLK2, CLK2#	SSTL (Inputs)	Crossing Point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CLK and falling edge of CLK#. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	SSTL	Active High	Activates the SDRAM CLK signal when high and deactivates the CLK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#, CS1#	SSTL	Active Low	Enables the associated DDR SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	SSTL	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0, BA1	SSTL	-	Selects which of the four internal SDRAM banks is activated.
A0~A9, A10/AP, A11~A12	SSTL	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA9, CA11) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0~DQ63 CB0~CB7	SSTL	-	Data Input/Output pins.
DM0~DM8	SSTL	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0~DQS8	SSTL	Negative & Positive Edge	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR SDRAMs and is sent at the leading edge of the data window.

Pin Description Table (Contd.)

Symbol	Type	Polarity	Function
SA0~SA2	LVTTL	-	These signals are tied on the system to either V_{SS} or V_{DD} to configure the serial SPD.
SDA	LVTTL	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected on the system board from the SDA bus line to V_{DD} to act as a pullup.
SCL	LVTTL	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected on the system board from the SCL bus line to V_{DD} to act as a pullup.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	-	Reference voltage for SSTL2 inputs.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports both 2.3 Volt and 3.3 Volt operation).
V_{DDID}	Supply	-	V_{DD} Identification flag (not used).
NC	-	-	No Connection.
DU	-	-	Do Not Use Pins.

Block Diagram

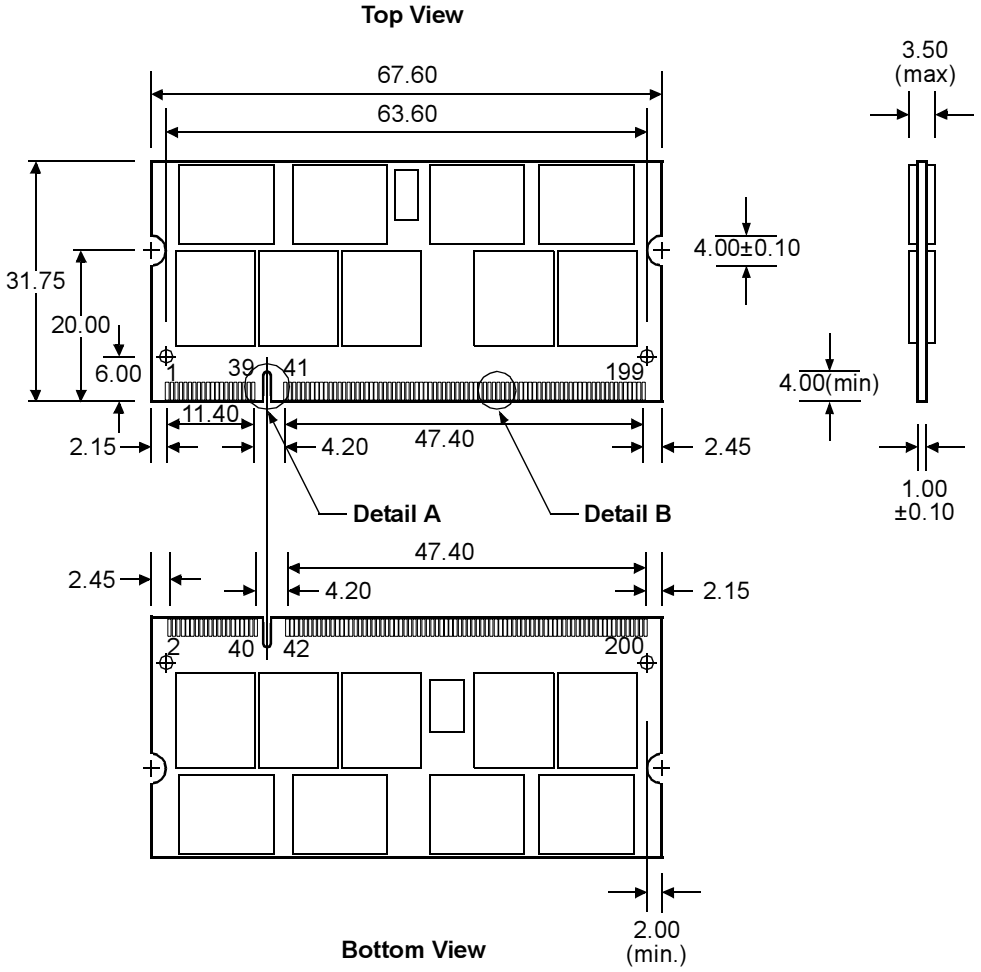


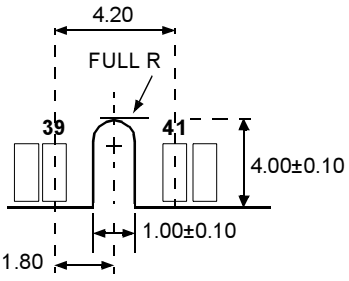


Notes:
1. Data bits may be swapped within a device. However, DQ/DQS/DM relationship is maintained as shown.
2. Only two PLL outputs are shown above. All additional PLL outputs will be wired in a similar manner.

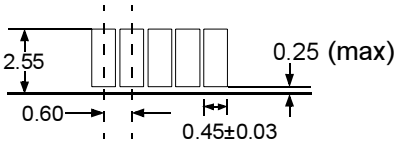
Physical Dimensions

200-pin SO-DIMM Module





Detail A : Position of Voltage Notch



Detail B : Edge Connector

(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Serial Presence Detect Table

Byte No.	Byte Description	Value Supported	Value in Hex
0	# of bytes written into serial memory at module manufacturer	128 Bytes	80h
1	Total # of bytes of SPD memory device	256 Bytes	08h
2	Fundamental memory type	SDRAM DDR	07h
3	# of row address on this assembly	13	0Dh
4	# of column address on this assembly	11	0Bh
5	# of module rows on this assembly	2	02h
6	Data width of this assembly	72	48h
7	.....Data width of this assembly	-	00h
8	Voltage interface standard of this assembly	SSTL	04h
9	SDRAM cycle time from clock @ CAS latency of 3.0	5.0ns	50h
10	SDRAM access time from clock @ CAS latency of 3.0	0.65ns	65h
11	DIMM configuration type	ECC	02h
12	Refresh rate & type	SR, 7.8	82h
13	Primary SDRAM width	8	08h
14	Error checking SDRAM width	8	08h
15	Minimum clock delay for back-to-back random column address	1	01h
16	SDRAM device attributes : Burst lengths supported	2, 4, 8	0Eh
17	SDRAM device attributes : # of banks on SDRAM device	4	04h
18	SDRAM device attributes : CAS latency	2.5, 3.0	18h
19	SDRAM device attributes : CS latency	CS# Latency = 0	01h
20	SDRAM device attributes : Write latency	WE# Latency = 1	02h
21	SDRAM module attributes	Diff. CK, PLL	24h
22	SDRAM device attributes : General	V_{DD} ± 0.2V	C0h
23	SDRAM cycle time @ CAS latency of 2.5	6.0ns	60h
24	SDRAM access time @ CAS latency of 2.5	0.65ns	65h
25	SDRAM cycle time @ CAS latency of 2.0	-	00h
26	SDRAM access time @ CAS latency of 2.0	-	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Value in Hex
27	Minimum row precharge time (=tRP)	15ns	3Ch
28	Minimum row active to row active delay (=tRRD)	10ns	28h
29	Minimum RAS to CAS delay (=tRCD)	15ns	3Ch
30	Minimum activate precharge time (=tRAS)	40ns	28h
31	Module row density	512MB	80h
32	Command and Address signal input setup time	0.60ns	60h
33	Command and Address signal input hold time	0.60ns	60h
34	Data signal input setup time	0.40ns	40h
35	Data signal input hold time	0.40ns	40h
36~40	Reserved for VCSDRAM	Not used	00h
41	Device Minimum activate/auto-refresh time (=tRC)	55ns	37h
42	Device Minimum auto-refresh to active/auto-refresh time (=tRFC)	70ns	46h
43	Maximum device cycle time (=tCK max)	12ns	30h
44	Device DQS-DQ skew for DQS and associated DQ signals (=tDQSQ max)	0.40	28h
45	Device read data hold skew factor (=tQHS)	0.50	50h
46	Superset Information (reserved for future use)	-	00h
47	SDRAM Module Attributes - DDR DIMM Height	1.125” - 1.25”	02h
48-61	Superset Information (reserved for future use)	-	00h
62	SPD data revision code	1.0	10h
63	Checksum for bytes 0~62		D4h
64	Manufacturer JEDEC ID code	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	SMART’s ID	94h
66~71	.....Manufacturer JEDEC ID code	Not Used	00h
72	Manufacturing location	See Note 1	01h
73~90	Manufacturer part #	SM572288FD8DZFO1	P. No
91	Manufacturer revision code	Rev 0	00h
92	.....Manufacturer revision code	None	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Value in Hex
93	Manufacturing data (Year)	Date	Date
94	Manufacturing data (Week)	Date	Date
95~98	Assembly serial #	Serial Number	S. No
99~125	Manufacturer specific data	SMART Modular Technologies	
126-127	Unused storage locations		00h
128-255	Unused storage locations		FFh

Note:

1. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

Mode Register Table Definition

The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, and an operating mode, as shown in the table below. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing). In the table below, note that n = 11 for 128Mb devices, n = 12 for 256Mb and 512Mb devices, and n = 13 for 1Gb devices.

Address Bus	BA1	BA0	An	..	..	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register Bits	Mn+2	Mn+1	Mn	..	..	M9	M8	M7	M6	M5	E4	E3	E2	E1	E0
	0	0	Operating Mode						CAS Latency			BT	Burst Length		

M2	M1	M0	Burst Length
0	0	1	2
0	1	0	4
0	1	1	8

M3	Burst Type
0	Sequential
1	Interleave

M6	M5	M4	CAS Latency
0	1	1	3.0
1	1	0	2.5
0	1	0	2.0*

M9	..	..	M9	M8	M7	Operating Mode
0	0	0	0	0	0	Normal Operation
0	0	0	0	1	0	Reset DLL

* This option is not supported by all vendors. Please check SPD byte 18 to confirm if the CAS Latency is supported by this module.

Extended Mode Register Table Definition

The Extended Mode Register is used to control functions beyond those controlled by Mode Register. This definition includes DLL Enable/Disable, Output Drive Strength, and QFC Enable/Disable as shown in table below. The Mode Register is programmed via the MODE REGISTER SET command (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a MODE REGISTER SET Command to the Mode Register (with BA0 = 0 and BA1 = 0) to reset the DLL. In the table below, note that n = 11 for 128Mb devices, n = 12 for 256Mb and 512Mb devices, and n = 13 for 1Gb devices. QFC# option is not currently supported.

Address Bus	BA1	BA0	An	..	..	..	..	..	..	..	A4	A3	A2	A1	A0
Mode Register Bits	En+2	En+1	En	..	..	..	..	..	..	..	E4	E3	E2	E1	E0
	0	1	Operating Mode										QFC#	DS	DLL

E0	DLL
0	Enable
1	Disable

E1	Drive Strength
0	Normal
1	Weak

En	. .	. .	E5	E4	E3	Operating Mode
0	0	0	0	0	0	Normal Operation
-	-	-	-	-	-	All other states reserved

Commands

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

Truth Table - Commands

Name (Function)	CS#	RAS#	CAS#	WE#	ADDR	Notes
Deselect (NOP)	H	X	X	X	X	9
No Operation (NOP)	L	H	H	H	X	9
Active (Select bank and activate Row)	L	L	H	H	Bank/Row	3
Read (Select bank and column and start Read burst)	L	H	L	H	Bank/Col	4
Write (Select bank and column and start Write burst)	L	H	L	L	Bank/Col	4
Burst Terminate	L	H	H	L	X	8
Precharge (Deactivate Row in bank or banks)	L	L	H	L	Code	5
Auto Refresh or Self Refresh (Enter Self Refresh Mode)	L	L	L	H	X	6, 7
Load Mode Register	L	L	L	L	Op-Code	2

Truth Table - DM Operation (Note 10)

Name (Function)	DM	DQS
Write Enable	L	Valid
Write Inhibit	H	X

Note:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. BA0–BA1 select either the Base or the Extended Mode Register (BA0 = 0, BA1 = 0 selects Mode Register; BA0 = 1, BA1 = 0 selects Extended Mode Register; other combinations of BA0–BA1 are reserved; A0-An provide the op–code to be written to the selected Mode Register).
3. BA0–BA1 provide bank address and A0-An provide row address.
4. BA0–BA1 provide bank address; A0–Ai provide column address; A10 HIGH enables the autoprecharge feature (nonpersistent), A10 LOW disables the auto precharge feature.
5. A10 LOW: BA0–BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0–BA1 are “Don’t Care.”
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
8. Applies only to read bursts with autoprecharge disabled; this command is undefined (and should not be used) for read bursts with autoprecharge enabled, and for write bursts.
9. DESELECT and NOP are functionally interchangeable.
10. Used to mask write date; DM should be asserted in the same cycle as DQ that needs to be masked.

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-1.0 ~ 3.6	V
Voltage on V_{DDSPD} relative to V_{SS}	V_{DDSPD}	-1.0 ~ 5.5	V
Power Dissipation	P_T	27	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Short Circuit Output Current	I_{OS}	50	mA

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	2.5	2.6	2.7	V
I/O Supply Voltage	V_{DDQ}	2.5	2.6	2.7	V
I/O Reference Voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V
I/O Termination Voltage	V_{TT}	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
SPD Voltage	V_{DDSPD}	2.5	-	5.5	V
Input High Voltage	$V_{IH(DC)}$	V_{REF} + 0.15	-	V_{DD} + 0.3	V
Input Low Voltage	$V_{IL(DC)}$	-0.3	-	V_{REF} - 0.15	V
Input Voltage Level, CK and CK#	$V_{IN(DC)}$	-0.3	-	V_{DDQ} + 0.3	V
Input Differential Voltage, CK and CK#	$V_{ID(DC)}$	0.36	-	V_{DDQ} + 0.6	V
Ground	V_{SS}	0	0	0	V

Notes:

1. V_{REF} is expected to track variation in V_{DDQ}. V_{REF} = 0.5 x V_{DDQ}.
2. Peak to peak noise on V_{REF} may not exceed 2% V_{REF}.
3. V_{TT} is not used on the module. It is the voltage used on the system board to terminate all the signals. However, this supply should track the variations in DC level of V_{REF}.

DC Characteristics (Contd.)
Capacitance
(V_{DD} = 2.6V±0.1V, T_A = +25°C, f = 100MHz)

Parameter	Symbol	Max	Unit
Input Capacitance (Address, RAS#, CAS#, WE#)	C_{I1}	54	pF
Input Capacitance (CS0#, CS1#, CKE0, CKE1)	C_{I2}	27	pF
Input Capacitance (CK0, CK0#)	C_{I3}	10	pF
Input Capacitance (DQS0~DQS8, DM0~DM8)	C_{I4}	10	pF
Input/Output Capacitance (DQ0~DQ63, CB0~CB7)	$C_{I/O}$	10	pF

Leakage Currents
(V_{DD} = 2.6V±0.1V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Test conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{DD}$	-36	36	µA
Output Leakage Current	I_{OZ}	$0V \le V_{out} \le V_{DD}$ DQ's are disabled	-10	10	µA
Output High Current	I_{OH}	$V_{OUT} = V_{DDQ} - 0.373$	-16.8	-	mA
Input Leakage Current	I_{OL}	$V_{OUT} = 0.373$	16.8	-	mA

AC Operating Conditions
(V_{DD} = 2.6V±0.1V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Input High Logic Voltage	$V_{IH(AC)}$	V_{REF} + 0.31	-	V	1, 2
Input Low Logic Voltage	$V_{IL(AC)}$	-	V_{REF} - 0.31	V	1, 2
Input differential voltage, CK and CK# inputs	$V_{ID(AC)}$	0.7	V_{DDQ} + 0.6	V	1, 2, 3
Input crossing point voltage, CK and CK# inputs	$V_{IX(AC)}$	$0.5*V_{DDQ}$ - 0.2	$0.5*V_{DDQ}$ + 0.2	V	1, 2, 3

Notes:
1. Input slew rate is 1V/ns.
2. Inputs are not recognized as valid until V_{REF} stabilizes.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
4. The value of V_{IX} is expected to equal $0.5*V_{DDQ}$ of the transmitting device and must track variations in the DC level of the same.

DC Characteristics (Contd.)
(V_{DD} = 2.6V±0.1V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Max	Unit	Notes
		5.0ns CL 3.0		
OPERATING CURRENT: One Bank; Active–Precharge; tRC = tRC MIN; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cyle; address and control inputs changing once per clock cycle.	IDD0	1623	mA	1
OPERATING CURRENT: One Bank; Active–Read–Precharge; Burst = 2; tRC = tRC MIN; CL = 3.0; tCK = tCK MIN; Iout = 0 mA; Address and control inputs changing once per clock cycle.	IDD1	1713	mA	1
PRECHARGE POWER–DOWN STANDBY CURRENT: All banks idle; power–down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD2P	372	mA	2
IDLE STANDBY CURRENT: CS# ≥ Vih (MIN); All banks idle; CKE ≥ Vih (MIN); tCK = tCK MIN; Address and other control inputs changing once per clock cycle	IDD2N	948	mA	2
ACTIVE POWER–DOWN STANDBY CURRENT: One bank active; power–down mode; CKE ≤ Vil (MAX); tCK = tCK MIN	IDD3P	867	mA	1
ACTIVE STANDBY CURRENT: CS# ≥ Vih (MIN); CKE ≥ Vih (MIN); One bank; Active–Precharge; tRC = tRAS MAX; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle.	IDD3N	1146	mA	1
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 3.0; tCK = tCK MIN; Iout = 0mA	IDD4R	1623	mA	1
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; CL = 3.0; tCK = tCK MIN; DQ, DM and DQS inputs changing twice per clock cycle	IDD4W	1668	mA	1
AUTO REFRESH CURRENT: tRC = tRFC (MIN)	IDD5	2928	mA	3
SELF REFRESH CURRENT: CKE ≤ 0.2 V	IDD6	93.6	mA	
OPERATING CURRENT: Four Bank operation;Four bank interleaving READs (BL = 4) with auto precharge. tRC= MIN tRC allowed; tCK =tCK MIN; Address and control inputs change only during Active READ, or WRITE commands.	IDD7	3513	mA	1

Notes:
1. One module bank active. Second bank in active standby.
2. All module banks idle
3. One bank in refresh. Second bank in active standby.
4. IDD specifications are valid after the SDRAMs are properly initialized.

Device AC Characteristics

Parameter		Symbol	5.0ns @ CL 3.0 DDR400B		Unit	Notes
			Min	Max		
Output data access time from CK/CK#		t_{AC}	-0.65	+0.65	ns	
DQS-out access time from CK/CK#		t_{DQSCK}	-0.55	+0.55	ns	
Clock high level width		t_{CH}	0.45	0.55	t_{CK}	
Clock low level width		t_{CL}	0.45	0.55	t_{CK}	
Clock half period		t_{HP}	Min(t_{CL}, t_{CH})	-	ns	6
Clock cycle time	CL=3.0	t_{CK}	5	10	ns	
	CL=2.5		6	12	ns	
	CL=2.0		-	-	ns	
DQ & DM setup time to DQS		t_{DH}	0.4	-	ns	
DQ & DM setup time to DQS		t_{DS}	0.4	-	ns	
DQ & DM input pulse width		t_{IPW}	2.2	-	ns	6
Address & Control input pulse width		t_{DIPW}	1.75	-	ns	6
Data out high impedence time from CK/CK#		t_{HZ}	-	+0.65	ns	7
Data out high impedence time from CK/CK#		t_{LZ}	-0.65	+0.65	ns	7
DQS-DQ Skew (DQS and associated DQ signals)		t_{DQSQ}	-	0.4	ns	
DQ/DQS Output hold time		t_{QH}	t_{HP}min - t_{QHS}	-	ns	8
Data Hold Skew Factor (DQS and associated DQ signals)		t_{QHS}	-	0.5	ns	
CK to valid DQS-in		t_{DQSS}	0.72	1.28	t_{CK}	
DQS-in high level width		t_{DQSH}	0.35	-	t_{CK}	
DQS-in low level width		t_{DQSL}	0.35	-	t_{CK}	
DQS falling edge to CK setup time		t_{DSS}	0.2	-	t_{CK}	
DQS falling edge to CK hold time		t_{DSH}	0.2	-	t_{CK}	
Mode Register Set Command Cycle time		t_{MRD}	2	-	ns	
Write preamble setup time		t_{WPRES}	0	-	ns	2
DQS write postamble time		t_{WPST}	0.4	0.6	t_{CK}	3
Write preamble		t_{WPRE}	0.25	-	t_{CK}	

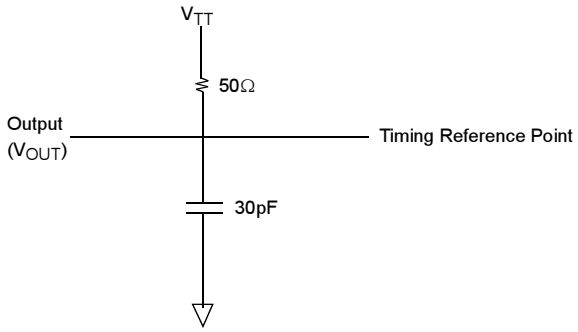
Device AC Characteristics (cont'd)

Parameter	Symbol	5.0ns @ CL 3.0 DDR400B		Unit	Notes
		Min	Max		
Address and Control Input hold time	t_{IH}	0.6	-	ns	6
Address and Control Input setup time	t_{IS}	0.6	-	ns	6
Read Preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read Postamble	t_{RPST}	0.4	0.6	t_{CK}	
Row active time	t_{RAS}	40	70K	ns	
Active to Active/AutoRefresh Period	t_{RC}	55	-	ns	
Refresh row cycle time	t_{RFC}	70	-	ns	
RAS# to CAS# delay	t_{RCD}	15	-	ns	
Row precharge time	t_{RP}	15	-	ns	
Active to Auto-Precharge Delay	t_{RAP}	15	-	ns	
Row active to Row active delay	t_{RRD}	10	-	ns	
Write recovery time	t_{WR}	15	-	ns	
Auto precharge write recovery + Precharge time	t_{DAL}	-	-	t_{CK}	
Internal write to read command delay	t_{WTR}	2	-	t_{CK}	
Exit self refresh to bank active command	t_{XSNR}	75	-	ns	4
Exit self refresh to read command	t_{XSRD}	200	-	t_{CK}	
Refresh Interval	t_{REFI}	7.8	-	µs	1

Notes:

1. Maximum burst refresh of 8.
2. The specific requirement is that DQS be valid(HIGH or LOW) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic low. If a previous write was in progress, DQS could be HIGH, LOW or transitioning from HIGH to LOW at this time, depending on t_{DQSS}.
3. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter but system performance (bus turnaround) will degrade accordingly.
4. A write command can be applied with t_{RCD} satisfied after this command.
5. Min(t_{CL},t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.
6. These parameters guarantee device timing, but they are not necessarily tested on each device.
7. t_{HZ}, and t_{LZ} transitions occur in the same access time windows as valid data transitions, These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ) or begins driving (LZ).
8. $t_{QH} = t_{HP} - X$, where t_{HP} = minimum half clock period for any given cycle and is defined by clock high or clock low (t_{CL},t_{CH}). X consists of t_{DQSQ}(max), the pulse width distortion of on-chip clock circuits, data pin to pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.
9. The CK/CK# input reference level (for timing reference to CK/CK#) is the point at which CK and CK# cross. The input reference level for signals other than CK and CK# is V_{REF}.
10. Inputs are not recognized as valid until V_{REF} stabilizes.
11. CK and CK# slew rates are ≥ 1.0V/ns.

AC Output Load Circuit Diagram



Part Number Decode

S	U	5	72	28	8	F	D	8	D	Z	F	O	1
1	2	3	4	5	6	7	8	9	10	11	12	13	

1 **SMART Modular Technologies**

2 **Module Process Technology**
M: Legacy Tin-Lead Process
G: Green Module (RoHS Compliant)

3 **Product Category**
5: SDRAM/DRAM SIMM/DIMM

4 **Module Data Bus Width**
72: x72

5 **Module Address Depth**
28: 128M

6 **Device Data Width**
8: x8

7 **Special Device Feature**
F: Standard (4 Bank SDRAM) FBGA

8 **Voltage/Mode**
D: DDR SDRAM

9 **Refresh/Power**
8: 8K Refresh/Standard Power

10 **Module Configuration**
D: Unbuffered with ECC

11 **Device Physicals**
Z: 200-pin SO-DIMM, 512Mb-based

12 **CAS Latency**
F: 2.5, 3.0

13 **Cycle Time (Clock Speed)**
O: 5.0ns (200MHz, PC3200, DDR400B)

Note : “U” in the part number should be replaced by user specified option.

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