Ordering Information	
Module Part Number	**Description**
SM572288578D03R01	128Mx72 (1GB), SDRAM, 168-pin DIMM, Unbuffered, ECC, 64Mx8 Based, CL = 3.0, PC133, 29.21mm.

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Revision History

- **June 15, 2004**
  Datasheet released.

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1GByte (128Mx72) CMOS Synchronous DRAM Module - 64Mx8 based 168-pin DIMM, Unbuffered, ECC

Features

- Standard : PC133
- Configuration : ECC
- Cycle Time : 7.5ns
- CAS# Latency : 3.0 only
- Burst Length : 1, 2, 4, 8, Full Page
- Burst Type : Sequential/Interleave
- No. of Internal Banks per SDRAM : 4
- Operating Voltage : 3.3V
- Refresh : 8K/64ms
- Device Physicals : 400mil TSOP
- Lead Finish : Gold
- Length x Height : 133.35mm x 29.21mm
- No. of sides : Double-sided
- Mating Connector (Examples)
  Vertical : AMP-390074-6

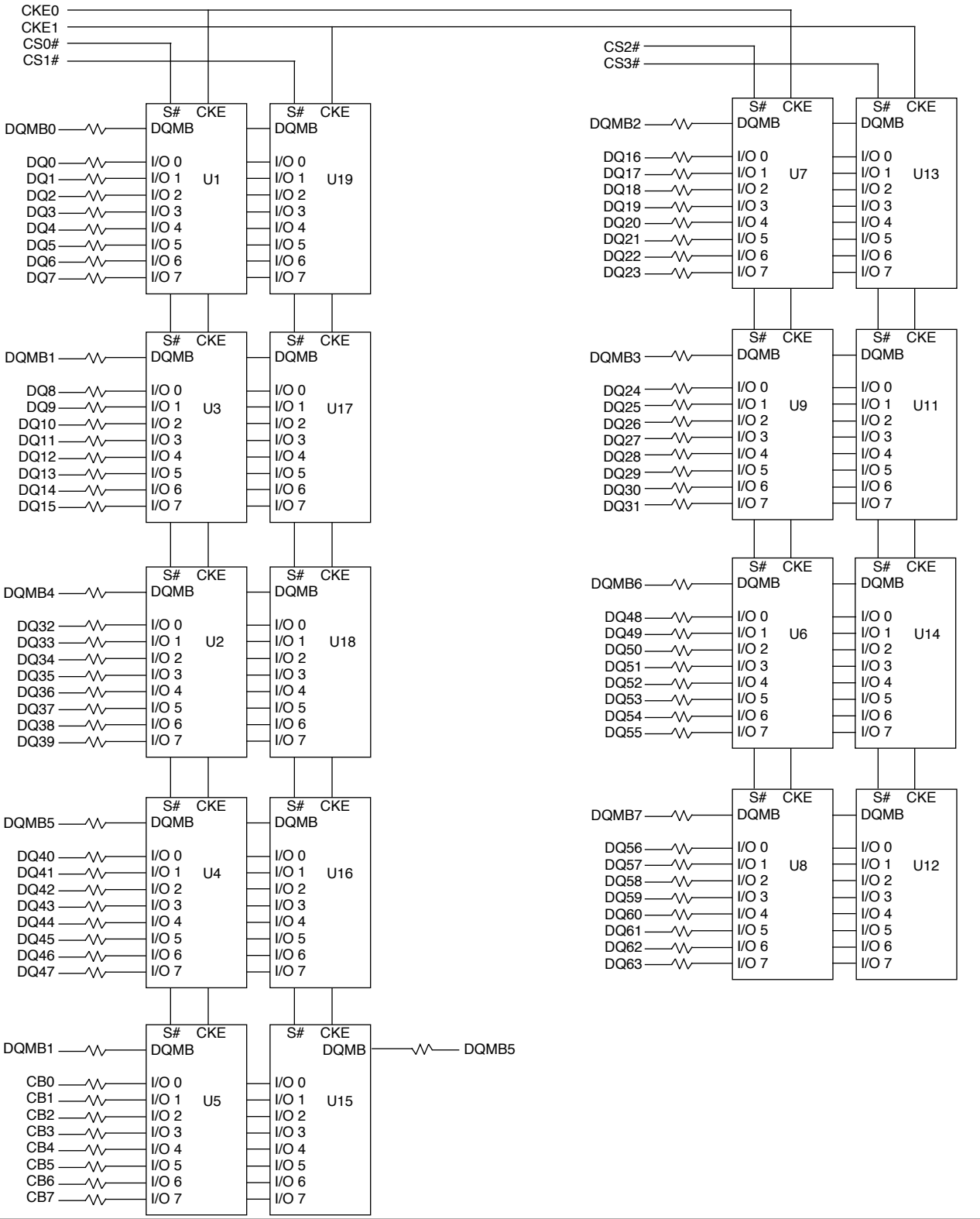
168-pin SDRAM DIMM Pin List

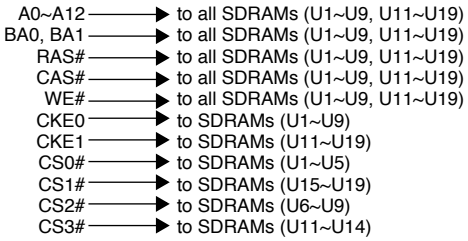
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	22	CB1	43	V_{SS}	64	V_{SS}	85	V_{SS}	106	CB5	127	V_{SS}	148	V_{SS}
2	DQ0	23	V_{SS}	44	NC	65	DQ21	86	DQ32	107	V_{SS}	128	CKE0	149	DQ53
3	DQ1	24	NC	45	CS2#	66	DQ22	87	DQ33	108	NC	129	CS3#	150	DQ54
4	DQ2	25	NC	46	DQMB2	67	DQ23	88	DQ34	109	NC	130	DQMB6	151	DQ55
5	DQ3	26	V_{DD}	47	DQMB3	68	V_{SS}	89	DQ35	110	V_{DD}	131	DQMB7	152	V_{SS}
6	V_{DD}	27	WE#	48	NC	69	DQ24	90	V_{DD}	111	CAS#	132	NC	153	DQ56
7	DQ4	28	DQMB0	49	V_{DD}	70	DQ25	91	DQ36	112	DQMB4	133	V_{DD}	154	DQ57
8	DQ5	29	DQMB1	50	NC	71	DQ26	92	DQ37	113	DQMB5	134	NC	155	DQ58
9	DQ6	30	CS0#	51	NC	72	DQ27	93	DQ38	114	CS1#	135	NC	156	DQ59
10	DQ7	31	NC	52	CB2	73	V_{DD}	94	DQ39	115	RAS#	136	CB6	157	V_{DD}
11	DQ8	32	V_{SS}	53	CB3	74	DQ28	95	DQ40	116	V_{SS}	137	CB7	158	DQ60
12	V_{SS}	33	A0	54	V_{SS}	75	DQ29	96	V_{SS}	117	A1	138	V_{SS}	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	V_{SS}	99	DQ43	120	A7	141	DQ50	162	V_{SS}
16	DQ12	37	A8	58	DQ19	79	CLK2	100	DQ44	121	A9	142	DQ51	163	CLK3
17	DQ13	38	A10/AP*	59	V_{DD}	80	NC	101	DQ45	122	BA0	143	V_{DD}	164	NC
18	V_{DD}	39	BA1	60	DQ20	81	WP	102	V_{DD}	123	A11	144	DQ52	165	SA0
19	DQ14	40	V_{DD}	61	NC	82	SDA	103	DQ46	124	V_{DD}	145	NC	166	SA1
20	DQ15	41	V_{DD}	62	NC	83	SCL	104	DQ47	125	CLK1	146	NC	167	SA2
21	CB0	42	CLK0	63	CKE1	84	V_{DD}	105	CB4	126	A12	147	NC	168	V_{DD}

Pin Description Table

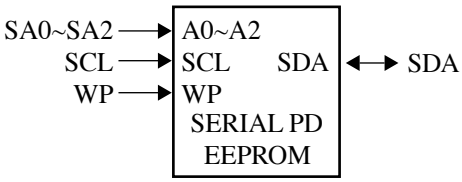
Symbol	Type	Polarity	Function
CLK0~CLK3	Input	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0~CKE1	Input	Active High	Activates the SDRAM CLK signal when high and deactivates the CLK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
CS0#~CS3#	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Active Low	When sampled at the positive rising edge of the clock, CAS#, RAS#, and WE# define the operations to be executed by the SDRAM.
BA0, BA1	Input	-	Selects which of the four internal SDRAM banks is activated.
A0~A9, A10/AP, A11~A12	Input	-	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9, A11 defines the column address (CA0-CA9, CA11) when sampled at the rising clock edge. In addition to the column address, A10/AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, A10/AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0~DQ63 CB0~CB7	Input-Output	-	Data and Check Bit Input/Output pins.
DQMB0~ DQMB7	Input	Active High	Data strobe for input and output data.
SA0~SA2	Input	-	These signals are tied on the system to either V_{SS} or V_{DD} to configure the serial SPD.
SDA	Input-Output	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected on the system board from the SDA bus line to V_{DD} to act as a pullup.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected on the system board from the SCL bus line to V_{DD} to act as a pullup.
WP	Input	-	Write protection.
V_{DD}, V_{SS}	Supply	-	Power and ground for the SDRAM input buffers and core logic.
NC	Supply	-	No Connect

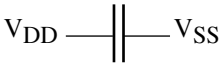
Block Diagram





Clock Wiring	
CLK0	5 SDRAMs
CLK1	5 SDRAMs
CLK2	4 SDRAMs
CLK3	4 SDRAMs





Decoupling capacitors to all devices.

Notes:
1. Data and CLKs are terminated using 10Ω series resistors.
2. CKE1 has a pull-up resistor of 10KΩ to $V_{DD.}$
3. WP signal has a pull-down resistor of 47KΩ.

DC Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on supply pins relative to V_{SS}	V_{DDT}	-1.0 ~ 4.6	V
Power Dissipation	P_T	18	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +150	°C
Short Circuit Output Current	I_{OS}	50	mA

Recommended DC Operating Conditions
(T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

DC Characteristics (cont'd)

Capacitance
(V_{DD} = 3.3V±0.3V, T_A = +25°C)

Parameter	Symbol	Max	Unit
Input Capacitance (Address, RAS#, CAS#, WE#)	C_{I1}	100	pF
Input Capacitance (CS0#, CS1#, CLK0~CLK1)	C_{I2}	35	pF
Input Capacitance (CS2#, CS3#, CLK2~CLK3)	C_{I3}	30	pF
Input Capacitance (DQMB1, DQMB5)	C_{I4}	25	pF
Input Capacitance (DQMB0, DQMB2~DQMB4, DQMB6~DQMB7)	C_{I5}	20	pF
Input Capacitance (CKE0, CKE1)	C_{I6}	55	pF
Input/Output Capacitance (DQ0~DQ63, CB0~CB7)	$C_{I/O}$	24	pF

Notes : Capacitance is sampled per Mil-Std-883.

Leakage Currents
(V_{DD} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Test conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	$0V \le V_{in} \le V_{DD} + 0.3$	-180	180	μA
Output Leakage Current	I_{OZ}	$0V \le V_{out} \le V_{DD}$ D_{out} = Disable	-20	20	μA
Output High Voltage	V_{OH}	High I_{out} = -2mA	2.4	-	mA
Output Low Voltage	V_{OL}	Low I_{out} = 2mA	-	0.4	mA

DC Characteristics (cont'd)

(V_{DD} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to +70°C)

Parameter	Symbol	Test Conditions	Max	Unit	Notes
Operating Current: (One Bank Active)	I_{CC1}	Burst Length = 1, $t_{RC} \geq t_{RC}$(min.), I_{OL} = 0mA	945	mA	1
Precharge Standby Current In Power–Down Mode:	I_{CC2}	CKE ≤ $V_{IL(max.)}$, t_{CK} = 1 CLK	36	mA	
		CKE & CLK ≤ VIL max., t_{CK} = ∞	36	mA	
Precharge Standby Current In Non Power–Down Mode:	I_{CC3}	CKE ≥ $V_{IH(min.)}$, CS# ≥ $V_{IH(min.)}$, t_{CK} = 1 CLK, Input signals are changed one time during 2 CLKs	360	mA	
		CKE ≥ $V_{IH(min.)}$, CLK ≤ $V_{IL\ (max.)}$, t_{CK} = ∞, Input signals are stable	180	mA	
Active Standby Current In Power-Down Mode:	I_{CC4}	CKE ≤ $V_{IL(max.)}$, t_{CK} = 1 CLK	279	mA	
		CKE & CLK ≤ $V_{IL(max.)}$, t_{CK} = ∞	279	mA	
Active Standby Current In Non Power–Down Mode:	I_{CC5}	CKE ≥ $V_{IH(min.)}$, CS# ≥ $V_{IH(min.)}$, t_{CK} = 1 CLK, Input signals are changed one time during 2 CLKs	450	mA	
		CKE ≥ $V_{IH(min.)}$, CLK ≤ $V_{IL\ (max.)}$, t_{CK} = ∞, Input signals are stable	450	mA	
Operating Current: (One Bank Active)	I_{CC6}	I_{OL} = 0mA, Page Burst, t_{CCD} = 2 CLKs	1125	mA	1
Auto Refresh Current:	I_{CC7}	$t_{RC} \geq t_{RC}$ min.	1845	mA	2
Self Refresh Current:	I_{CC8}	CKE ≤ 0.2 V	54	mA	

Notes:
1. Measured with outputs open.
2. Refresh period is 64ms.

AC Characteristics

Parameter	CAS Latency	Symbol	Min	Max	Unit	Notes
Clock Cycle Time	CL = 3	t_{CK}	7.5	-	ns	
	CL = 2		10.0	-	ns	
CLK High Pulse Width		t_{CH}	2.5	-	ns	
CLK Low Pulse Width		t_{CL}	2.5	-	ns	
Access time from CLK	CL = 3	t_{AC}	-	5.4	ns	
	CL = 2		-	6.0	ns	
CKE setup time		t_{CKS}	1.5	-	ns	
CKE hold time		t_{CKH}	0.8	-	ns	
Address setup time		t_{AS}	1.5	-	ns	
Address hold time		t_{AH}	0.8	-	ns	
Command setup time		t_{CSS}	1.5	-	ns	
Command hold time		t_{CSH}	0.8	-	ns	
Data In setup time		t_{DS}	1.5	-	ns	
Data In hold time		t_{DH}	0.8	-	ns	
Data Out to Hi-Z time	CL = 3	t_{HZ}	-	5.4	ns	
	CL = 2		-	6.0	ns	
Data Out to Lo-Z time		t_{LZ}	1.0	-	ns	
Data Out hold time		t_{OH}	2.7	-	ns	
Active to Precharge Period		t_{RAS}	45	100000	ns	
Active to Active Command time		t_{RC}	65	-	ns	
Active to Read/Write time		t_{RCD}	20	-	ns	
Bank to bank active time		t_{RRD}	15	-	ns	
Precharge to Active Period		t_{RP}	20	-	ns	
Refresh Period		t_{REF}	-	64	ms	
Self Refresh Exit to Active time		t_{XSR}	-	75	ns	
Data In to Precharge Period		t_{DPL}	15	-	ns	
CAS# to CAS# delay time		l_{CCD}	1	-	cycle	
CKE to clock disable/enable		l_{CKE}	1	-	cycle	
DQM to input data delay		l_{DID}	0	-	cycle	
DQM to data out disable delay		l_{DOD}	2	-	cycle	
Write command to data delay		l_{DWD}	0	-	cycle	
Data in to Active Command		l_{DAL}	5	-	cycle	
MRS command to Active delay		l_{MRD}	2	-	cycle	

Notes:

1. AC measurement assumes t_T =1 ns. Reference level for timing of input signals is 1.4V.
2. Load condition is CL = 50 pF.
3. Maximum value is a reference value and a device may work at a slower untested clock rate.
4. t_{OH}, t_{LZ}, and t_{HZ} define the times at which the output level achieves ±200mV.
5. All the latency timings are measured in terms of clock period t_{CLK}.

Table 1: Command Truth Table

Function	CKE		CS#	RAS#	CAS#	WE#	DQM	BA	A10 (AP)	ADDR	Notes
	Previous	Current									
Mode Register Set	H	X	L	L	L	L	X	OP Code			
Auto (CBR) Refresh	H	H	L	L	L	H	X	X	X	X	
Entry Self Refresh	H	L	L	L	L	H	X	X	X	X	
Exit Self Refresh	L	H	H	X	X	X	X	X	X	X	
			L	H	H	H					
Single Bank Precharge	H	X	L	L	H	L	X	BA	L	X	2
Precharge all Banks	H	X	L	L	H	L	X	X	H	X	
Bank Activate	H	X	L	L	H	H	X	BA	Row Address		2
Write	H	X	L	H	L	L	X	BA	L	Column	2
Write with Auto-Precharge	H	X	L	H	L	L	X	BA	H	Column	2
Read	H	X	L	H	L	H	X	BA	L	Column	2
Read with Auto-Precarge	H	X	L	H	L	H	X	BA	H	Column	2
Burst Termination	H	X	L	H	H	L	X	X	X	X	3, 8
No Operation	H	X	L	H	H	H	X	X	X	X	
Device Deselect	H	X	H	X	X	X	X	X	X	X	
Clock Suspend Mode Entry	H	L	X	X	X	X	X	X	X	X	4
Clock Suspend Mode Exit	L	H	H	X	X	X	X	X	X	X	4
Data Write/Output Enable	H	X	X	X	X	X	L	X	X	X	5
Data Mask/Output Disable	H	X	X	X	X	X	H	X	X	X	5
Power Down Mode Entry	H	L	H	X	X	X	X	X	X	X	6, 7
			L	H	H	X					
Power Down Mode Exit	L	H	H	X	X	X	X	X	X	X	6, 7
			L	H	H	X					

Notes:

1. All of the SDRAM operations are defined by states of CS#, WE#, RAS#, CAS#, and DQM at the positive rising edge of the clock.
2. Bank Select (BA0, BA1): BA0, BA1 = 0,0 selects banks 0; BA0, BA1 = 0,1 selects bank 1; BA0, BA1 = 1,0 selects bank 2; BA0, BA1 = 1,1 selects bank 3.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS# latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. (If this command is issued during a burst operation, the device state will be clock suspend mode.) The Power Down Mode does not perform any refresh operations, therefore the device can't remain in this mode longer than the Refresh period (t_{REF}) of the device. One clock delay is required for mode entry and exit.
7. If CS# is low, then when CKE returns high, no command is registered into the chip for one clock cycle. A No Operation (NOP) or Device Deselect command is required on the next edge following CKE going high.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

Table 2: Mode Register Table

Address	BA0,1	An~A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	Operation Mode			CAS Latency			BT	Burst Length		

Operation Mode				CAS Latency				Burst Type		Burst Length				
A9	A8	A7	Mode	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	0	Prog. Burst length	0	0	0	Rsvd.	0	Sequential	0	0	0	1	1
1	0	0	Burst Read / Single Write	0	0	1	Rsvd.	1	Interleave	0	0	1	2	2
				0	1	0	2			0	1	0	4	4
				0	1	1	3			0	1	1	8	8
				1	0	0	Rsvd.			1	0	0	Rsvd.	Rsvd.
				1	0	1	Rsvd.			1	0	1	Rsvd.	Rsvd.
				1	1	0	Rsvd.			1	1	0	Rsvd.	Rsvd.
				1	1	1	Rsvd.			1	1	1	Full Page	Rsvd.

Note: 1. RFU (Reserved for future use) should stay "0" during MRS cycle.

Serial Presence Detect

Byte No.	Byte Description	Value Supported	Value in Hex
0	# of bytes written into serial memory at module manufacturer	128 Bytes	80h
1	Total # of bytes of SPD memory device	256 Bytes	08h
2	Fundamental memory type	SDRAM	04h
3	# of row address on this assembly	13	0Dh
4	# of column address on this assembly	11	0Bh
5	# of module rows on this assembly	2	02h
6	Data width of this assembly	72	48h
7	.....Data width of this assembly	-	00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM cycle time from clock @ CAS latency of 3.0	7.5ns	75h
10	SDRAM access time from clock @ CAS latency of 3.0	5.4ns	54h
11	DIMM configuration type	ECC	02h
12	Refresh rate & type	SR, 7.8	82h
13	Primary SDRAM width	8	08h
14	Error checking SDRAM width	8	08h
15	Minimum clock delay for back-to-back random column address	1	01h
16	SDRAM device attributes : Burst lengths supported	1, 2, 4, 8, Full	8Fh
17	SDRAM device attributes : # of banks on SDRAM device	4	04h
18	SDRAM device attributes : CAS latency	2.0, 3.0	06h
19	SDRAM device attributes : CS latency	CS# Latency = 0	01h
20	SDRAM device attributes : Write latency	WE# Latency = 0	01h
21	SDRAM module attributes	Non-Registered/Unbuffered DQM, address & control, No PLL	00h

Byte No.	Byte Description	Value Supported	Value in Hex
22	SDRAM device attributes : General	+/- 10% voltage tolerance, Burst Read Single bit Write precharge all, auto precharge	0Eh
23	SDRAM cycle time @ CAS latency of 2.0	10.0ns	A0h
24	SDRAM access time @ CAS latency of 2.0	6.0ns	60h
25	SDRAM cycle time @ CAS latency of 1.0	-	00h
26	SDRAM access time @ CAS latency of 1.0	-	00h
27	Minimum row precharge time (=tRP)	20ns	14h
28	Minimum row active to row active delay (=tRRD)	15ns	0Fh
29	Minimum RAS to CAS delay (=tRCD)	20ns	14h
30	Minimum activate precharge time (=tRAS)	45ns	2Dh
31	Module row density	512MB	80h
32	Command and Address signal input setup time	1.5ns	15h
33	Command and Address signal input hold time	0.8ns	08h
34	Data signal input setup time	1.5ns	15h
35	Data signal input hold time	0.8ns	08h
36~61	Superset information (may be used in future)	Not used	00h
62	SPD data revision code	1.2	12h
63	Checksum for bytes 0 ~ 62		26h
64	Manufacturer JEDEC ID code	Continuation Code	7Fh
65	.....Manufacturer JEDEC ID code	SMART's ID	94h
66~71	.....Manufacturer JEDEC ID code	Not Used	FFh
72	Manufacturing location	See Note 1	xxh
73~90	Manufacturer part#	SM572288578D03R01	P. No
91	Manufacturer revision code	Rev 0	00h
92	.....Manufacturer revision code	None	FFh

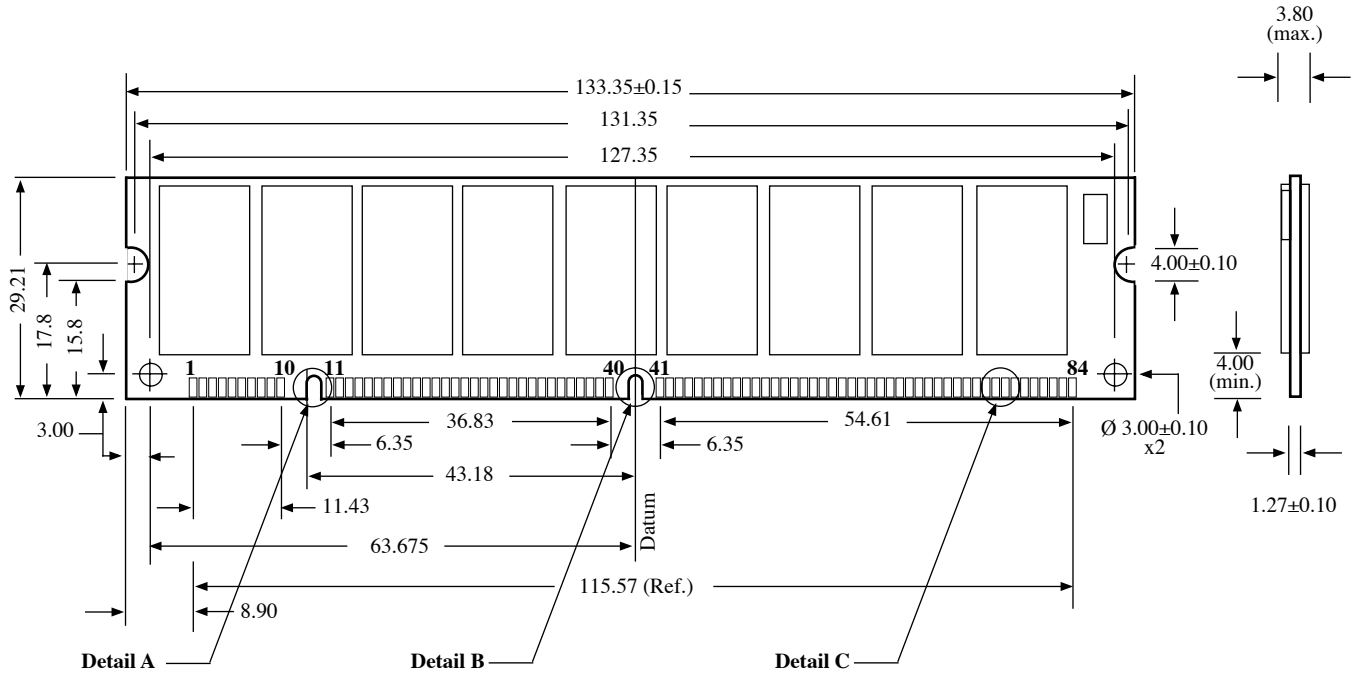
Byte No.	Byte Description	Value Supported	Value in Hex
93	Manufacturing data (Year)	Date	Date
94	Manufacturing data (Week)	Date	Date
95~98	Assembly serial#	Serial Number	S. No
99~125	Manufacturer specific data	SMART Modular Technologies	
126	System frequency for 100MHz	100MHz	64h
127	Intel Specification details	2, 3	F7h
128~255	Unused storage locations		FFh

Note:

1. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia

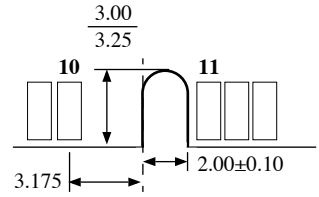
Physical Dimensions

168-pin DIMM Module

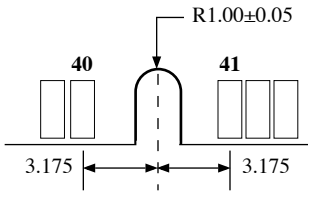


Note : Pin 85 is behind pin 1 on the back side.

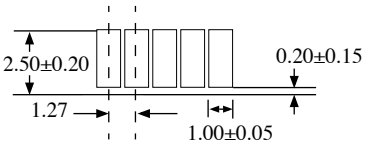
Front View



Detail A : Position of Technology Notch



Detail B : Position of Voltage Notch



Detail C : Edge Connector

(All dimensions are in millimeters with ±0.13mm tolerance unless specified otherwise.)

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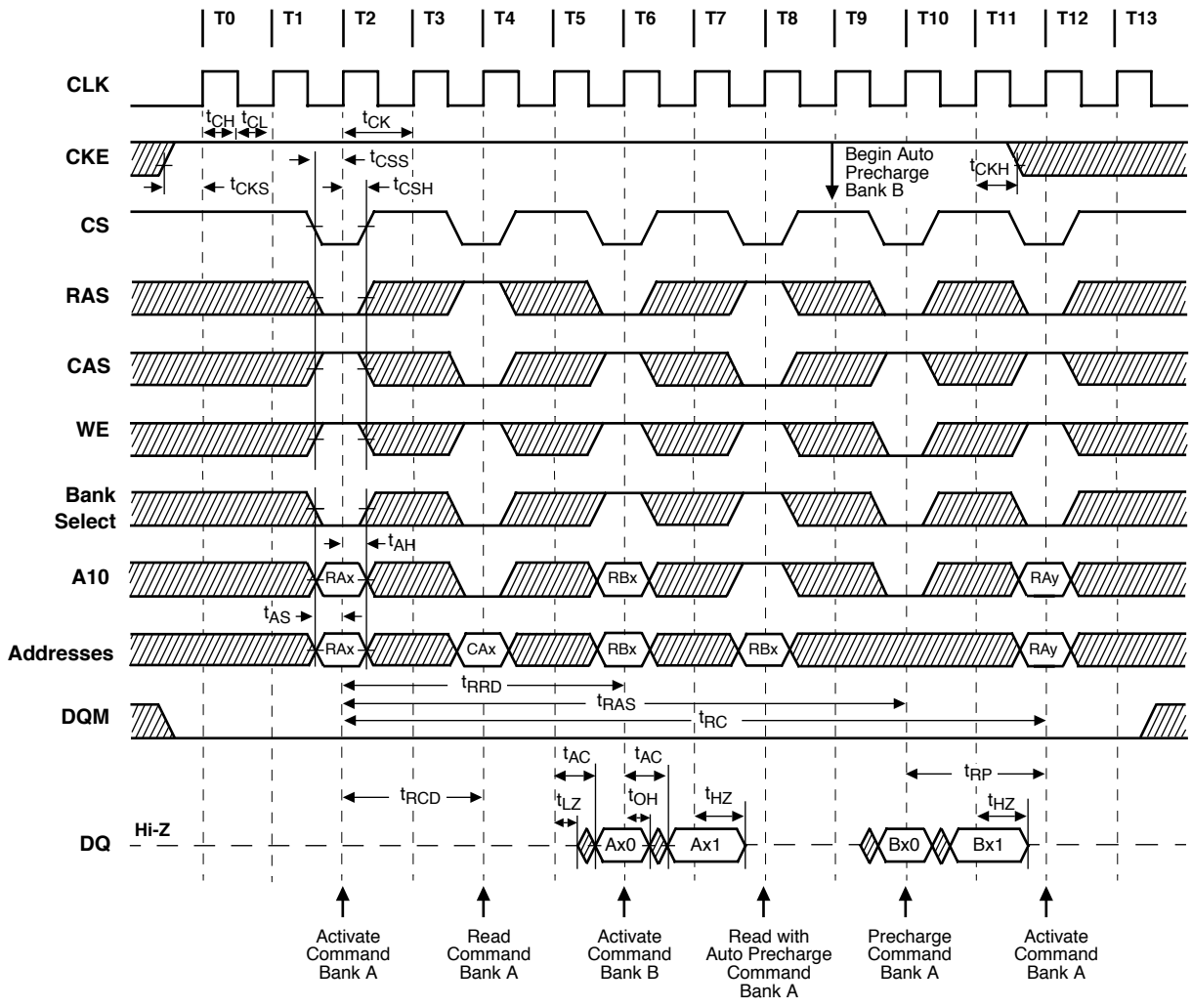
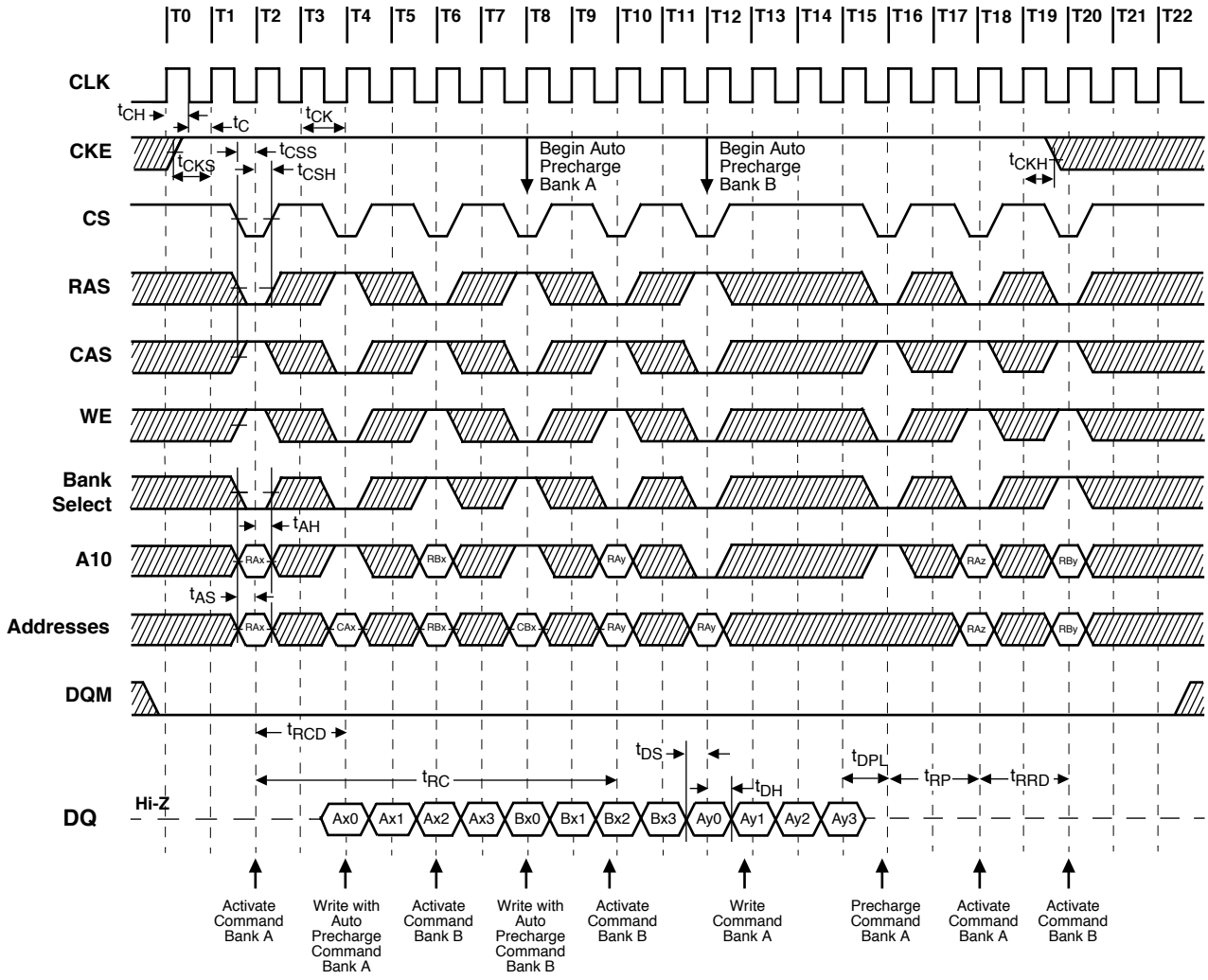
Timing Waveforms

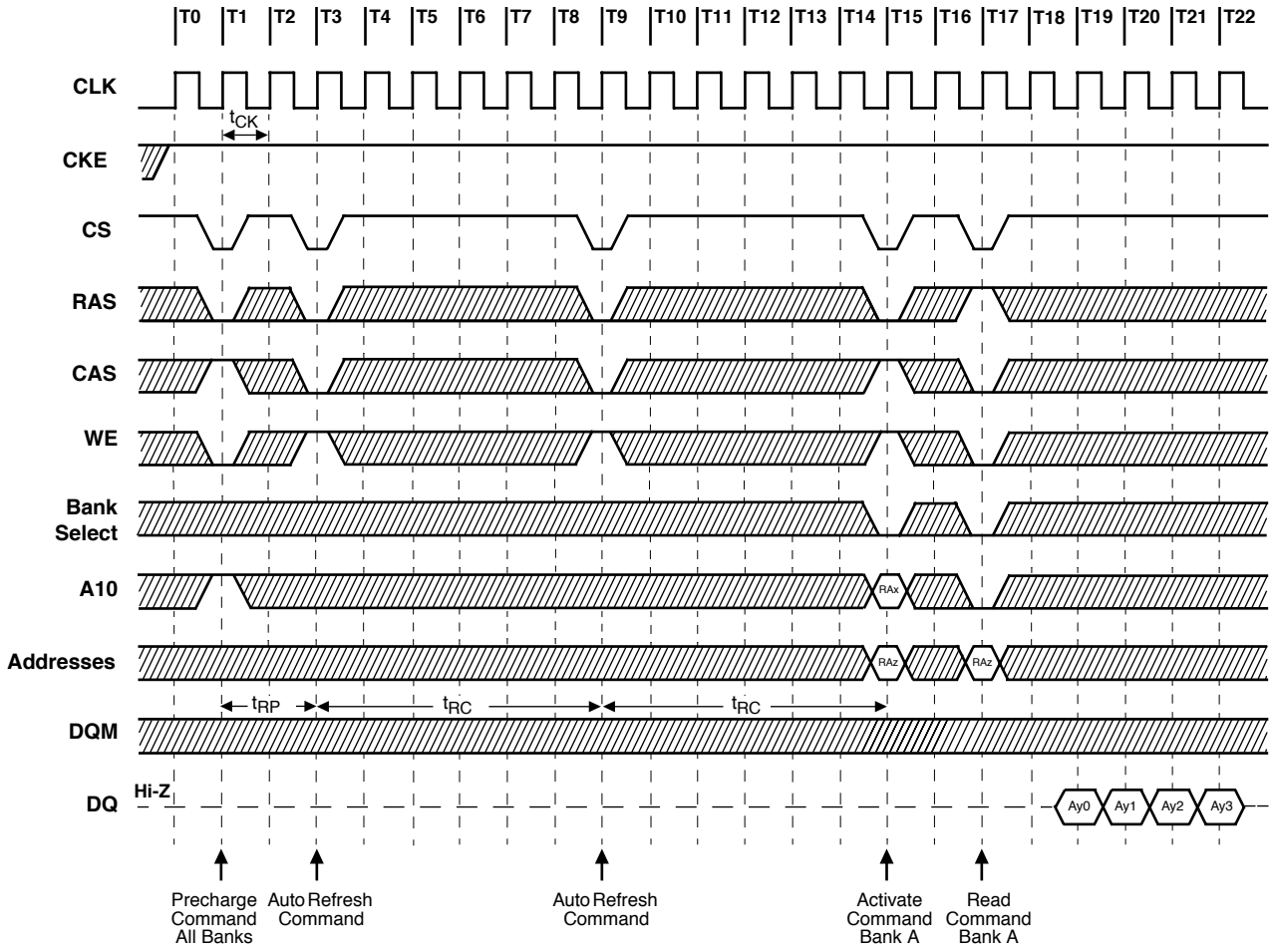
Read Cycle



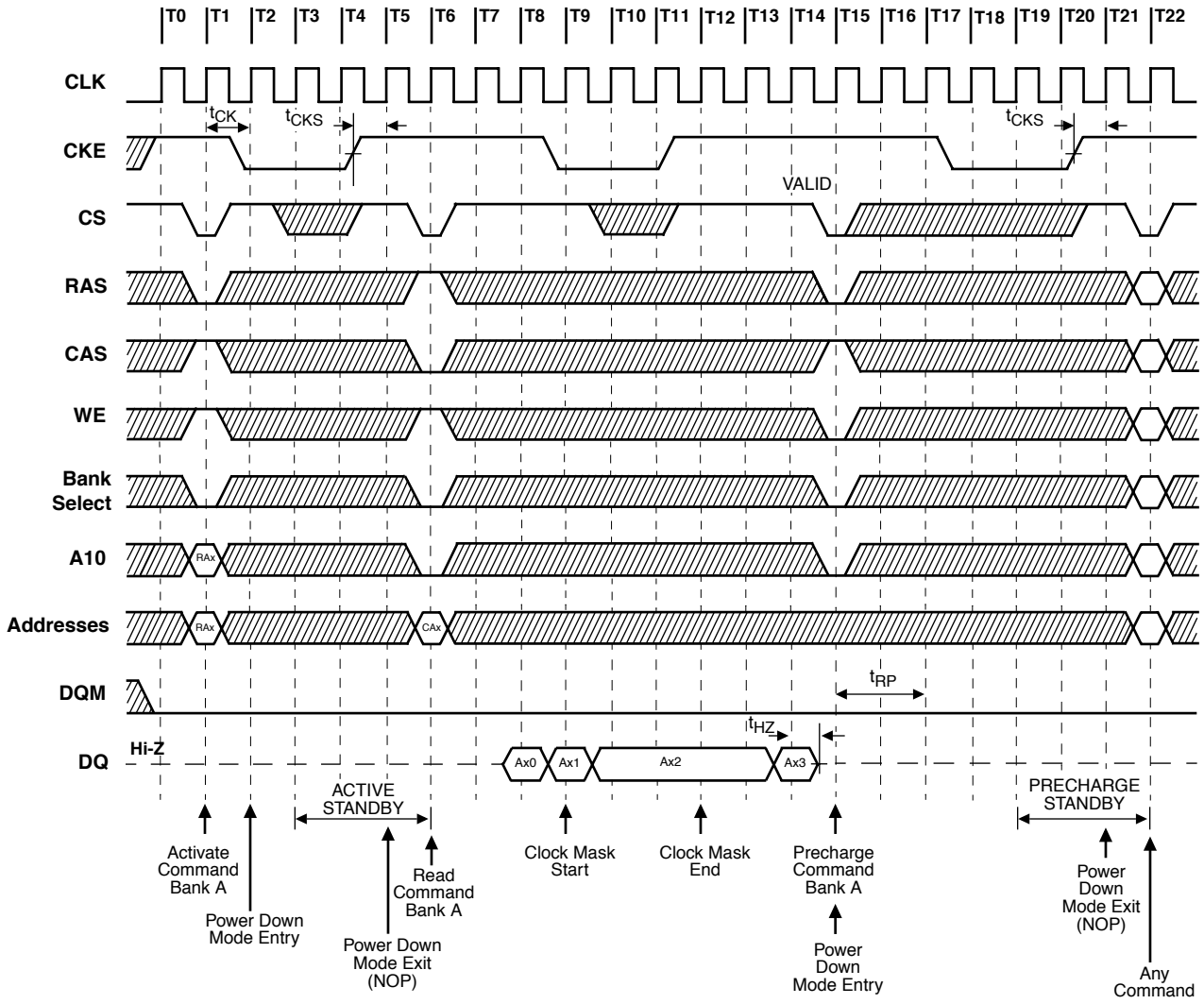
Write Cycle


T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22
CLK
CKE
CS
RAS
CAS
WE
Bank Select
A10
Addresses
DQM
DQ
Hi-Z
tCH
tC
tCK
tCKS
tCSS
tCSH
tCKH
tAH
tAS
tRCD
tRC
tDS
tDH
tDPL
tRP
tRRD
Begin Auto Precharge Bank A
Begin Auto Precharge Bank B
RAx
RBx
RAy
RAz
RBy
CAx
CBx
Ax0 Ax1 Ax2 Ax3 Bx0 Bx1 Bx2 Bx3 Ay0 Ay1 Ay2 Ay3
Activate Command Bank A
Write with Auto Precharge Command Bank A
Activate Command Bank B
Write with Auto Precharge Command Bank B
Activate Command Bank B
Write Command Bank A
Precharge Command Bank A
Activate Command Bank A
Activate Command Bank B

Auto Refresh (CBR) Cycle



Power Down Mode and Clock Mask



Part Number Decode

SM	5	72	28	8	5	7	8	D	0	3	R	01
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	

① **SMART**
Modular Technologies

② **Product Category**
5 : SDRAM SIMM/DIMM

③ **Module Data Bus Width**
72 : x72

④ **Module Address Depth**
28 : 128M

⑤ **Device Data Width**
8 : x8

⑥ **Special Device Feature**
5 : Standard (4 Bank SDRAM)

⑦ **Voltage/Mode**
7 : 3.3V, Synchronous DRAM

⑧ **Refresh / Power**
8 : 8K Ref./Standard Power

⑨ **Module Configuration**
D : 168 pin Unbuffered, ECC

⑩ **Device Physicals**
0 : 128Mbit Device Based (400mil TSOP)

⑪ **CAS Latency**
3 : CL = 3.0 only

⑫ **Cycle Time (Clock Speed)**
R : 7.5ns (PC133/133 MHz)
tRP = 3, tRCD = 3

Note : “U” in the part number should be replaced by user specified option.

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