PCMCIA 2.1 Compliant MLC Series FLASH Memory Cards
8 to 64 Megabyte 5 Volt Only Card Capacities
Using 3Volt Intel Strata™ Flash Technology

Description

Smart Modular MLC (Multi-Level Cell) Flash products are high quality PCMCIA 2.1 compliant Type I memory cards, which operate in a 5 Volt only environment. Smart Modular MLC Flash cards feature an array of 1 to 4 Intel®64 Megabit (28F640J3) or Intel®128 Megabit (28F128J3) FLASH components, which are packaged in a quality PCMCIA housing by our ISO 9001, certified production team. FLASH technology assures data retention without the need for battery back-up of any kind, even when system power is removed.

MLC Series cards offer memory capacities ranging from 8 to 64 Megabytes with a 128 Kbyte block erase resolution. Memory blocks that are not busy with program/erase operations, may be accessed by both read and write commands without concern for on going operations in other blocks. Additionally data may be handled in either 8 bit or 16 bit bus modes. The hardware RESET and Ready/Busy signals offer Host systems added control over card operations.

These features make Smart Modular memory cards especially desirable for a wide variety of custom applications that utilize PCMCIA slots such as Automotive Diagnostics, Consumer Electronics, Communications and Portable

Features

- PC Card 97 compliant (PCMCIA 2.1)
- FLASH Architecture, non volatile memory
- Single Supply Voltage Operation (4.5V-5.5V)
- Standard 200 nsec Access Time from Standby
- Common Flash Interface (CFI) compliant
- Byte-wide and Word-wide access
- Embedded Program/Erase Algorithms
- Erase Suspend/Resume Feature
- 128 Kilobyte Block Erase Resolution
- 32 byte Write Buffer – 6µsec per byte effective Programming time
- High Write Endurance - 100,000 Write/Erase Cycles Minimum
- Dedicated Attribute Memory EEPROM
- Extremely Low Power Consumption
  - 120 µA Max. Standby Current (CMOS)
  - 75 mA Max. Byte Write Current
  - 50 mA Max. Block Erase Current
- ISO 9001 Quality Controls

PIN DESCRIPTION

Signal	Name	Function
A[25:0]	Address Bus	Address Inputs, A25-A0
D[15:0]	Data Bus	Data Input/Outputs
/OE	Output Enable	Active Low for Read
/WE	Write Enable	Active Low for Write
/CE1	Card Enable Low Byte	Active Low for Read/ Write Even Byte
/CE2	Card Enable High Byte	Active Low for Read/ Write Odd Byte
/REG	Register Select	Active Low to enables Attribute Memory
RESET	Card Reset	Active High to Reset the Card
/BUSY	Ready / Busy	Active Low during Erase/Write operations
WP	Write Protect	Output Signal indicates the WP switch state
/VS1, /VS2	Voltage Sense 1, 2	Voltage Sense Outputs (VS1 open, VS2 open for 5V)
/CD1, /CD2	Card Detect Signals 1, 2	Tied to GND
V_{CC}	Power Supply	Power Supply Voltage, 4.5V – 5.5V
GND (V_{SS})	Ground	Card Ground

Corporate Headquarters: P. O. Box 1757, Fremont, CA 94538, USA • Tel:(510) 623-1231 • Fax:(510) 623-1434 • E-mail: info@smartm.com
Flash Design Center: 7 Lopez Road, Wilmington , MA 01887 USA • Tel:(978) 988-8848 • Fax:(978) 988-7651 • Customers@Smartm.com
Europe: 5 Kelvin Park South, Kelvin South, East Kilbride, G75 ORH, United Kingdom• Tel: +44-870-870-8747 • Fax: +44-870-870-8757
Asia: Plot 18, Lrg Jelawat 4, Kawasan Perindustrian Seberang Jaya 13700, Prai, Penang, Malaysia • Tel: +604-3992909 • Fax: +604-3992903

PIN ASSIGNMENTS

Pin #	Signal	I/O	Function		Pin #	Signal	I/O	Function	
1	GND		Ground		35	GND		Ground	
2	D3	I/O	Data Bit 3		36	/CD1	O	Card Detect - Grounded	
3	D4	I/O	Data Bit 4		37	D11	I/O	Data Bit 11	
4	D5	I/O	Data Bit 5		38	D12	I/O	Data Bit 12	
5	D6	I/O	Data Bit 6		39	D13	I/O	Data Bit 13	
6	D7	I/O	Data Bit 7		40	D14	I/O	Data Bit 14	
7	/CE1	I	Card Enable Low byte	PH	41	D15	I/O	Data Bit 15	
8	A10	I	Address Bit 10		42	/CE2	I	Card Enable High byte	PH
9	/OE	I	Output Enable	PH	43	/VS1		Vltg Sense Signal 1- Open	
10	A11	I	Address Bit 11		44	*RFU*		*Reserved For Future Use*	NC
11	A9	I	Address Bit 9		45	*RFU*		*Reserved For Future Use*	NC
12	A8	I	Address Bit 8		46	A17	I	Address Bit 17	
13	A13	I	Address Bit 13		47	A18	I	Address Bit 18	
14	A14	I	Address Bit 14		48	A19	I	Address Bit 19	
15	/WE	I	Write Enable	PH	49	A20	I	Address Bit 20	
16	/BUSY	O	Ready Busy Signal	PH	50	A21	I	Address Bit 21	
17	V_{CC}		Power Supply		51	V_{CC}		Power Supply	
18	*Vpp1*		*Program Voltage 1*	NC	52	*Vpp2*		*Program Voltage 2*	NC
19	A16	I	Address Bit 16		53	A22	I	Address Bit 22	
20	A15	I	Address Bit 15		54	A23	I	Address Bit 23 **(Note 1)**	
21	A12	I	Address Bit 12		55	A24	I	Address Bit 24 **(Note 2)**	
22	A7	I	Address Bit 7		56	A25	I	Address Bit 25 **(Note 3)**	
23	A6	I	Address Bit 6		57	/VS2		Vltg Sense Signal 2- Open	
24	A5	I	Address Bit 5		58	RESET	I	Hardware RESET	PH
25	A4	I	Address Bit 4		59	WAIT	O	Wait State Control	PH
26	A3	I	Address Bit 3		60	*RFU*		*Reserved For Future Use*	NC
27	A2	I	Address Bit 2		61	/REG	I	Register Select	PH
28	A1	I	Address Bit 1		62	/BVD2	O	Batt. Voltage Detect 2	PH
29	A0	I	Address Bit 0		63	/BVD1	O	Batt. Voltage Detect 1	PH
30	D0	I/O	Data Bit 0		64	D8	I/O	Data Bit 8	
31	D1	I/O	Data Bit 1		65	D9	I/O	Data Bit 9	
32	D2	I/O	Data Bit 2		66	D10	I/O	Data Bit 10	
33	WP	O	Write Protect		67	/CD2	O	Card Detect - Grounded	
34	GND		Ground		68	GND		Ground	

Notes :

1. *A23 is NC for cards of 8 Megabytes capacity.*
2. *A24 is NC for cards of 16 Megabytes capacity or lower.*
3. *A25 is NC for cards of 32 Megabytes capacity or lower.*

Legend :

I = *Input to card only*
O = *Output from card only*
I/O = *Bi-directional signal*
PH = Pulled High (10 - 50K Typ.)
PL = Pulled Low (100K Min.)
NC = Not Connected

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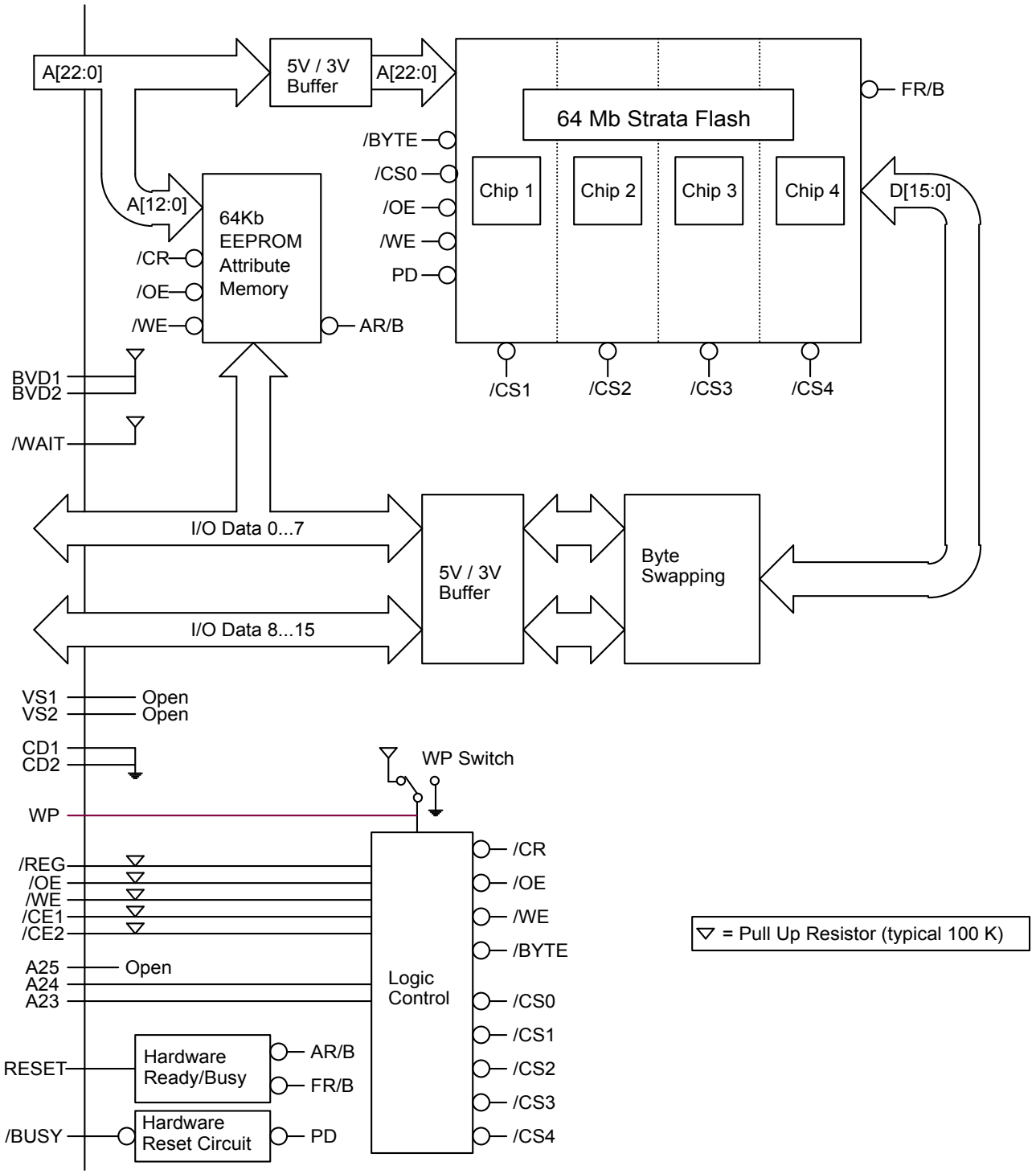
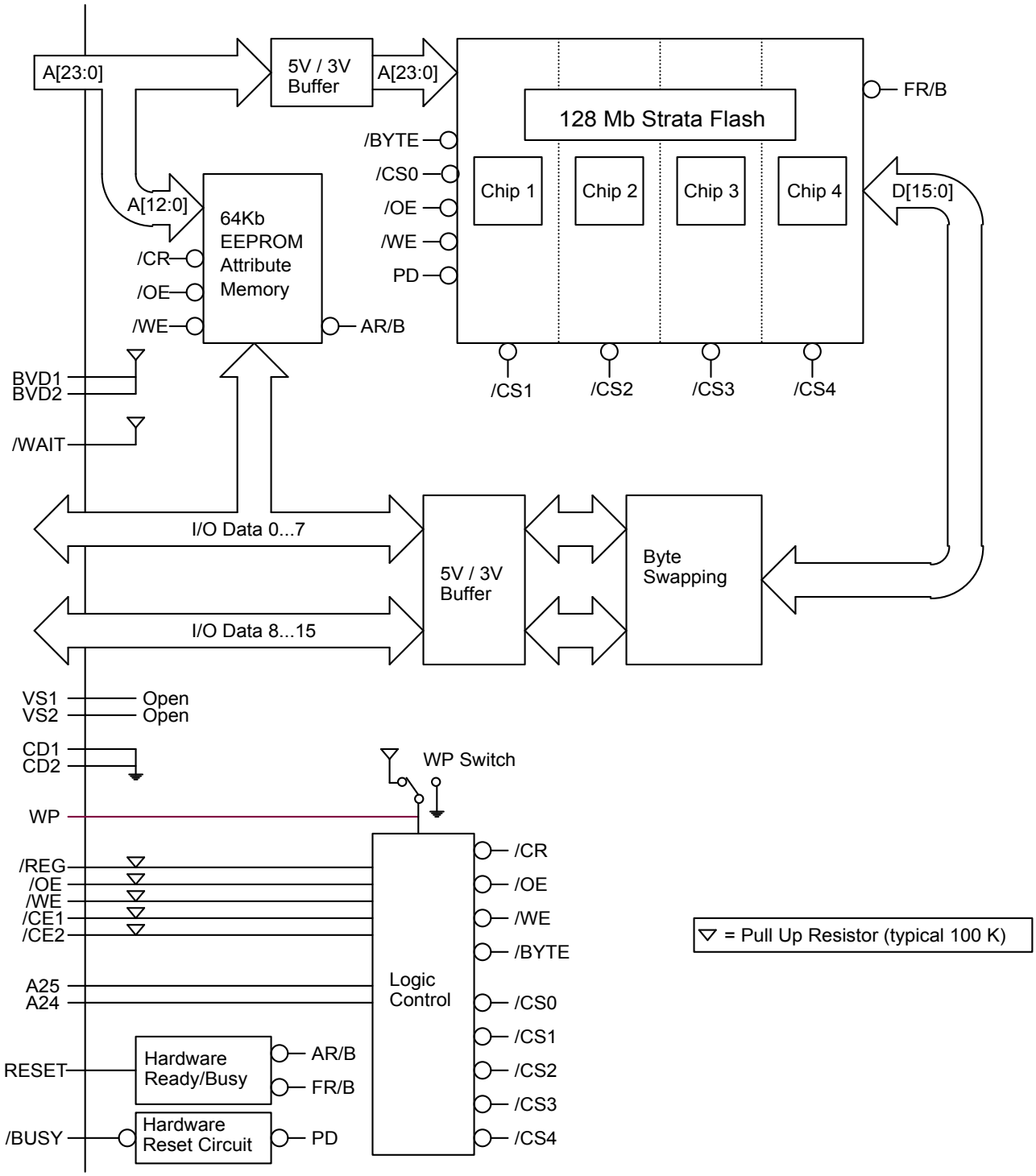
Asia: Plot 18, Lrg Jelawat 4, Kawasan Perindustrian Seberang Jaya 13700, Prai, Penang, Malaysia • Tel: +604-3992909 • Fax: +604-3992903

FUNCTIONAL BLOCK DIAGRAM – CARDS BASED ON **28F640J3**



FUNCTIONAL BLOCK DIAGRAM – CARDS BASED ON **28F128J3**



COMMON MEMORY BUS OPERATIONS

Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ								
Read Even (x8)	H	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 1)**	H	H	L	L	H	H	High -Z	**Data Out-Odd**
Read Odd (x8)	H	L	H	L	H	X	**Data Out-Odd**	High-Z
Read Word (x16)	H	L	L	L	H	X	**Data Out-Odd**	**Data Out-Even**
WRITE/ERASE								
Write Even (x8)	H	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 1)**	H	H	L	H	L	H	High -Z	**Data In-Odd**
Write Odd (x8)	H	L	H	H	L	X	**Data In-Odd**	High-Z
Write Word (x16)	H	L	L	H	L	X	**Data In-Odd**	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Notes:

2. *Byte access - Odd. In this x8 mode, A0 = V_{IH} outputs or inputs the "odd" byte (high order byte of the x16 word on D7 – D0). This is accomplished internal to the card by transposing D15-D8 to D7-D0.*

Legend:

$H = V_{IH}$
$L = V_{IL}$
X = Don't Care

ATTRIBUTE MEMORY BUS OPERATIONS

Pins/Operation	/REG	/CE2	/CE1	/OE	/WE	A0	D8-D15	D0-D7
READ (Note 1)								
Read Even (x8)	L	H	L	L	H	L	High -Z	**Data Out-Even**
Read Odd (x8) **(Note 2)**	L	H	L	L	H	H	High -Z	Data Out-Odd Not Valid
Read Odd (x8) **(Note 2)**	L	L	H	L	H	X	Data Out-Odd Not Valid	High-Z
Read Word (x16) **(Note 2)**	L	L	L	L	H	X	Data Out-Odd Not Valid	**Data Out-Even**
WRITE (Note 1)								
Write Even (x8)	L	H	L	H	L	L	High -Z	**Data In-Even**
Write Odd (x8) **(Note 3)**	L	H	L	H	L	H	High -Z	Data In-Odd Not Valid
Write Odd (x8) **(Note 3)**	L	L	H	H	L	X	Data In-Odd Not Valid	High-Z
Write Word(x16) **(Note 3)**	L	L	L	H	L	X	Data In-Odd Not Valid	**Data In-Even**
INACTIVE								
Card Output Disable	X	X	X	H	X	X	High-Z	High-Z
Standby	X	H	H	X	X	X	High-Z	High-Z

Note:

1. *Refer to the data sheets for the Microchip 28C16A EEPROM for details on programming the attribute memory.*
2. *Data Read operations will produce data information that has no valid meaning for the Odd byte of information.*
3. *Data Write operations may be initiated, however data information for the Odd byte will not be stored.*

Legend:

H = V_{IH}
L = V_{IL}
X = Don't Care

PIN DESCRIPTIONS

Vcc
Card Power Supply

Power input required for device operation. The Vcc must be 4.5V to 5.5V

GND
Card Ground

The V_{ss} pins of all IC components and related circuitry are connected to this card ground, which must be connected to the system ground provided by the Host.

NC
Not Connected

These pins are physically not connected to any circuitry.

A0-A25
Address Bus

These signals are address input lines that are used for accesses to card memory. A0 selects odd or even byte addresses when read or write operations are issued as a byte wide command, in word mode A0 is a "don't care". For Cards based on 28F640J3 components, A23 through A24 (A25 is NC) select which Flash Memory Device will be accessed. A1 through A22 are used to select the specific address that is to be accessed on an individual memory component.
For Cards based on 28F128J3 components, A24 through A25 select which Flash Memory Device will be accessed. A1 through A23 are used to select the specific address that is to be accessed on an individual memory component.

D0-D15
Data (Input/Output) Bus

Data lines D0 through D15 are used to transfer data to and from the card. When memory is not selected or outputs are disabled data lines are placed in a high impedance state.

/OE
Output Enable Signal

This active low input signal enables memory devices to activate data lines and output data information.

/WE
Write Enable Signal

This active low input signal controls memory write functions and is used to strobe data into the card memory.

WP
Write Protect Signal

This output signal indicates whether or not card write operations have been disabled by the Write Protect Switch (WPS). When the signal is asserted high, card write operations are disabled. When this signal is asserted low, write operations to the card are allowed.

/CE1, /CE2
Card Enable

/CE1 and /CE2 are active low inputs driven by the host to enable even byte, odd byte, or word data transfers. In conjunction with A0, asserting either /CE1 or /CE2 accesses even and odd numbered bytes, respectively. Word transfers are accomplished via the assertion of both /CE1 and /CE2, in this case A0 is a "don't care". The card is deselected and power consumption is reduced to stand-by levels when both /CE1 and /CE2 are driven high by the host.

NOTE: Interchanged byte and word data transfers require a mandatory 1 msec wait state before data becomes valid.

PIN DESCRIPTIONS *(CONTINUED)*

/REG
Register Select Signal

This active low input signal enables access to the Attribute memory EEPROM. Attribute memory is typically used to store the CIS file, which contains specific card information. Access to common memory is not possible when /REG is asserted low.

RESET
RESET Signal

This is an active high input signal that is used by the Host to place the card in the deep power down mode of operation. After the RESET signal is returned to the inactive low state, the card memory will be initialized in read mode.

/WAIT
Extended Bus Cycle

This active low output signal is used by the card to delay completion of a memory access operation. There are no wait states generated by these memory cards. For this reason the /WAIT signal is pulled high by a resistor.

/BUSY
Ready Busy Signal

This active low output signal indicates that at least one memory device in the card is busy performing a task.

/CD1, /CD2
Card Detect

These pins are tied directly to ground and are used by the Host system to detect the presence of the card. If /CD1 and /CD2 are not both detected low by the Host, then the card is not properly inserted.

/VS1, /VS2
Voltage Sense Signals

The Voltage Sense Signals notify the socket of the card's Vcc requirements on initial power up. When /VS1 and /VS2 are open, as is the case on these cards, the card is identified to the Host system as a 5V only card.

/Vpp1, /Vpp2
Program and Peripheral Voltages

These signals are normally used to supply additional programming voltages for memory devices that require programming voltages other than the Vcc supply. These memory cards require only Vcc voltages, therefore Vpp1 and Vpp2 are Not Connected.

/BVD1, /BVD2
Battery Voltage Detect

These pins are normally used to indicate the status of an internal card battery. Since FLASH cards do not require or use a battery, these signals are internally pulled high by a resistor.

MANUFACTURER'S IDENTIFICATION CODE TABLE

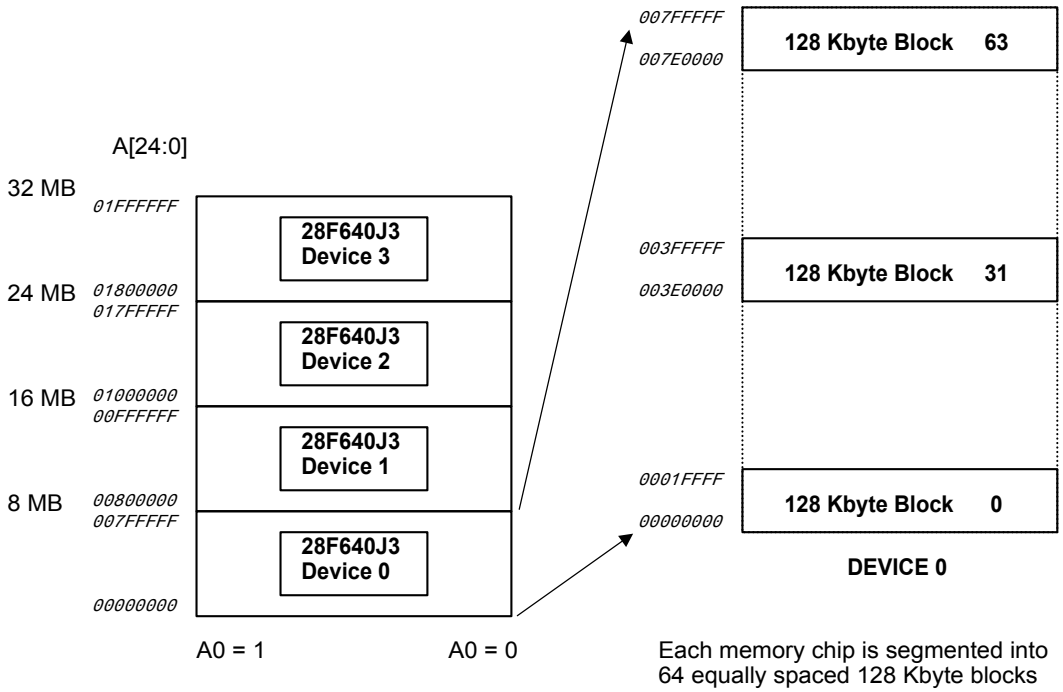
Device	Manufacturer	Hex Data	
		Manufacturer Code	Device Code
28F640J3	Intel	89h	17h
28F128J3A	Intel	89h	18h

The component manufacturer and device ID codes of each common memory component may be read form the Card Information Structure (CIS), or directly from each memory device. The CIS file is located in the Attribute Section of the card memory. Typically the CIS is stored in the EEPROM.

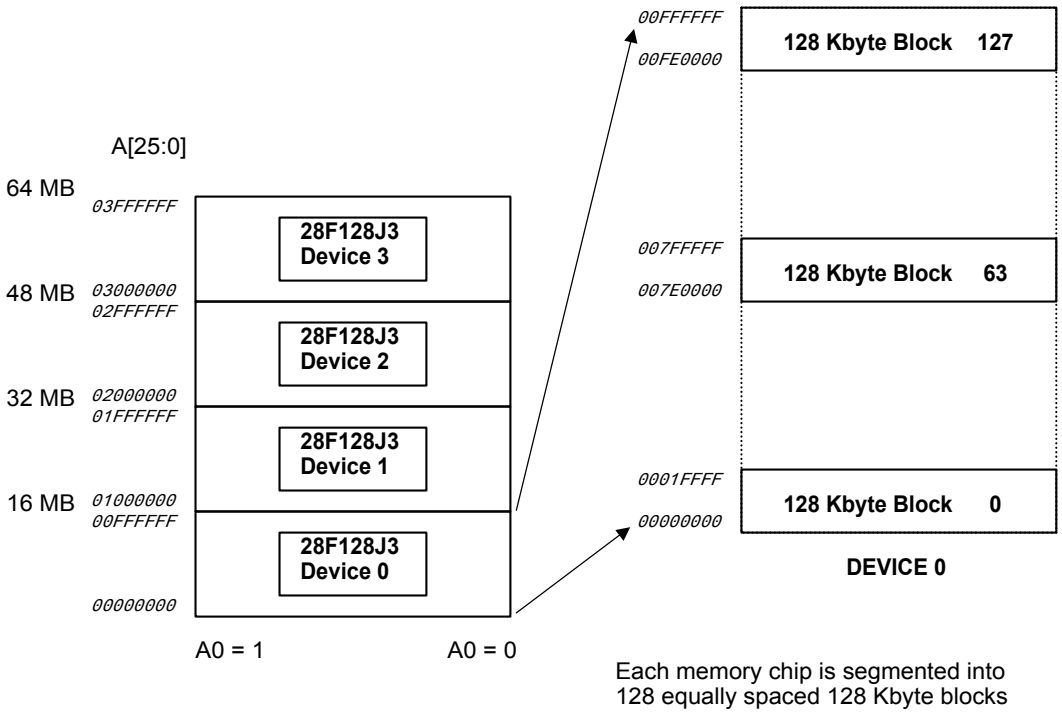
Directly reading the IDs from a memory component may be done by initiating the embedded Read Identifier Codes Command (See Command Definitions Table for command sequence and codes). Once the appropriate command sequence codes have been written to a device, a read operation at chip address 00000h will return the Manufacture ID code and a read at 00001h will return the device ID code for the specific component use on the Card. This mode may be exited by initiating another valid command operation.

For complete details of these memory devices refer to the manufacturers published data sheets.

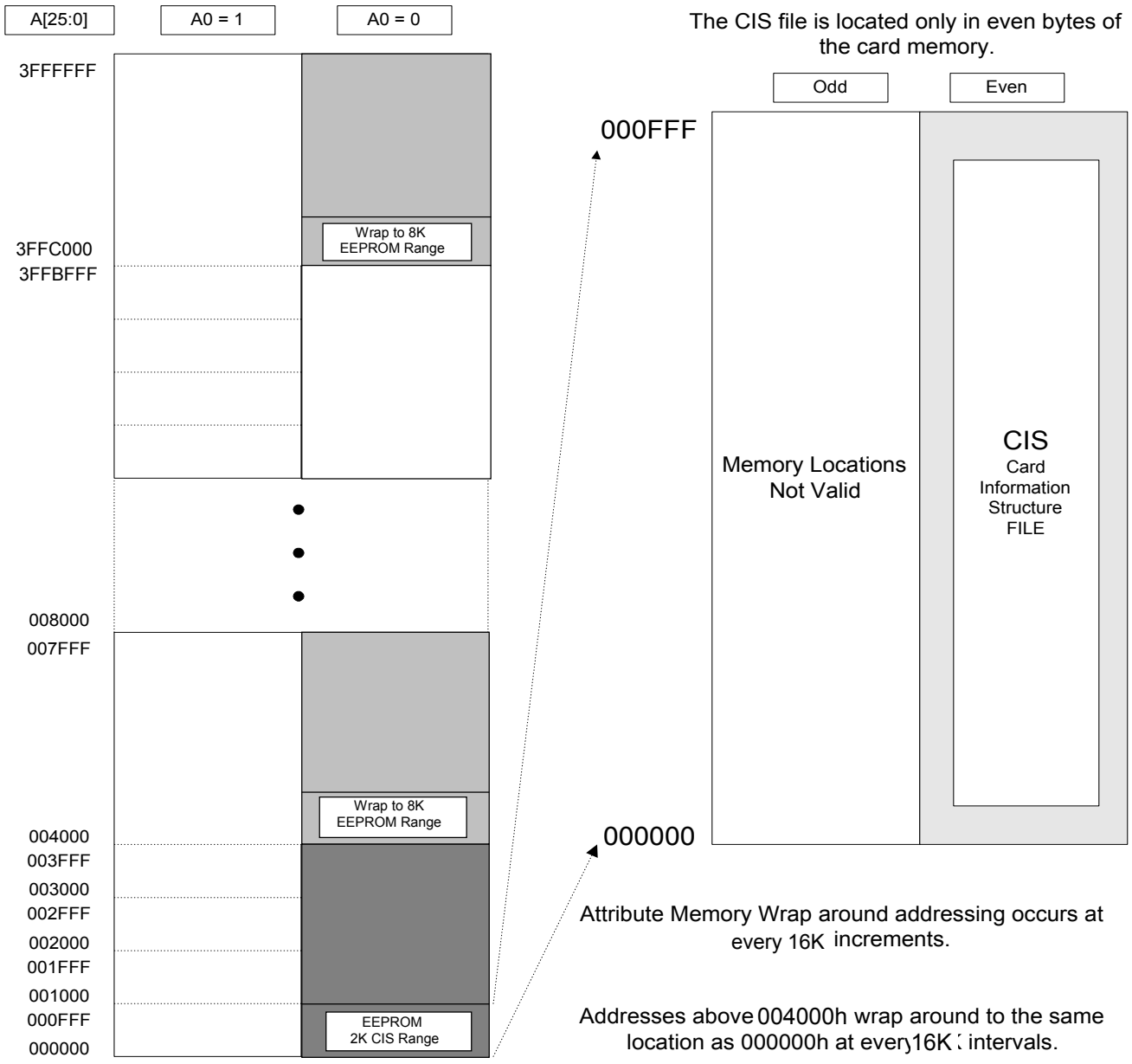
CARD COMMON MEMORY MAP – CARDS BASED ON **28F640J3**



CARD COMMON MEMORY MAP – CARDS BASED ON 28F128J3



ATTRIBUTE MEMORY MAP



COMMAND DEFINITIONS TABLE

Listed in the table shown below, are the standard Command Set codes, detailed descriptions for each are provided on the following pages.

Command Code Sequence	Bus Cyc	1st Bus Cycle				2nd Bus Cycle			
		Bus Opr	Addr	Data		Bus Opr	Addr	Data	
				Even	Odd			Even	Odd
Read Array	1	WRT	X	X	FFh				
Read Identifier Codes	≥2	WRT	X	X	90h	RD	IA		ID
Read Status Register	2	WRT	X	X	70h	RD	X		SRD
Clear Status Register	1	WRT	X	X	50h				
Block Erase	2	WRT	BA	X	20h	WRT	BA		D0h
Byte/Word Write	2	WRT	WA	X	40h or 10h	WRT	WA		WD
Erase Suspend	1	WRT	X	X	B0h				
Erase Resume	1	WRT	X	X	D0h				

Data is latched on the rising edge of /WE (See CARD TIMING CHARACTERISTICS).

Only those commands listed in the above table should be used. Commands not shown in the above table are reserved by the manufacturer for future device implementation.

Legend:

RD = Read operation
WRT = Write operation

X = Any valid address with in a memory device
IA = Identifier Code Address
BA = Address within the block being erased
WA = Address of the memory location to be written

SRD = Data read from status register
WD = Data to be written at location WA
ID = Read identifier code data

Specific memory addresses may be calculated by the following method;

Card Address	Chip Address	Device Number (0 – 4)	Chip Memory Capacity	Binary Shift Left by 1 bit	A0 = 0 = Even byte A0 = 1 = Odd byte
A [25 : 0] =	(Addr + (DP# * 1000000h)) * 2) + A0				

Where: Addr = Chip addresses.
DP# = the device pair number that the memory device belongs to (see Common Memory Map).
A0 = Card address line used for access to even or odd byte of memory.

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Read Array Command :

Cards may be read in Byte wide or Word wide modes. In Word-Wide mode, each byte of memory is independently read from each device pair. Each memory device in the card may read at different rates. Therefore the Host should wait until each byte has a valid data output (See MEMORY BUS OPERATIONS Table for specific Control line States and CARD TIMING CHARACTERISTICS for timing information).

Upon reset of the Card, each memory chip automatically powers up in the Read Array/Reset state in order to prevent spurious data changes during power up, and does not require an additional Read command in order to begin reading data from memory at this time. This operation mode can also be initiated by writing the command code to the internal Write State Machine (WSM) of an individual memory device (See Command Definitions Table). The device remains enabled for read operations until another command is written to the WSM of that device.

Read operations may also be performed after a Block Erase Suspend or Byte Write Suspend command has been initiated (See Sector Erase Suspend Command and Byte Write Suspend Command).

Read Identifier Codes Command :

The identifier code operation is initiated by writing the Read Identifier Codes Command (See Command Definitions Table) to the Write State Machine (WSM) of an individual memory device. Following the command, a read from the chip addresses shown in the table below recalls specific information regarding the chip manufacture and device code.

To terminate the Read identifier Code operation, another valid command must be written to the CUI.

Chip Address (Note 1)	Information / Bit Status	Data
00000h	Manufacture Code (Intel)	89h
00001h	Device Code (28F640J3A)	17h
00001h	Device Code (28F128J3A)	18h
X0002h	Block Lock Configuration **(Note 2)**	
	• Block is unlocked	DQ0 = 0
	• Block is locked	DQ0 = 1
	• Reserved for Future Use **(Note 3)**	DQ[7:1]

Notes:

1. *A0 is not used in either x8 or x16 modes when obtaining the identifier codes. The lowest order address line is A1. Data is always presented on the low byte in x16 mode (upper byte contains 00h)*
2. *The X in the address indicates the specific block of memory to be read.*
3. *DQ{7:1]are invalid and should be ignored.*

Standby Mode of Operation :

During any card operation only certain memory devices are active. Those that are not involved in a specific operation and are not directly made active by control signals can be placed into a reduced power mode by setting the /CE1 and /CE2 signals to a high logic state. Data output bits are then placed in a high-impedance state, independent of /OE. If a device is deselected during block erase or byte write operations, the device continues functioning normally until the operation is completed. At which point the device then enters the Standby Mode.

Each chip may be brought out of standby mode and made active by setting the chip enable signals to a low logic value (See MEMORY BUS OPERATIONS Table for specific control line states, see also DC CHARACTERISTICS for the standby current value).

Deep Power Down Mode of Operation :

The card RESET signal held High for a minimum of 100 ns will initiate a Deep Power Down Mode, which places all output drivers in a high-impedance state and turns off all internal memory chip circuits. During block erase or byte write modes, applying a High RESET signal will abort these operations. It should be noted memory contents involved in an aborted operation may no longer be valid.

In order to exit the Deep Power Down Mode, the RESET signal must be brought to a logic low state. A Wake up period is required before memory read or write operations may be initiated (See CARD TIMING CHARACTERISTICS for the wake up time required). After this wake up period, all common memory components are initialized to the read mode of operation and normal operation may continue.

As with any automated device, it is important to assert RESET during any system wide reset.

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Block Erase Command :

Block Erase is executed one block at a time and initiated by a two cycle command written to the WSM of a memory device (See Command Definitions Table). The erase operation command requires any valid address within a block and will change all data within that block to FFh. The WSM of each memory device will handle all block preconditioning, erase, and verify operations and also automatically updates the device status register data. The Host can detect completion of the operation by analyzing the status register SR7 data bit of the device or by monitoring the Card /BUSY signal. However, in order to determine if an operation has completed successfully without encountering any errors, the status register bits SR5, SR4, SR3, and SR1 of the memory device should also be checked (See Status Register Definitions Table).

A system designer has the following choices when initiating the Block Erase Command:

- The Host may monitor the Status Register 7 bit of each device or the card /BUSY signal to determine when an operation has completed.
- A single operation may be performed, then the appropriate device status register bits checked to determine if the operation completed successfully.
- Multiple operations may be performed, then the appropriate device status register bits checked to determine if all of the operation completed successfully.

Block Erase Suspend/Resume Commands :

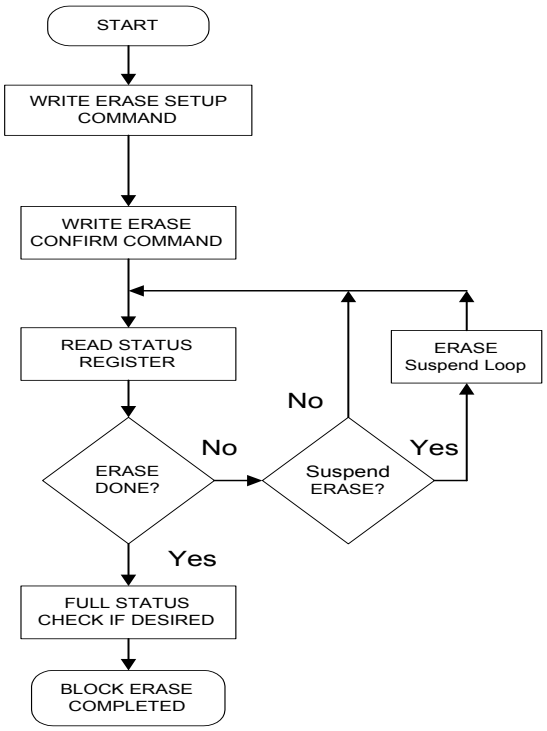
When the Block Erase Suspend command is written to the WSM of a specific device within the card, the WSM will suspend the current block erase operation at a pre-determined point in the algorithm. A Block Erase Suspend command allows the host to issue commands to the WSM with respect to adjacent blocks within the device or other devices within the common memory array. Immediately following the suspend command, polling SR7 and SR6 of the Status Register will identify when the Block Erase command has been suspended.

In suspend mode, Read Array, Write, Read Query, Read Status Register, Clear Status Register, Configure, and Block Erase Resume commands are the only supported commands. Block erase operations for the specific device cannot resume until all operations initiated during the block erase suspend period have been completed.

Writing a Block Erase Resume command to a device within the card instructs the WSM resident in that device to resume the operation of any suspended block erase operations. Status register bits SR7 and SR6 will clear, and subsequent reads of the Status register contents will reflect the status of the block erase command currently in progress.

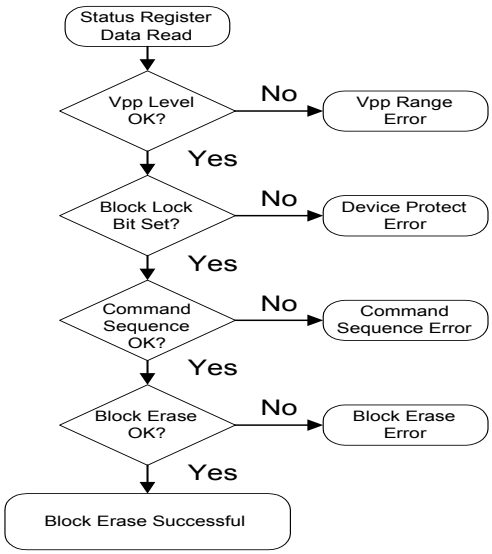
COMMAND DEFINITIONS TABLE *(CONTINUED)*

Block Erase Algorithm Description Table and Diagram :



Command	Bus	Notes
Erase Setup	Write	Data = 20h Address = Block
Erase Confirm	Write	Data = D0h Address = Block
Device Status Register Read	Read	Status Register Data update
	Standby	Check SR7 Bit 1 = Ready, 0 = Busy

Full Status Check Procedure



Bus	Notes
Standby	Check SR3 Bit 1 = Vpp Detected Low
Standby	Check SR1 Bit Block Lock-Bit Set
Standby	Check SR4 and 5 Bit All 1's = Command Sequence Error
Standby	Check SR5 Bit 1 = Block Erase Error

Byte/Word Write Command :

The Byte/Word Write Command is executed via a two-cycle command sequence to the Write State Machine (WSM) of the active device within the card's common memory flash array. Byte/Word write operations can be enabled using either Write Enable (WE#) or Card Enable ($CE_{1,2}$#), data written to the card will be latched on the rising of either signal. The WSM within each device manages the byte/word write, write verify, and the status register contents. The host can detect completion of a write operation command sequence by either monitoring the RDY/BSY# or polling the RDY/BSY# Status Register bit (SR7– ref. Status Register Definitions Table.) When any device within the common memory flash array is busy, only the SR7 register output will be driven by the card. Register bits SR6-SR0 should be ignored, while SR7 is set low. When the status register Write State Machine Status bit transitions to logic high, the remaining status register bits will be driven to a valid logic state. Status register bits SR5, SR4, SR3, and SR1 should be checked to insure successful completion of the write cycle prior to executing subsequent commands

A system designer has the following choices when initiating the Byte Write Command:

- The Host may monitor the Status Register 7 bit of each device or the card /BUSY signal to determine when an operation has completed.
- A single operation may be performed, then the appropriate device status register bits checked to determine if the operation completed successfully.
- Multiple operations may be performed, then the appropriate device status register bits checked to determine if all of the operation completed successfully.

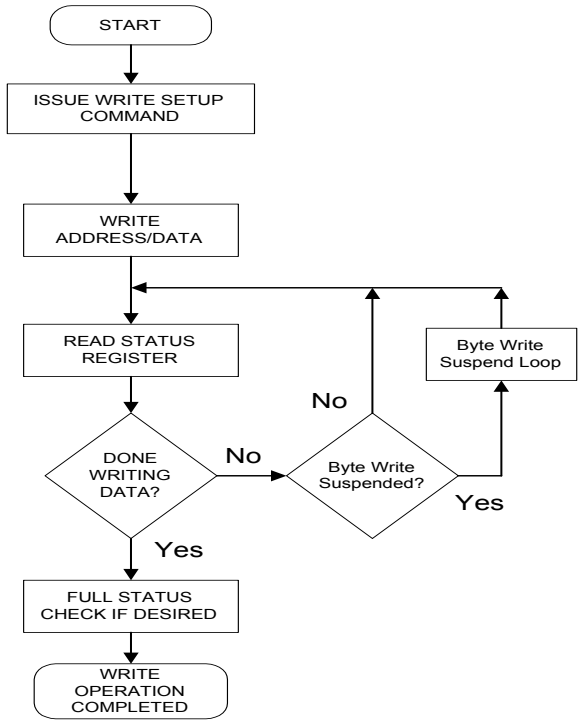
Byte Write Suspend/Resume Commands :

The Byte Write Suspend command allows byte write interruption within a memory device in order to perform read operations in other memory locations of that device. The Byte Write Suspend command instructs the WSM of a device to suspend the byte write operation sequence at a predetermined point in the algorithm. At this point, a Read Array command may be written to the device in order to read data from other locations not involved in the suspended write operation. In order for the Host to determine the status of the operation, a Read Status Register command may be written to the device (See Status Register Definitions Table). Polling the Status Register data bits SR7 and SR2 of the device will indicate that the operation has been suspended. Additionally the card /BUSY signal will indicate that some device is busy.

Writing a Block Erase Resume command to a device instruct the WSM of that device to resume any suspended block erase operations.

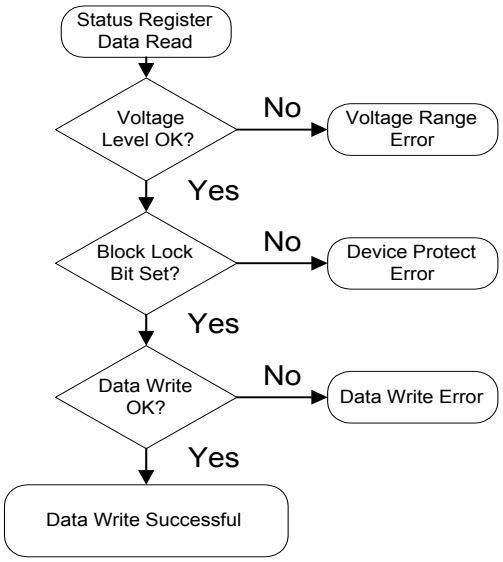
COMMAND DEFINITIONS TABLE *(CONTINUED)*

Byte Write Algorithm Description Table and Flow Chart :



Command	Bus	×8 Mode	×16 Mode
Write Setup	Write	Data = 40h Address = Byte	Data = 40h Address = Word
Data Write	Data Write	Data to be written Address = Byte	Data to be written Address = Word
Device Status Register Read	Read	Status Register Data update	Status Register Data update
	Write	Check SR Bit 7 1 = Ready, 0 = Busy	Check SR Bit 7 1 = Ready, 0 = Busy

Full Status Check Procedure



Bus	×8 Mode	×16 Mode
Standby	Check SR Bit 3 1 = Low Programming Voltage Detected	Check SR Bit 3 1 = Low Programming Voltage Detected
Standby	Check SR Bit 1 1 = Block Lock-Bit Set	Check SR Bit 1 1 = Block Lock-Bit Set
Standby	Check SR Bit 4 1 = Data Write Error	Check SR Bit 4 1 = Data Write Error

Read Status Register Command :

The Status register of each device may be read to determine when a block erase or byte write operation is completed and whether the operation completed successfully (See Status Register Definitions Table). The Status Register Command may be written to a device whenever the device is ready to accept a new command. After which further read operations of the device will output data form the status register of that device until a different command is initiated. In order to update the status register of a device, /OE or /CE must toggle to a logic high value before status information is made current. The status register contents are latched by the device on the falling edge of /OE or /CE, whichever occurs first.

The Host system designer may chose to execute several repeated operations in one or several memory components before checking the Status Register of a given device. In this way the Host is able to execute several operation at once, and then determine if all of the operations completed successfully.

Clear Status Register Command :

Once Status Register bits SR5, SR4, SR3, and SR1 of a memory device have been set to "1"s by the WSM, indicating various failure conditions, only a Clear Status Register Command (50h) will resets all register bits of the device to "0" (See Status Register Definitions Table).

It is important to note that this command is not available during block erase or byte write suspend modes.

COMMAND DEFINITIONS TABLE *(CONTINUED)*

Status Register Definitions Table:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
WSMS	ESS	ECLBS	PSLBS	VPENS	R	DPS	R

Note: *Status Register Data is presented on D[7:0] regardless of x8 or x16 modes. In world wide modes D[15:8] are set to 00h.*

Field and Bit Values	Status Indications
WSMW = Write State Machine Status **(Note 1)** 1 = Ready 0 = Busy	Check RDY/BY or SR7 to determine block erase, byte write, or lock-bit configuration completion.
ESS = Erase Suspend Status 1 = Block Erase Suspended 0 = Block Erase in Progress/Complete	Erase Suspend Status: SR6 may not equal "0" when SR7 equals "0"
ECLBS = Erase Clear Lock-Bits Status **(Note 1)** 1 = Error in Block Erasure or Error Clear Lock-Bits 0 = Successful of Block Eraser of Clear Lock-Bits	If both SR5 and SR4 are "1"s after a block erase or lock-bit operation attempt, an improper command sequence was entered.
PSLBS = Program and Set Lock-Bit Status **(Note 1)** 1 = Error in Programming or Set Master /Block Lock-Bits 0 = Successful Programming or Set Master /Block Lock-Bits	If both SR5 and SR4 are "1"s after a block erase or lock-bit operation attempt, an improper command sequence was entered.
VPENS = Programming Voltage Status **(Note 1)** 1 = Low Programming Voltage Detected, Operation Abort 0 = Programming Voltage OK	The WSM interrogates and indicates the Programming Voltage Status only after Block Erase, Byte Write, Set Lock-Bit, or Clear Lock-Bits command sequence.
R = Reserved for Future Enhancements	Reserved for Future use and should be masked out when polling the status register.
DPS = Device Protect Status **(Note 1)** 1 = Block Lock-Bit, Operation Aborted 0 = Unlock	The WSM interrogates the block lock-bit, and RESET only after Block Erase, Byte Write, or Lock-Bit command sequences. It informs the system if the master lock or a block lock-bit is set.
R = Reserved for Future Enhancements	Reserved for Future use and should be masked out when polling the status register.

Note:

1. *The Block Lock Configuration and Master Lock Configuration features are not yet supported by the chip manufacture and should always be in the unlocked state.*

SCALEABLE COMMAND SET DEFINITIONS TABLE

Command Code Sequence	Bus Cyc.	1st Bus Cycle				2nd Bus CycleData			
		Bus Opr	Addr	Data		Bus Opr	Addr	Data	
				Even	Odd			Even	Odd
Read Query	≥2	WRT	X	X	98h	RD	QA	X	QD
Write to Buffer	≥2	WRT	BA	X	E8h	WRT	BA	X	N
Configuration	2	WRT	X	X	B8h	WRT	X	X	CC

Legend:
RD = Read operation
WRT = Write operation

X = Any valid address with in a memory device or "Don't Care" for data
QA = Query Database Address
QD = Query Data
CC = Configuration Code
N = Byte/Word count to be written to the input Buffer

SCALEABLE COMMAND SET DEFINITIONS TABLE *(CONTINUED)*

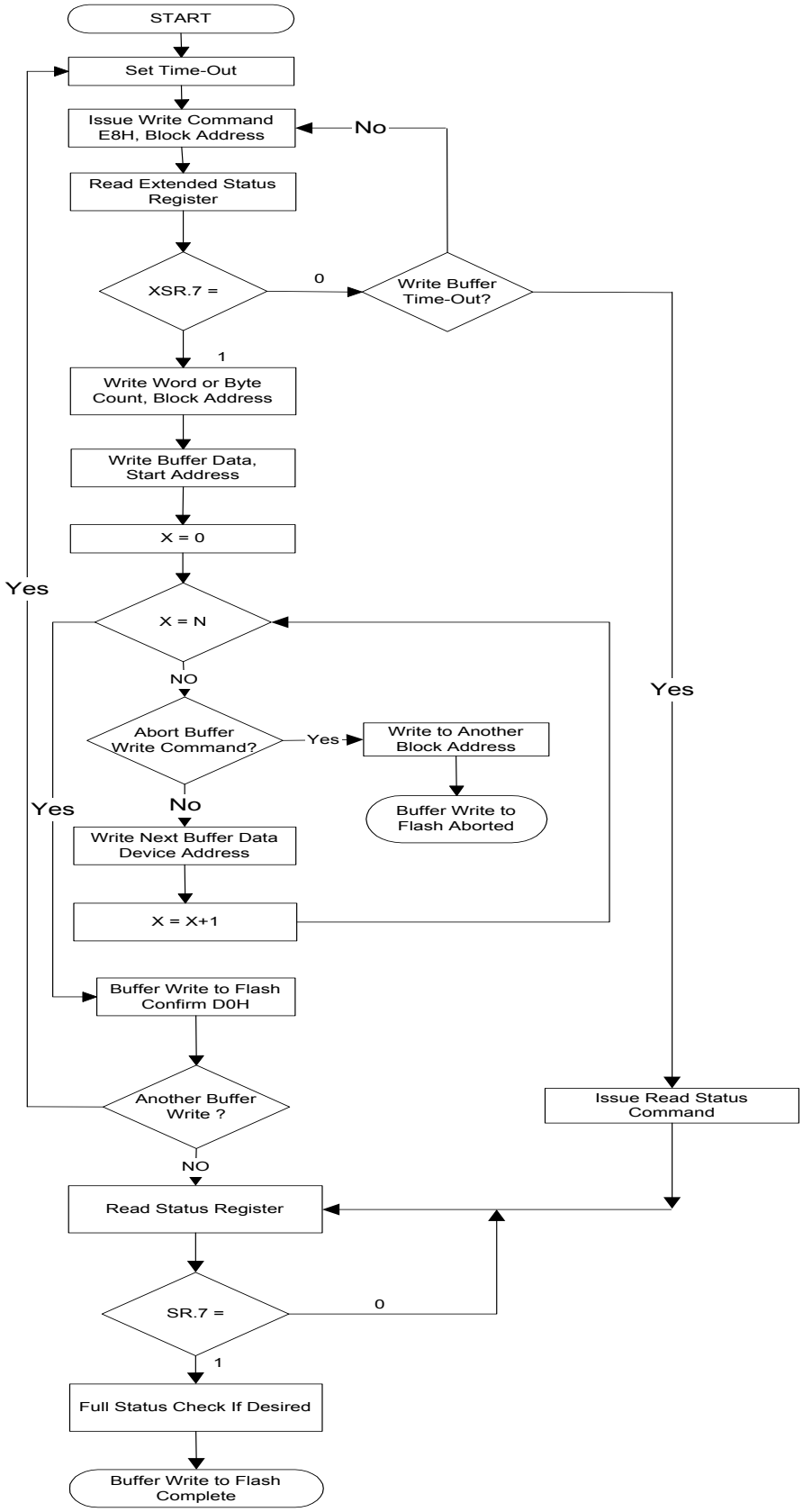
Read Query Mode Command

The Read Query Command is a feature of the Intel Strata Flash Scaleable Command Set (SCS), this command provides the host with access to Common Flash Interface (CFI) information structure. The CFI is an industry standard data structure that allows system level software to evaluate the configuration, electrical characteristics and supported functions of the StrataFlash chip set. CFI is intended to support future upgrades with a standard set of programming algorithms, thus alleviating the need for continued system software modifications and updates.

The data output in response to a Query command will always be presented on the lower eight [D_7-D_0] data lines.

Write to Buffer Command

The Scaleable Command Write to Buffer utilizes an internal 32-byte buffer in each flash device to write up to 32 bytes or 16 words to the card. By programming many flash cells in parallel, the Write to Buffer command provides a 20x performance improvement over conventional single byte write cycle performance. The Write to Buffer command is initiated by first writing the Write to Buffer Command Code (E8h) to the appropriate card/device address, followed by a second write to the same location conveying the number of words or bytes to be written. The card/device address is the starting address of the 128K block location within a specific flash device on the card.


START
Set Time-Out
Issue Write Command E8H, Block Address
No
Read Extended Status Register
XSR.7 =
0
Write Buffer Time-Out?
1
Write Word or Byte Count, Block Address
Write Buffer Data, Start Address
X = 0
Yes
X = N
NO
Yes
Abort Buffer Write Command?
Yes
Write to Another Block Address
Buffer Write to Flash Aborted
Yes
No
Write Next Buffer Data Device Address
X = X+1
Buffer Write to Flash Confirm D0H
Another Buffer Write ?
NO
Issue Read Status Command
Read Status Register
SR.7 =
0
1
Full Status Check If Desired
Buffer Write to Flash Complete

SCALEABLE COMMAND SET DEFINITIONS TABLE *(CONTINUED)*

Configuration Command

The Configuration Command is a Scaleable command that allows the host to configure the RDY/BSY output pin. The default configuration for the device array is level mode Ready/Busy #. The table below summarizes the configuration options available.

NOTE: If a mode other than the default Level Mode is desired the host is required to configure the entire common memory flash array.

STS Pin Configuration Codes	Pulse On Program Complete	Pulse On Erase Complete
	D_1	D_0
Level Mode RDY/BSY# (default)	0	0
Pulse on Erase Complete	0	1
Pulse on Program Complete	1	0
Pulse on Erase or Program Compete	1	1

CARD TIMING CHARACTERISTICS

(Standard operating times for both Common and Attribute Memory unless otherwise noted.)

Read Cycle Timing (/WE = V_{HI})

Parameter	Symbol	Min	Max	Units
Read Cycle Time	t_{AVAV}	120		ns
Address Access Time	t_{AVQV}		120	ns
Card Enable Access Time	t_{ELQV}		120	ns
Output Enable Access Time	t_{GLQV}		50	ns
/OE High to Data Output Disable	t_{GHQZ}		15	ns
/CE Low to Data Output Enable	t_{ELQNZ}	5		ns
Address change to Data no longer valid	t_{AXQX}	0		ns
Address Setup to /OE Low time	t_{AVGL}	20		ns
/OE High Setup to Address time	t_{GHAX}	20		ns
/CE Low Setup to /OE Low time	t_{ELGL}	0		ns
/OE High to /CE High Hold time	t_{GHEH}	20		ns
RESET to Low to Output Access Time	t_{PLQV}		400	ns

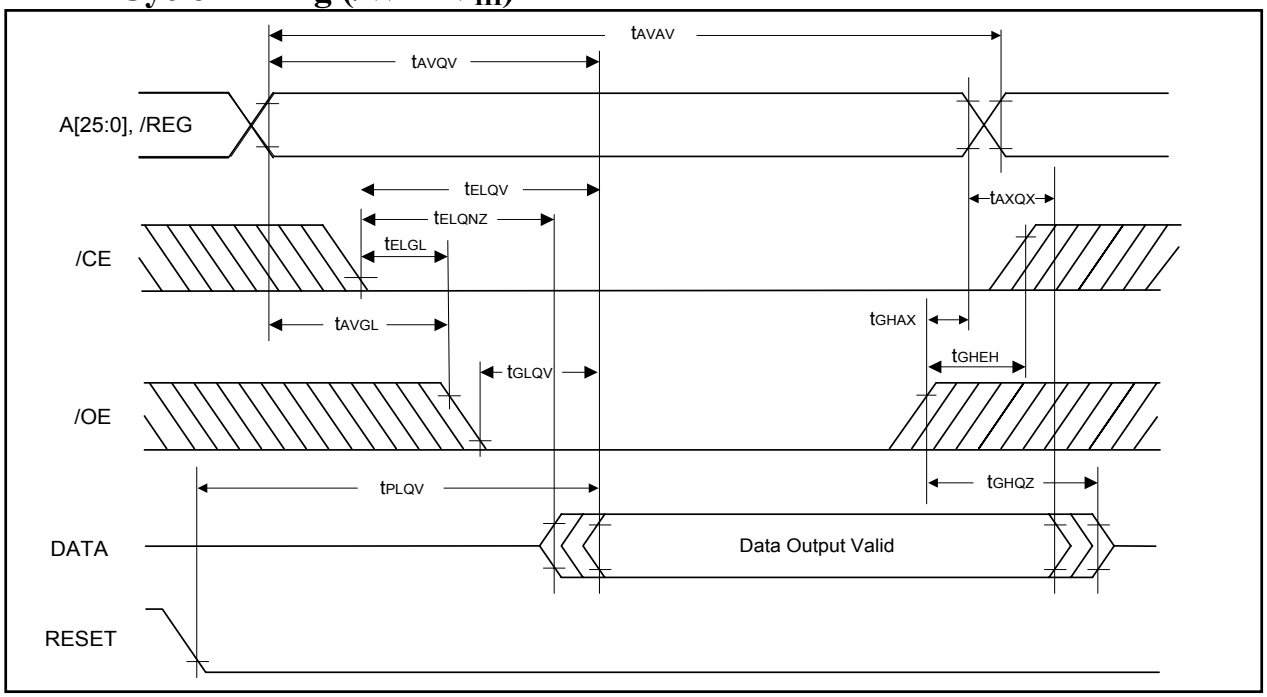
Write Cycle Timing (/OE = V_{HI})

Parameter	Symbol	Min	Max	Units
Write Cycle Time	t_{AVAV}	120		ns
Write Pulse Width	t_{WLWH}	70		ns
Address Setup Time for /WE Low	t_{AVWL}	20		ns
Address Setup to /WE High	t_{AVWH}	55		ns
Card Enable Setup to /WE Low	t_{ELWH}	140		ns
Data Setup to /WE High	t_{DVWH}	50		ns
Data Hold from /WE High	t_{WHDX}	0		ns
Address Hold from /WE High	t_{WHAX}	0		ns
Data Output Disable Time form /WE Low	t_{WLQZ}		90	ns
Data Output Disable Time form /OE Low	t_{GHQZ}		90	ns
/WE High time to Data Output Enable	t_{WHQNZ}	5		ns
/OE Low time to Data Output Enable	t_{GLQNZ}	5		ns
/OE High to /WE Low Setup time	t_{GHWL}	10		ns
/WE High to /OE Low Hold time	t_{WHGL}	10		ns
/CE Low to /WE Low Setup time	t_{ELWL}	0		ns
/WE High to /CE High Hold time	t_{WHEH}	20		ns

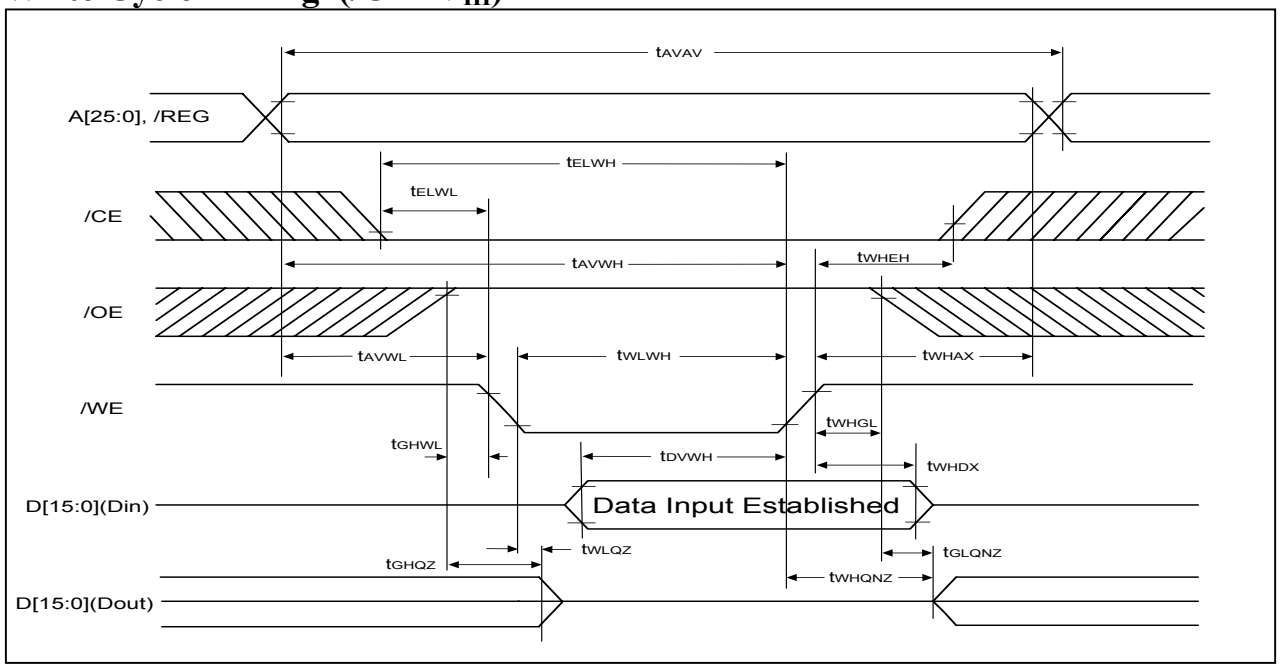
CARD TIMING CHARACTERISTICS *(CONTINUED)*

Common and Attribute Memory Read and Write Cycle Timing.

READ Cycle Timing (/WE=V_{IH})



Write Cycle Timing (/OE=V_{IH})



CARD TIMING CHARACTERISTICS *(NOTE 1)* *(CONTINUED)*

Memory component Timing Characteristics

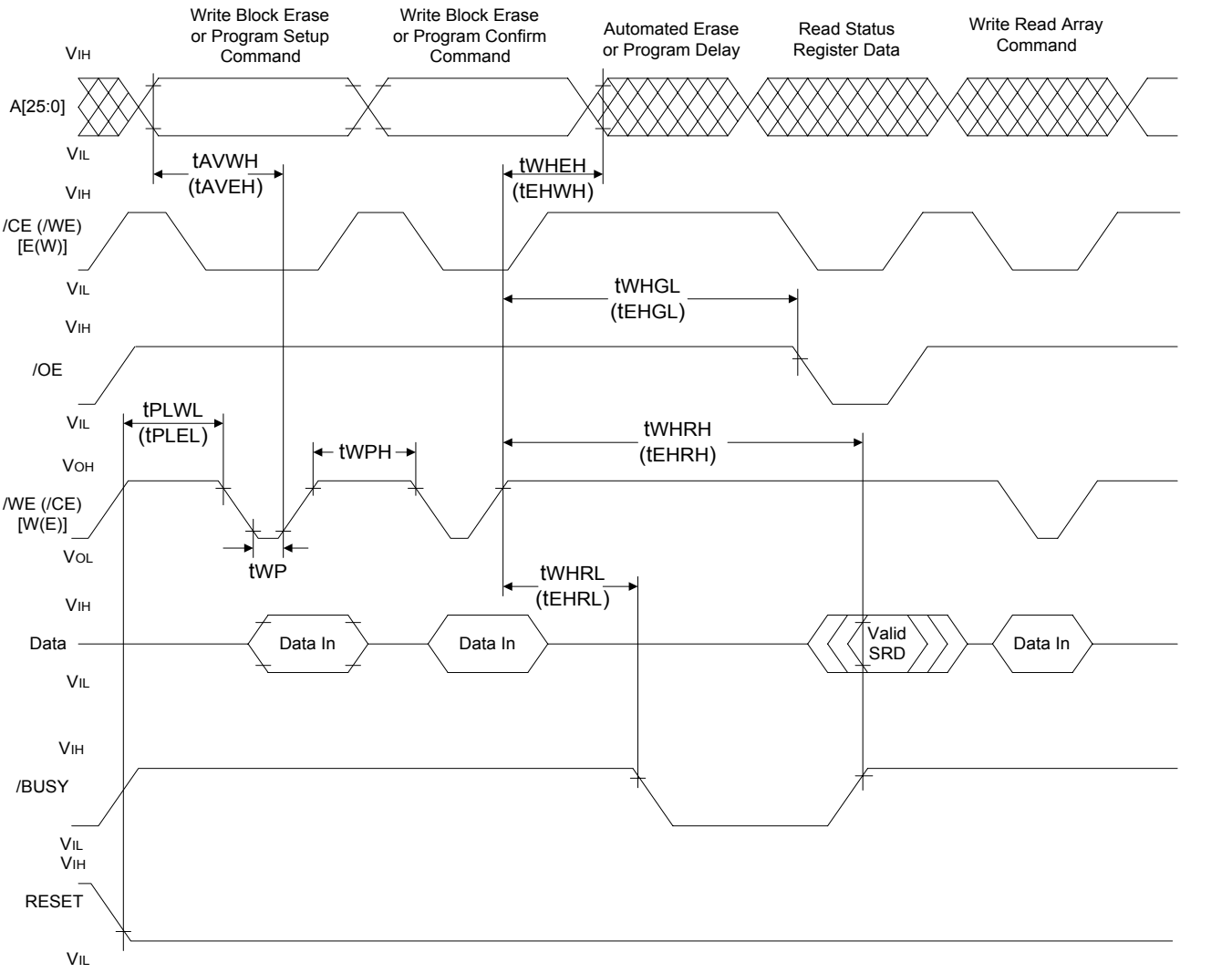
Parameter	Symbol	**Min**	**Max**	**Unit**
RESET Low Recovery to /WE Going Low	t_{PLWL} (t_{PLEL})	1		µs
Address Setup to /WE Going High	t_{AVWH} (t_{AVEH})	40		ns
/CE (/WE) Hold form /WE High	t_{WHEH} (t_{EHWH})	0		ns
Address Hold form /WE High	t_{WHDX} (t_{EHAX})	5		ns
Write Pulse Width	t_{WP}	50		ns
Write Pulse Width High	t_{WPH}	25		ns
Write Recovery before Read	t_{WHGL} (t_{EHGL})	0		ns
/WE High to /BUSY going Low	t_{WHRL} (t_{EHRL})		90	ns

Notes:

1. *Read Timing characteristics during Block Erase/Program Suspend operations are the same as during read operations. Refer to AC Characteristics for read operations.*

CARD TIMING CHARACTERISTICS *(CONTINUED)*

COMMON MEMORY PROGRAM/ERASE TIMING DIAGRAM



Operation Mode (Note1)	Symbol	Min	Typ	Unit
Program Time	t_{WHRH} (t_{EHRH})	6.5	8	µs
Block Erase		0.9	1.1	sec
Program Suspend			5	µs
Erase Suspend			9.6	µs

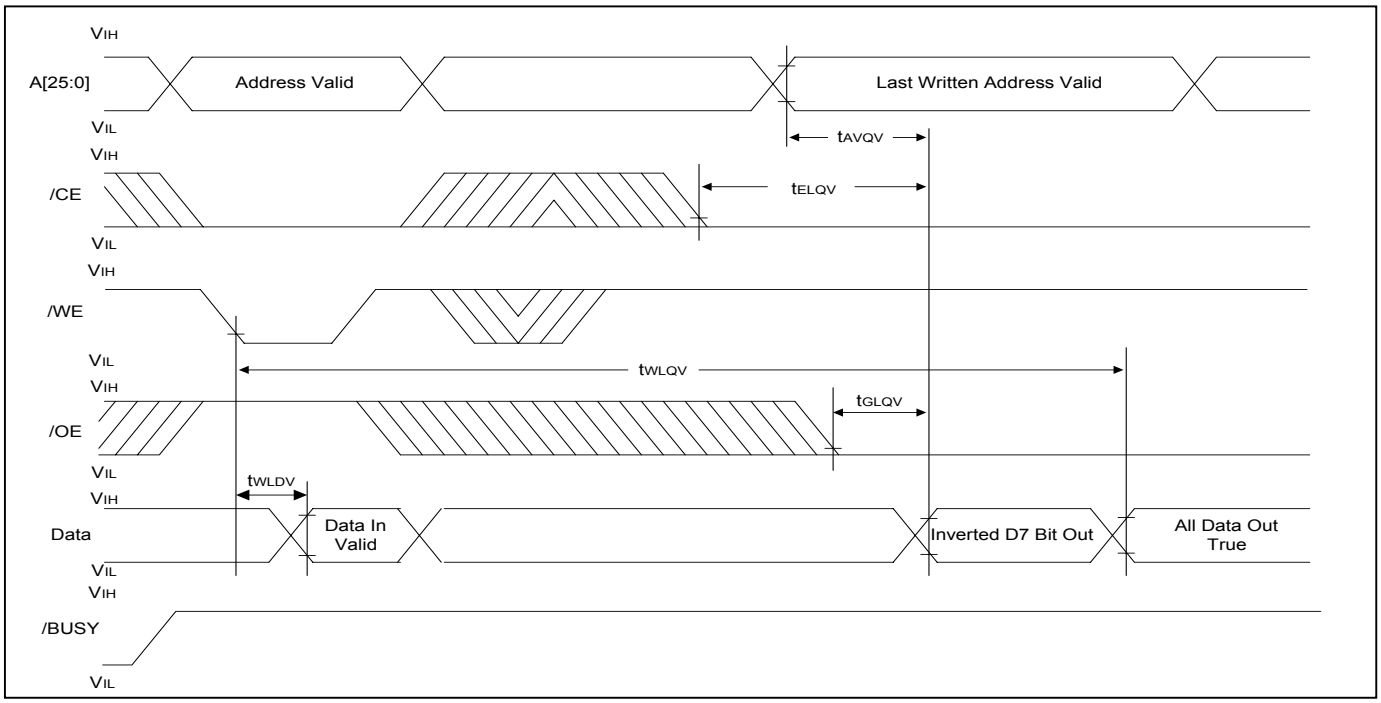
***Note**:*

1. Maximum values are To Be Determined. (TBD).

Corporate Headquarters: P. O. Box 1757, Fremont, CA 94538, USA • Tel:(510) 623-1231 • Fax:(510) 623-1434 • E-mail: info@smartm.com
Flash Design Center: 7 Lopez Road, Wilmington , MA 01887 USA • Tel:(978) 988-8848 • Fax:(978) 988-7651 • Customers@Smartm.com
Europe: 5 Kelvin Park South, Kelvin South, East Kilbride, G75 ORH, United Kingdom• Tel: +44-870-870-8747 • Fax: +44-870-870-8757
Asia: Plot 18, Lrg Jelawat 4, Kawasan Perindustrian Seberang Jaya 13700, Prai, Penang, Malaysia • Tel: +604-3992909 • Fax: +604-3992903

CARD TIMING CHARACTERISTICS *(CONTINUED)*

ATTRIBUTE MEMORY TIMING DIAGRAM



Attribute Parameter (Note 1, 2)	Symbol	Min	Max	Unit
Read Cycle Time	t_{AVAV}	120		ns
Card Enable Access Time	t_{ELQV}		200	ns
Output Enable Access Time	t_{GLQV}		70	ns
Write Enable Low to Data Valid Time	t_{WLDV}		1000	ns
Write Enable Low to Data Read Valid Time	t_{WLQV}		1	ms

Note:

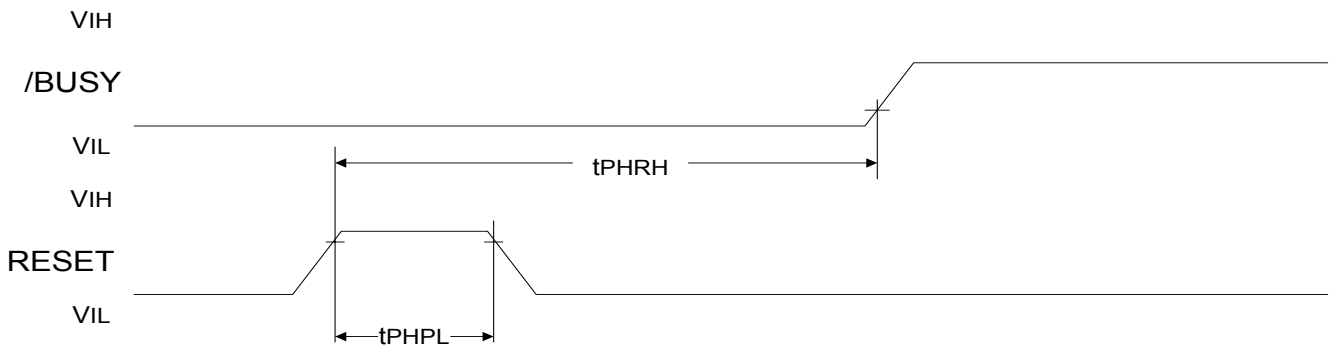
1. *All timing values are constant with standard Read/Write Times, unless otherwise shown in the Table.*
2. *Attribute memory latches address values on the falling edge of /WE. Data is latched on the rising edge of /WE.*

Attribute Data Polling Mode :

Data Polling the 28C16A features /DATA polling to signal the completion of a byte write cycle. During a write cycle, an attempt to read the last byte written to memory will produce the complement of the D7 (D6 to D0 are indeterminate). After completion the true data is available. Data Polling allows a simple read/compare operation to determine the status of the chip.

CARD TIMING CHARACTERISTICS *(CONTINUED)*

RESET TIMING DIAGRAM



Parameter	Symbol	Min	Max	Unit
RESET High Time	t_{PHPL}	100		ns
RESET High to Reset during Block Erase or Program **(Note 1,2)**	t_{PHRH}		12	µs

Note:

1. *If RESET is asserted High when the WSM is not busy (/BUSY = "1"), the reset will complete within 100 ns.*
2. *A reset time or Wake up period, t_{PLQV}, is required from RESET going high until outputs are valid.*

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min.	Max.	Units
Vcc Supply Voltage	Vcc	4.5	5.5	V
Operating Temperature	T_A	0	70	°C

DC CHARACTERISTICS

Supply current is an RMS value. Typical values at nominal V_{CC} voltage at T_A = +25°C.

Symbol	Parameter	Condition	Typ	Max	Units
I_{CCS}	Standby Current **(Notes 2, 3)**	Per device: CMOS; V_{CC} = V_{CC} Max /CE1, /CE2, = V_{CC} ±0.2V RESET = GND ± 0.2V	50	150	µA
I_{CCD}	V_{CC} Deep Power-Down Current	RESET = V_{CC} ±0.2V I_{OUT} = 0 **(Full 20 MB capacity)**	350		µA
I_{CCR}	Active Read Current **(Note 1, 3)**	CMOS; V_{CC} = V_{CC} Max /CE1 or /CE2 = GND f = 8MHZ, I_{OUT} = 0mA **Byte (×8)**	20	35	mA
		Byte (×16)	40	70	mA
I_{CCW}	Active Program Current **(Note 1, 4)**	Per device (including programming current)		75	mA
I_{CCE}	Active Block Erase Current **(Note 4)**	Per device (including programming current)		50	mA
I_{CCWS} I_{CCES}	Program Suspend or Block Erase Suspend Current	Per device /CE1, /CE2 = V_{IH}	1	10	mA
I_{IL}	Input Leakage Current	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin		±20	µA
I_{ILpu}	Input Leakage Current with Pull Up Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 10KΩ pull up resistor		+500	µA
I_{ILpd}	Input Leakage Current with Pull Down Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 100KΩ pull down resistor		-50	µA
I_{OLpd}	Output Leakage Current with Pull Down Resistor	V_{IN} = GND to V_{CC}, $V_{CC\ MAX}$ Per Pin with 100KΩ pull down resistor		-50	µA
V_{IL}	Input Low Voltage **(Note 4)**		-0.5	0.8	V
V_{IH}	Input High Voltage **(Note 4)**		0.7 × V_{CC}	V_{CC} +0.5	V
V_{OL}	Output Low Voltage **(Notes 2,4)**	V_{CC} = V_{CC} Min I_{OL} = 2 mA (3.3V) = 5.8 mA (5V)		0.45	V
V_{OH}	Output High Voltage **(Notes 2,4)**	CMOS; V_{CC} = V_{CC} Min I_{out} = -2.5mA	0.85 × V_{CC}		V
		CMOS; V_{CC} = V_{CC} Min I_{out} = -100µA	V_{CC} -0.4		V

Notes:

1. *I_{CCWS} and I_{CCES} are specified with the device deselected. If read or written while in erase suspend mode, the device's current is the sum of I_{CCWS} or I_{CCWS} and I_{CCR} or I_{CCW}.*
2. *Includes /BUSY.*
3. *CMOS inputs are either VCC ± 0.2V or GND ± 0.2V.*
4. *Sample tested by component manufacturer.*

CARD INFORMATION STRUCTURE

The CIS is data which describes the PCMCIA card and is described by the PCMCIA standard. This information can be used by the Host system to determine a number of things about the card that has been inserted. For information regarding the exact nature of this data, and how to design Host software to interpret it, refer to the PCMCIA standard Metaformat Specification.

Physical Address	Logical Address	Data Value(s)	Tuple Description
00h	00h	01h	CISTPL_DEVICE
02h	01h	03h	CISTPL_LINK
04h	02h	52h	Speed = 200ns, WPS=Yes, FLASH
06h	03h	**FEh (Note 1)**	Bits 2-0 = 110b = 2 Meg units, Bits 7-3 = 11111b = 32 Units (0=1, 1=2...) 2 Meg x 32 Units = 64 Meg size
08h	04h	FFh	CISTPL_END - End of Tuple

0Ah	05h	18h	CISTPL_JEDEC
0Ch	06h	03h	CISTPL_LINK
0Eh	07h	89h	Manufacturer ID (Intel)
10h	08h	18h (17h)	Device ID 28F128J3 (Device ID 28F640J3)
12h	09h	FFh	CISTPL_END - End of Tuple

14h	0Ah	1Eh	CISTPL_DEVICEGEO
16h	0Bh	07h	CISTPL_LINK
18h	0Ch	02h	DGTPL_BUS - Bus Width - 2 Bytes
1Ah	0Dh	12h	DGTPL_EBS - Erase Block Size 2^11h = 128K Bytes or Words
1Ch	0Eh	01h	DGTPL_RBS - Byte Accessible
1Eh	0Fh	01h	DGTPL_WBS - Byte Accessible
20h	10h	01h	DGTPL_PART - One Partition
22h	11h	01h	DGTPL_HWIL - No Interleave
24h	12h	FFh	CISTPL_END - End of Tuple

CARD INFORMATION STRUCTURE *(CONTINUED)*

Physical Address	Logical Address	Data Value(s)	Tuple Description
26h	13h	15h	CISTPL_VERS1
28h	14h	56h	CISTPL_LINK
2Ah	15h	04h	TPLLV1_MAJOR (PCMCIA 2.1/JEIDA 4.2)
2Ch	16h	01h	TPLLV1_MINOR
2Eh...60h	17h...30h	53 6D 61 72 74 20 4D 6F 64 75 6C 61 72 20 54 65 63 68 6E 6F 6C 6F 67 69 65 73	ASCII Text is : Smart Modular Technologies. {26 Characters total}
62h	31h	00	NULL String Delimiter (String 1)
64h...84h	32h...42h	**46 4C 36 34** **4D 2D 32 30** **2D 31 31 37** **33 37 2D 4A** **33 (Note 2)**	ASCII Text is : FL64M-20-11737-J3 {17 Characters total}
86h	43h	00	NULL String Delimiter (String 2)
88h...CEh	44h...67h	**36 34** 20 4D **(Note 3)** 45 47 20 46 4C 41 53 48 20 77 **31 32** (2F 36 34) **38** 20 4D 62 69 74 20 49 6E 74 65 6C 20 64 65 76 69 63 65 73	ASCII Text is : 64 MEG FLASH w128 Mbit Intel devices (w/64) {36 Characters total}
D0h	68h	00	NULL String Delimiter (String 3)
D2h	69h	00	NULL String Delimiter (String 4)
D4h	6Ah	FF	CISTPL_END - End of Tuple
D6h	6Bh	FF	CISTPL_END - End of Chain Tuple

CARD INFORMATION STRUCTURE *(CONTINUED)*

Note:

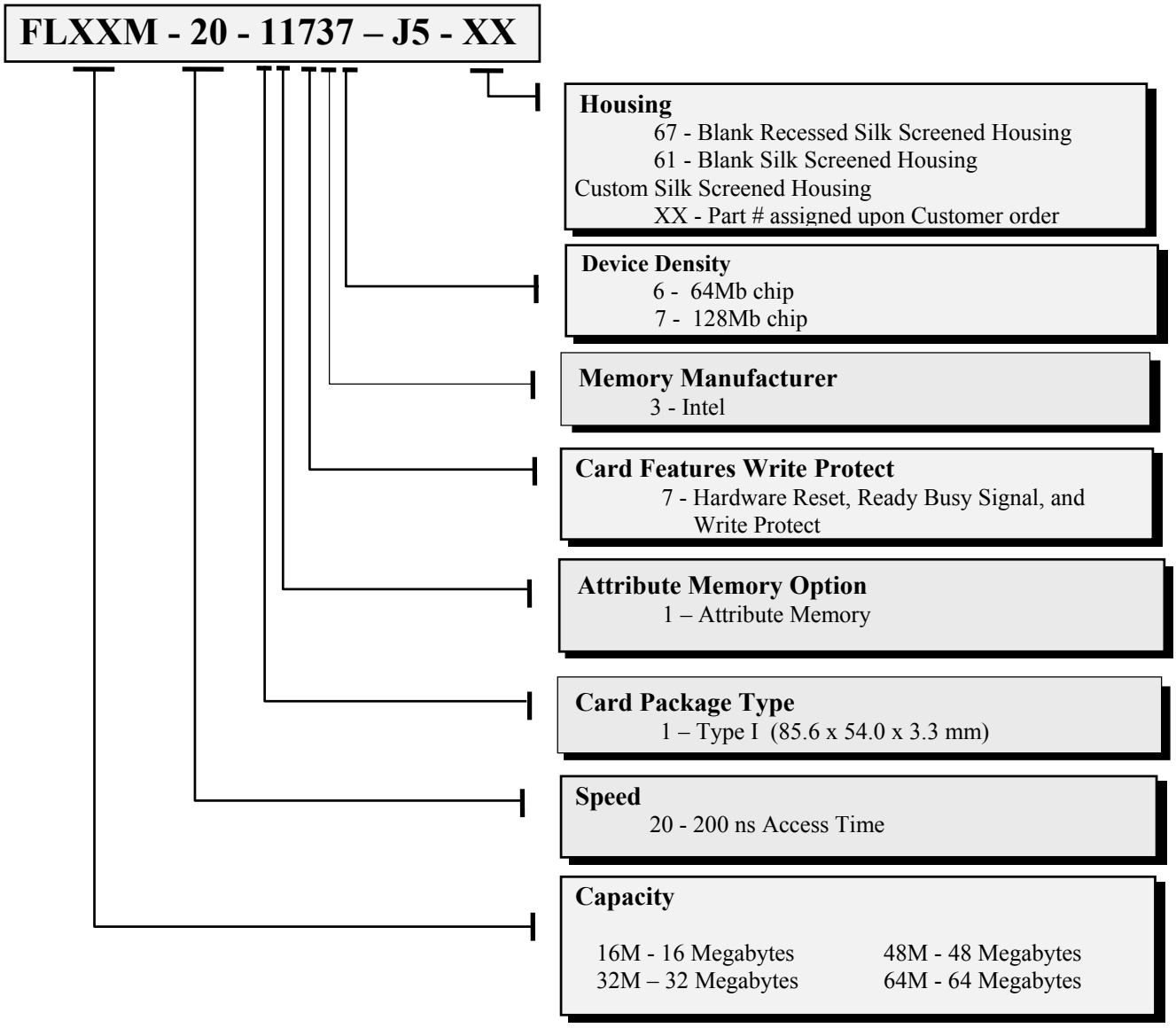
1. *Refer to the table (right) for Smart Modular part numbers and corresponding data value.*
2. *Specific Product description will be listed (See Note 1 Part Numbers).*
3. *Specific Product memory capacities will be listed for specific products.*

Part Number	Data value
FL08M-20-11736-J3	1Eh
FL16M-20-11737-J3	3Eh
FL16M-20-11736-J3	3Eh
FL32M-20-11737-J3	7Eh
FL32M-20-11736-J3	7Eh
FL48M-20-11737-J3	BEh
FL64M-20-11737-J3	FEh

SALES AND SUPPORT

To order or to obtain information on pricing or delivery, contact a Smart Modular Technologies Sales and Support representative. (See AVAILABLE CONFIGURATIONS on the following page.)

PART NUMBER INFORMATION



Variations of this standard Smart Modular Technologies Product are available.
Contact a Smart Sales Representative for additional information.

ORDERING INFORMATION

SG - RoHS products
SM – non RoHS products

	Ordering part numbers	
Description	***RoHS***	***non RoHS***
FL08M-20-10636-J5	SG9F0083P3205	SM9F0083P3205
FL08M-20-11736-J5	SG9FA083P3205	SM9FA083P3205
FL16M-20-11737-J5		
FL16M-20-11736-J5	SG9FA163P3205	SM9FA163P3205
FL32M-20-11737-J5		
FL32M-20-11736-J5	SG9FA323P3205	SM9FA323P3205
FL48M-20-11737-J5	SG9FA483P3205	SM9FA483P3205
FL64M-20-11737-J5	SG9FA643P3205	SM9FA643P3205

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