Ordering Information

Part Number	Description	Device Vendor
STI1027RD410893SC	1Gx72 (8GB), DDR4, 288-Pin Registered DIMM, Parity, ECC, 1Gx8 Based, DDR4-2666-19-19-19, 31.25mm, 1.2V, Halogen-Free & RoHS Compliant, Industrial Temperature[1].	Samsung, Rev. C K4A8G085WC-BCTD[2]

Notes:
1. Industrial Temperature = -40 to +85°C (Ambient).
2. Commercial temperature devices are tested by SMART at -40°C and 85°C for operation at the Industrial Temperature range.

(All specifications of this module are subject to change without notice.)

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Part Number Decode

S	T	I	102	7	RD4	108	9	3	S	C
1	2	3	4	5	6	7	8	9	10	11

1	**SMART Modular Technologies**
2	**Module Process Technology** T: RoHS Compliant DDR4 Enterprise
3	**Operating Temperature** I: Industrial Temperature Testing
4	**Module Address Depth** 102: 1G
5	**Module Data Bus Width** 7: x72
6	**Module Configuration** RD4: 1.2V DDR4 288-Pin Registered DIMM
7	**Device Configuration** 108: 1Gx8 Based
8	**CAS Latency** 9: CL 19
9	**Device Speed** 3: DDR4-2666
10	**Device Vendor** S: Samsung
11	**Device Revision** C: Revision C

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Revision History

Date	Description
March 27, 2018	Datasheet released.

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8GB (1Gx72) DDR4 SDRAM Module - 1Gx8 Based
288-Pin Registered DIMM, Parity, ECC

Features

- Standard = JEDEC
- Configuration = ECC
- Number of Module Ranks = 1 Rank
- Number of Devices = 9
- $V_{DD} = V_{DDQ} = 1.2V$
- $V_{PP} = 2.5V$
- $V_{DDSPD} = 2.25V$ to 2.75V
- Cycle Time = 0.75ns
- $\overline{CAS}$ Latency = 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
- $\overline{CAS}$ Latency with Read DBI = 12, 13, 14, 15, 17, 18, 19, 20, 21, 22, 23
- Additive Latency = 0, CL - 1, and CL - 2
- $\overline{CAS}$ Write Latency (CWL) = 9, 10, 11, 12, 14, 16,18
- Burst Length (BL) switch on-the-fly BL8 or BC4 (Burst Chop)
- Burst Type = Sequential & Interleave
- Bi-Directional Differential Data Strobe
- On-Die Termination (ODT)
- 8 bit pre-fetch
- Device Package = FBGA
- Lead Finish = ≥ 0.76µm Gold
- Length x Height = 133.35mm x 31.25mm
- No. of sides = Double-sided
- Mating Connector (Examples)
  - Vertical = Molex - 0787261002
  - Vertical = TE Connectivity - 2199154-2
- Bank Grouping is applied, and $\overline{CAS}$ to $\overline{CAS}$ latency (t_{CCD_L}, t_{CCD_S}) for the banks in the same or different bank group accesses are available
- Supports ECC error correction and detection
- Temperature sensor with integrated SPD
- Per DRAM Addressability is supported
- Internal V_{REF} DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported (x8)
- CA parity (Command/Address Parity) mode is supported

Addressing

Device Configuration	1Gx8
Number of Bank Groups	4
Bank Groups	BG0 - BG1
Bank Address	BA0 - BA1
Row Address	A0 - A15
Column Address	A0 - A9
Page size	1KB

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Pin Description Table

Symbol	Type	Function
CK0-CK1, CK0-CK1	Input	Clock: CK and CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK.
CKE0	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power- Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After V_{REFCA} and Internal DQ V_{REF} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self- Refresh.
CS0	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
ODT0	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM/DBI/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT	Input	Activation Command Input: ACT defines the Activation command being entered along with CS. The input into RAS/A16, CAS/A15 and WE/A14 will be considered as Row Address A16, A15 and A14.
RAS/A16, CAS/A15, WE/A14	Input	Command Inputs: RAS/A16, CAS/A15 and WE/A14 (along with CS) define the command being entered. Those pins have multi function. For example, for activation with ACT Low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT High, those are Command pins for Read, Write and other command defined in command truth table.
DM0/DBI0/ TDQS0- DM8/DBI8/ TDQS8	Input/ Output	Input Data Mask and Data Bus Inversion: DM is an input mask signal for write data. Input data is masked when DM is sampled LOW coincident with that input data during a Write access. DM is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. The function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI is an input/output identifying whether to store/output the true or inverted data. If DBI is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI is HIGH.
BG0-BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0-BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0-A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC, RAS/A16, CAS/A15 and WE/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is connected to the register for the CA parity check.
A10/AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/BC	Input	Burst Chop: A12/BC is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET	Input	Active Low Asynchronous Reset: Reset is active when RESET is LOW, and inactive when RESET is HIGH. RESET must be HIGH during normal operation. RESET is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.

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Pin Description Table (Continued)

Symbol	Type	Function
DQ0-DQ63 CB0-CB7	Input/ Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal V_{REF} level during test via Mode Register Setting MR4 A4 = HIGH.
DQS0-DQS8 $\overline{DQS0}$-$\overline{DQS8}$	Input/ Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS0-TDQS8 $\overline{TDQS0}$-$\overline{TDQS8}$	Output	Termination Data Strobe: TDQS/$\overline{TDQS}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11 = 0 in MR1, $\overline{DM}$/$\overline{DBI}$/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and $\overline{TDQS}$ is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with $\overline{CS}$ LOW.
$\overline{ALERT}$	Input/ Output	Alert: It has multiple functions, such as CRC error flag, or Command and Address Parity error flag. If there is error in the CRC, then $\overline{ALERT}$ goes LOW for a period of time and goes back HIGH. If there is error in the Command Address Parity Check, then $\overline{ALERT}$ goes LOW for a relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case it is not connected, $\overline{ALERT}$ Pin must be connected to V_{DD} on the board.
SA0-SA2	Input	These signals are tied at the system to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	Input/ Output	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pull-up on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus tied to V_{DDSPD} to act as a pull-up on the system board.
$\overline{EVENT}$	Output	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part. No pull-up resister is provided on DIMM.
NC	-	No Connect.
V_{DD}	Supply	Power Supply.
V_{SS}	Supply	Ground.
V_{PP}	Supply	DRAM Activating Power Supply.
V_{REFCA}	Supply	Reference voltage for address/command inputs.
V_{DDSPD}	Supply	Power supply for SPD EEPROM/Thermal Sensor.
V_{TT}	Supply	Termination voltage for address/command/control/clock nets.

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DDR4 288-Pin Registered DIMM Pin List

Front Side						Back Side					
Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	NC	49	CB0	97	DQ32	145	NC	193	V_{SS}	241	V_{SS}
2	V_{SS}	50	V_{SS}	98	V_{SS}	146	V_{REFCA}	194	CB1	242	DQ33
3	DQ4	51	$\overline{DM8}/\overline{DBI8}$/ TDQS17	99	$\overline{DM4}/\overline{DBI4}$/ TDQS13	147	V_{SS}	195	V_{SS}	243	V_{SS}
4	V_{SS}	52	NC/$\overline{TDQS17}$	100	NC/$\overline{TDQS13}$	148	DQ5	196	$\overline{DQS8}$	244	$\overline{DQS4}$
5	DQ0	53	V_{SS}	101	V_{SS}	149	V_{SS}	197	DQS8	245	DQS4
6	V_{SS}	54	CB6	102	DQ38	150	DQ1	198	V_{SS}	246	V_{SS}
7	$\overline{DM0}/\overline{DBI0}$/ TDQS9	55	V_{SS}	103	V_{SS}	151	V_{SS}	199	CB7	247	DQ39
8	NC/$\overline{TDQS9}$	56	CB2	104	DQ34	152	$\overline{DQS0}$	200	V_{SS}	248	V_{SS}
9	V_{SS}	57	V_{SS}	105	V_{SS}	153	DQS0	201	CB3	249	DQ35
10	DQ6	58	$\overline{RESET}$	106	DQ44	154	V_{SS}	202	V_{SS}	250	V_{SS}
11	V_{SS}	59	V_{DD}	107	V_{SS}	155	DQ7	203	CKE1 (NC)	251	DQ45
12	DQ2	60	CKE0	108	DQ40	156	V_{SS}	204	V_{DD}	252	V_{SS}
13	V_{SS}	61	V_{DD}	109	V_{SS}	157	DQ3	205	RFU	253	DQ41
14	DQ12	62	$\overline{ACT}$	110	$\overline{DM5}/\overline{DBI5}$/ TDQS14	158	V_{SS}	206	V_{DD}	254	V_{SS}
15	V_{SS}	63	BG0	111	NC/$\overline{TDQS14}$	159	DQ13	207	BG1	255	$\overline{DQS5}$
16	DQ8	64	V_{DD}	112	V_{SS}	160	V_{SS}	208	$\overline{ALERT}$	256	DQS5
17	V_{SS}	65	A12/$\overline{BC}$	113	DQ46	161	DQ9	209	V_{DD}	257	V_{SS}
18	$\overline{DM1}/\overline{DBI1}$/ TDQS10	66	A9	114	V_{SS}	162	V_{SS}	210	A11	258	DQ47
19	NC/$\overline{TDQS10}$	67	V_{DD}	115	DQ42	163	$\overline{DQS1}$	211	A7	259	V_{SS}
20	V_{SS}	68	A8	116	V_{SS}	164	DQS1	212	V_{DD}	260	DQ43
21	DQ14	69	A6	117	DQ52	165	V_{SS}	213	A5	261	V_{SS}
22	V_{SS}	70	V_{DD}	118	V_{SS}	166	DQ15	214	A4	262	DQ53
23	DQ10	71	A3	119	DQ48	167	V_{SS}	215	V_{DD}	263	V_{SS}
24	V_{SS}	72	A1	120	V_{SS}	168	DQ11	216	A2	264	DQ49
25	DQ20	73	V_{DD}	121	$\overline{DM6}/\overline{DBI6}$/ TDQS15	169	V_{SS}	217	V_{DD}	265	V_{SS}
26	V_{SS}	74	CK0	122	NC/$\overline{TDQS15}$	170	DQ21	218	CK1	266	$\overline{DQS6}$
27	DQ16	75	$\overline{CK0}$	123	V_{SS}	171	V_{SS}	219	$\overline{CK1}$	267	DQS6
28	V_{SS}	76	V_{DD}	124	DQ54	172	DQ17	220	V_{DD}	268	V_{SS}

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DDR4 288-Pin Registered DIMM Pin List

Front Side						Back Side					
Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
29	$\overline{DM2}/\overline{DBI2}$/ TDQS11	77	V_{TT}	125	V_{SS}	173	V_{SS}	221	V_{TT}	269	DQ55
30	NC/$\overline{TDQS11}$	78	$\overline{EVENT}$	126	DQ50	174	$\overline{DQS2}$	222	PARITY	270	V_{SS}
31	V_{SS}	79	A0	127	V_{SS}	175	DQS2	223	V_{DD}	271	DQ51
32	DQ22	80	V_{DD}	128	DQ60	176	V_{SS}	224	BA1	272	V_{SS}
33	V_{SS}	81	BA0	129	V_{SS}	177	DQ23	225	A10/AP	273	DQ61
34	DQ18	82	$\overline{RAS}$/A16	130	DQ56	178	V_{SS}	226	V_{DD}	274	V_{SS}
35	V_{SS}	83	V_{DD}	131	V_{SS}	179	DQ19	227	RFU	275	DQ57
36	DQ28	84	$\overline{CS0}$	132	$\overline{DM7}/\overline{DBI7}$/ TDQS16	180	V_{SS}	228	$\overline{WE}$/A14	276	V_{SS}
37	V_{SS}	85	V_{DD}	133	NC/$\overline{TDQS16}$	181	DQ29	229	V_{DD}	277	$\overline{DQS7}$
38	DQ24	86	$\overline{CAS}$/A15	134	V_{SS}	182	V_{SS}	230	NC	278	DQS7
39	V_{SS}	87	ODT0	135	DQ62	183	DQ25	231	V_{DD}	279	V_{SS}
40	$\overline{DM3}/\overline{DBI3}$/ TDQS12	88	V_{DD}	136	V_{SS}	184	V_{SS}	232	A13	280	DQ63
41	NC/$\overline{TDQS12}$	89	$\overline{CS1}$ (NC)	137	DQ58	185	$\overline{DQS3}$	233	V_{DD}	281	V_{SS}
42	V_{SS}	90	V_{DD}	138	V_{SS}	186	DQS3	234	A17	282	DQ59
43	DQ30	91	ODT1 (NC)	139	SA0	187	V_{SS}	235	NC	283	V_{SS}
44	V_{SS}	92	V_{DD}	140	SA1	188	DQ31	236	V_{DD}	284	V_{DDSPD}
45	DQ26	93	$\overline{CS2}$ (NC)	141	SCL	189	V_{SS}	237	$\overline{CS3}$ (NC)	285	SDA
46	V_{SS}	94	V_{SS}	142	V_{PP}	190	DQ27	238	SA2	286	V_{PP}
47	CB4	95	DQ36	143	V_{PP}	191	V_{SS}	239	V_{SS}	287	V_{PP}
48	V_{SS}	96	V_{SS}	144	RFU	192	CB5	240	DQ37	288	V_{PP}

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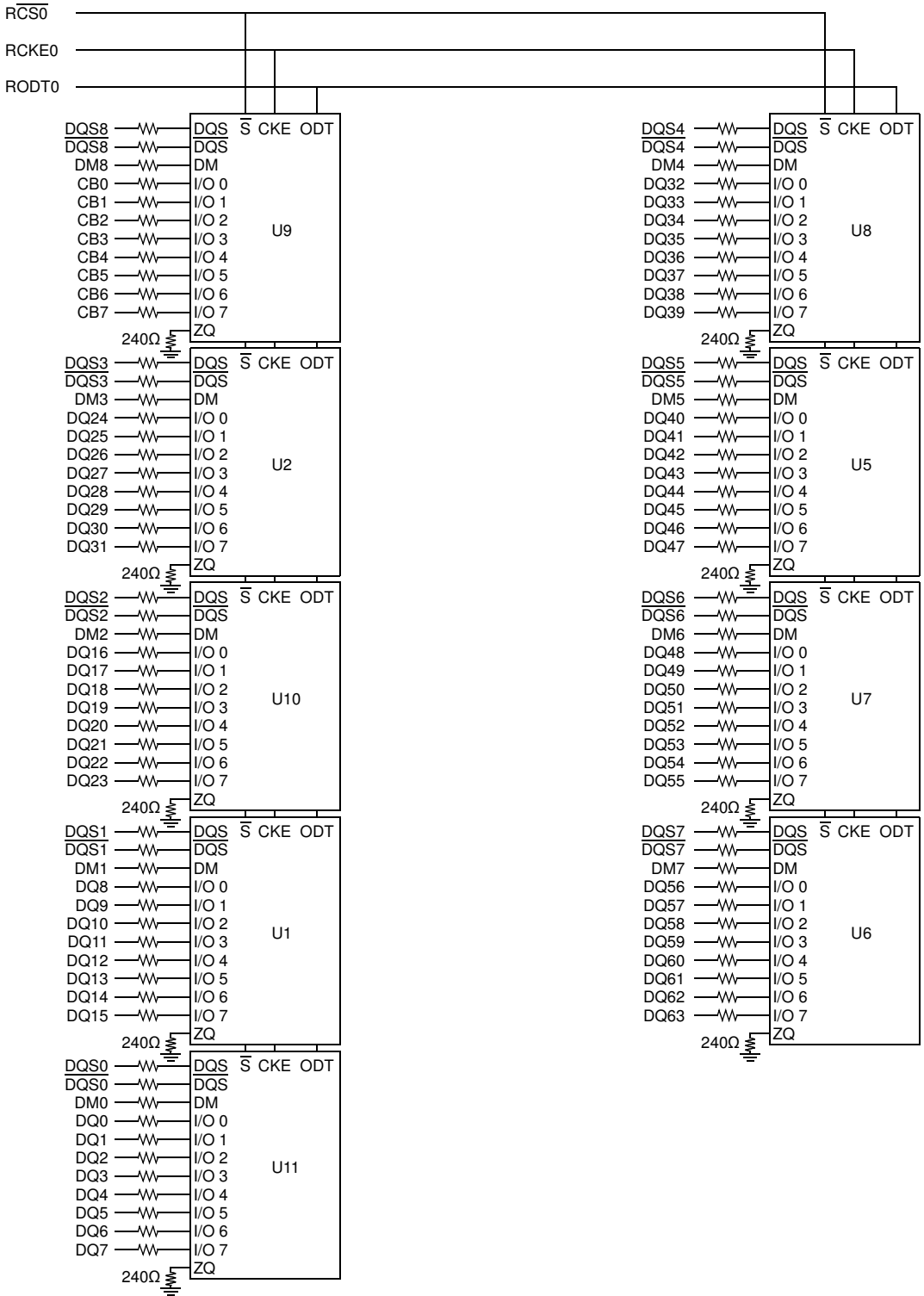
Block Diagram



Note: Unless otherwise noted, data resistor values are 15Ω ± 5%.

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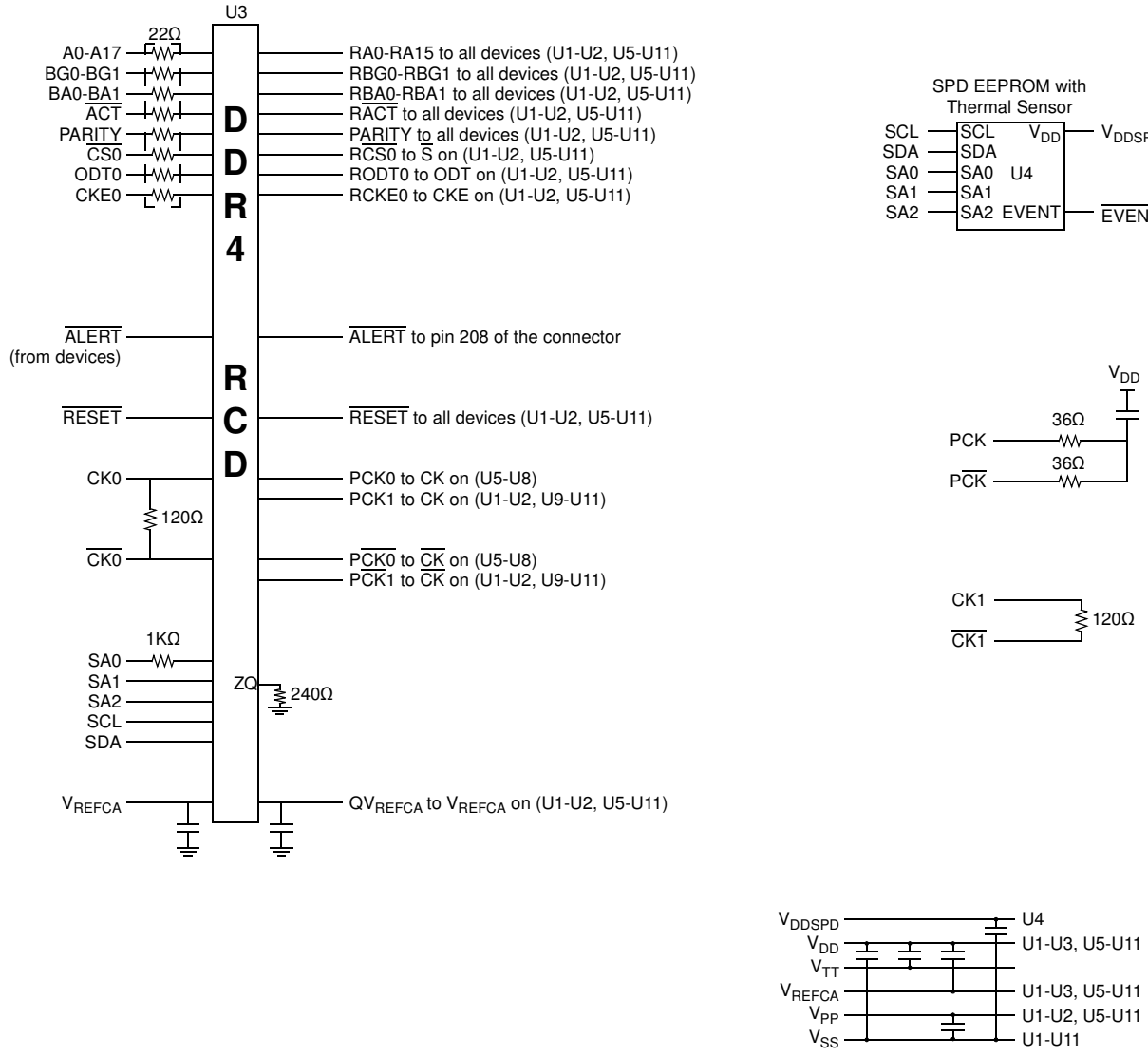
Block Diagram (Continued)



Notes:

1. Each address, command and control signal output line from the register is terminated through a 36Ω series resistor to V_{TT}.
2. Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 9.

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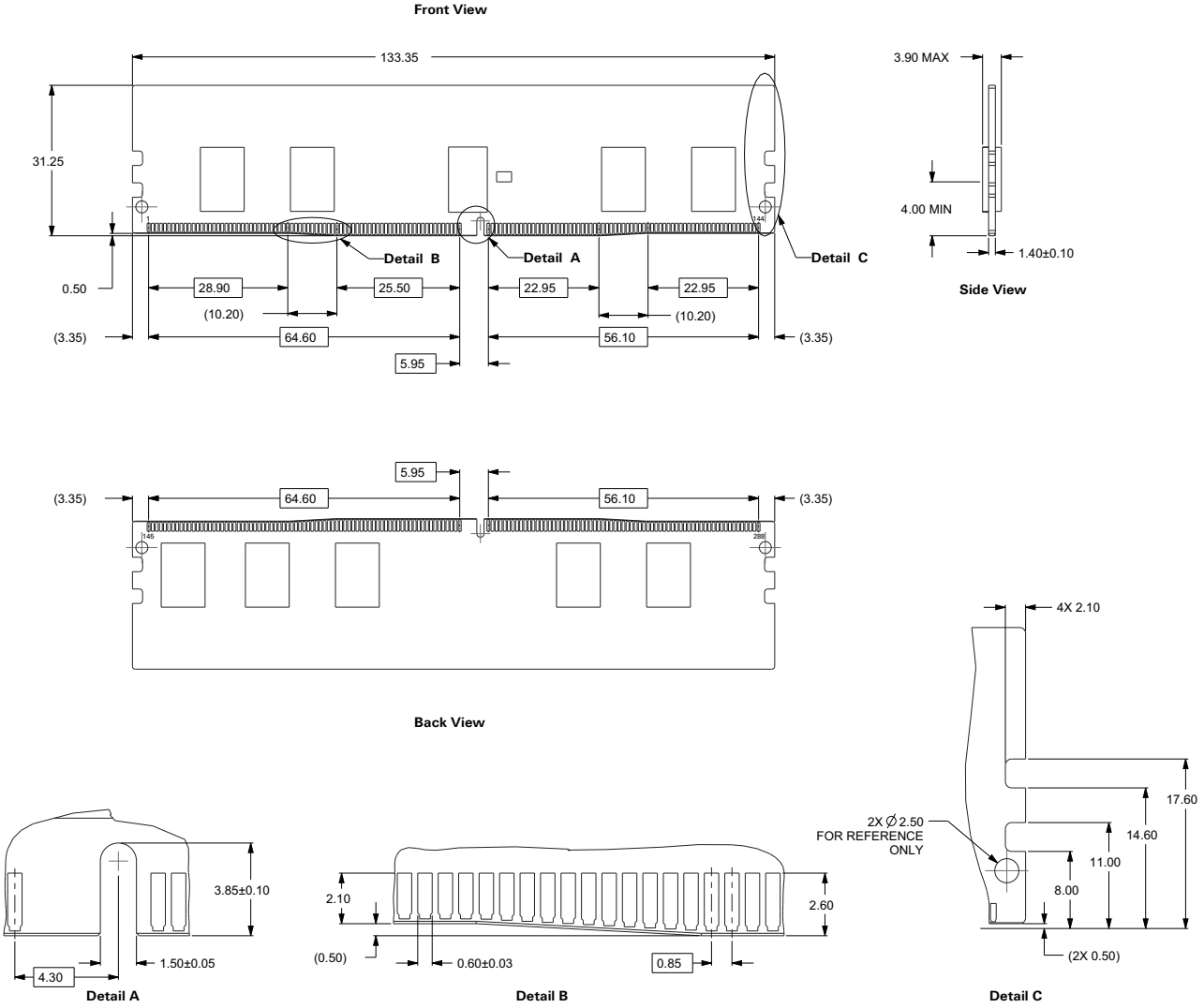
Physical Dimensions

288-Pin Registered DIMM Module



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

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Control Words Programming

DDR4 registered modules (RDIMM) use a JEDEC standard registering clock driver device (RCD). This device features a set of control words that allows the device to be optimized for different RDIMM and motherboard designs. The recommended control word settings for each RDIMM design are programmed in the SPD from bytes 137-138. The control word values from the SPD must be programmed into the registering clock driver to ensure proper operation. This control word programming should be performed prior to the Mode Register programming.

The address & control parity must be generated correctly during the control word programming, otherwise the programming values will be ignored and the registering clock driver will maintain all zero default values. The $\overline{\text{ALERT}}$ signal from the RDIMM should be monitored during control word programming to ensure that the programming is successful.

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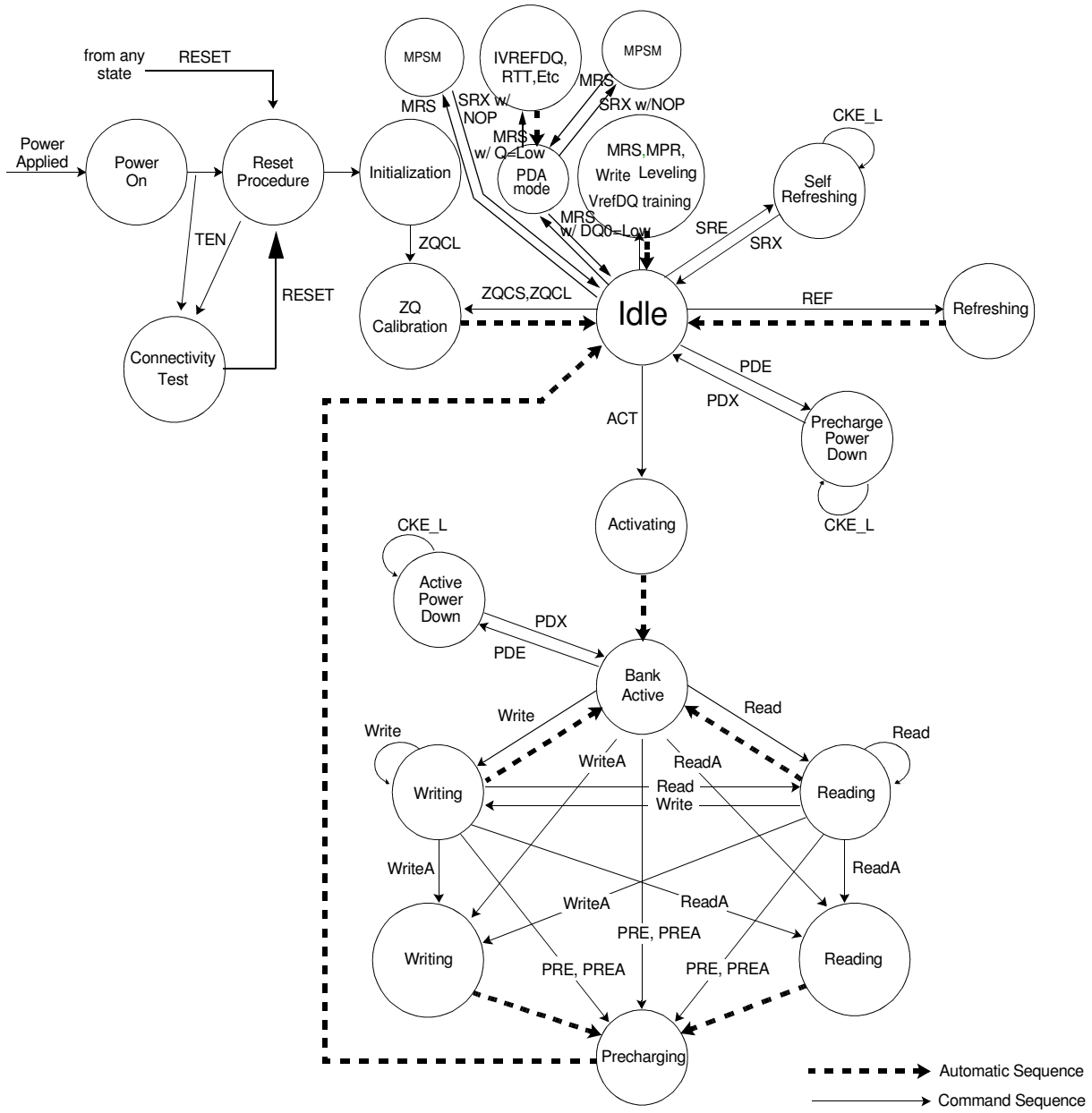
State Diagram



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Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD, RDS4, RDS8	PDE	Enter Power-Down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Enter Power-Down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh Entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh Exit
REF	Refresh, Fine Granularity Refresh	$\overline{\text{RESET}}$	Start $\overline{\text{RESET}}$ Procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

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Mode Registers

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13, A11-A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto-precharge (See Write Recovery and Read to Precharge (cycles) table)
A8	DLL Reset	0 = No 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6-A4, A2	$\overline{CAS}$ Latency[4]	(See $\overline{CAS}$ Latency table)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1-A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for auto-precharge)min in clock cycles is calculated following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given $\overline{CAS}$ Latency. For actual supported $\overline{CAS}$ Latencies, please refer to the Speed Bin tables.
5. A13 for WR and RTP setting is optional for 4Gb.

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Write Recovery and Read to Precharge (Cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

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$\overline{\text{CAS}}$ Latency

A12	A11	A10	A9	WR	$\overline{\text{CAS}}$ Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27
1	0	0	1	1	28
1	0	1	0	0	Reserved for 29
1	0	1	0	1	30
1	0	1	1	0	Reserved for 29
1	0	1	1	1	32
1	1	0	0	0	Reserved

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MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff[2]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10-A8	RTT_NOM	(See RTT_NOM table)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6-A5	RFU	0 = must be programmed to 0 during MRS
A4-A3	Additive Latency	00 = 0 (AL disabled) 01 = CL - 1 10 = CL - 2 11 = Reserved
A2-A1	Output Driver Impedance Control	(See Output Driver Impedance Control table)
A0	DLL Enable	0 = Disable[3] 1 = Enable

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. Outputs disabled - DQs, DQSs, $\overline{\text{DQS}}$s.
3. States reversed to "0 as Disable" with respect to DDR4.

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RTT_NOM

A11	A10	A9	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

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MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
	RFU	0 = must be programmed to 0 during MRS
A11-A9	RTT_WR	(See RTT_WR table)
A8, A2	RFU	0 = must be programmed to 0 during MRS
A7-A6	Low Power Auto Self-Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self-Refresh)
A5-A3	$\overline{CAS}$ Write Latency (CWL)	(See $\overline{CAS}$ Write Latency table)
A1-A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

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RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CWL ($\overline{\text{CAS}}$ Write Latency)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 t_{CK} Write Preamble		Speed Grade in MT/s for 2 t_{CK} Write Preamble	
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	3200	2400	2666	2400
1	1	0	18		2666	3200	2666
1	1	1	20		3200		3200

Notes:

1. The 2 t_{CK} Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 t_{CK} Write Preamble, no additional CWL is needed.

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MR3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12-A11	MPR Read Format	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved Temperature
A10-A9	Write CMD Latency when CRC and DM are enabled	(See Write Command Latency when CRC and DM are both Enabled table)
A8-A6	Fine Granularity Refresh Mode	(See Fine Granularity Refresh Mode table)
A5	Temperature Sensor Readout	0 = Disabled 1 = Enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1-A0	MPR Page Selection	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved Temperature (See MPR Data Format section)

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

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Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

Write Command Latency when CRC and DM are both Enabled

A10	A9	CRC + DM Write Command Latency	Speed Bin (in MT/s)
0	0	4 nCK	1600
0	0	5 nCK	1866, 2133, 2400
0	1	6 nCK	TBD
0	1	RFU	RFU

MPR Data Format

MPR page 0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page 1 (C/A Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-Only
	01 = MPR1	$\overline{CAS}$/ A15	$\overline{WE}$/A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	$\overline{ACT}$	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	$\overline{RAS}$/ A16	
	11 = MPR3	CRC Error Status	C/A Parity Error Status	C/A Parity Latency[4]			C[2]	C[1]	C[0]	
				MR5. A[2]	MR5. A[1]	MR5. A[0]				

Notes:
1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3.
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.
4. MPR3 bit 0~2 (C/A parity latency) reflects the latest programmed C/A parity latency values.

MPR page 2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	PPR	sPPR	RTT_WR	Temperature Sensor Status (See table below)		CRC Write Enable	RTT_WR		Read-Only
		-	-	MR2	-	-	MR2	MR2		
		-	-	A11	-	-	A12	A10	A9	
	01 = MPR1	V_{REF} DQ Training Range	V_{REF} DQ Training Value						Gear-down Enable	
		MR6	MR6						MR3	
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	$\overline{CAS}$ Latency				RFU	$\overline{CAS}$ Write Latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	RTT_NOM			RTT_PARK			Driver Impedance		
		MR1			MR5			MR2		
		A10	A9	A6	A8	A7	A6	A2	A1	

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MR bit for Temperature

MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X Refresh (> t_{REFI})
0	1	1X Refresh Rate (= t_{REFI})
1	0	2X Refresh Rate (1/2 * t_{REFI})
1	1	Reserved

MPR page 3 (Vendor Use Only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Read-Only
	01 = MPR1	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	
	10 = MPR2	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	
	11 = MPR3	Don't Care	Don't Care	Don't Care	Don't Care	MAC	MAC	MAC	MAC	

Notes:

1. MPR page 3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	PPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self-Refresh Abort	0 = Disable 1 = Enable
A8-A6	$\overline{CS}$ to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 100 = 6 101 = 8 110 = Reserved 111 = Reserved (See $\overline{CS}$ to CMD/ADDR Latency Mode Setting table)
A5	sPPR	0 = Disable 1 = Enable
A4	Internal V_{REF} Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

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$\overline{CS}$ to CMD/ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

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MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	C/A Parity Persistent Error	0 = Disable 1 = Enable
A8-A6	RTT_PARK	(See RTT_PARK table)
A5	ODT Input Buffer during Power Down Mode	0 = ODT Input Buffer is activated 1 = ODT Input Buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2-A0	C/A Parity Latency Mode	(See C/A Parity Latency Mode table)

Notes:
1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

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RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A5	A4	A3	PL	Speed Bin (in MT/s)
0	0	0	Disable	
0	0	1	4	1600, 1866, 2133
0	1	0	5	2400
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Notes:

1. Parity latency must be programmed according to the timing parameters in the speed grade table.

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MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12-A10	t_{CCD_L}	(See t_{CCD_L} table)
A9-A8	RFU	0 = must be programmed to 0 during MRS
A7	V_{REFDQ} Training Enable	0 = Disable (Normal Operation Mode) 1 = Enable (Training Mode)
A6	V_{REFDQ} Training Range	(See V_{REFDQ} Training: Range table)
A5-A0	V_{REFDQ} Training Value	(See V_{REFDQ} Training: Values table)

Notes:
1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

t_{CCD_L} & t_{DLLK}

A12	A11	A10	t_{CCD_L}min (nCK)[1]	t_{DLLK}min (nCK)[1]	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps< Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps< Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	≤ TBD
1	0	0	8		≤ TBD
1	0	1	Reserved		
1	1	0			
1	1	1			

Notes:
1. t_{CCD_L}/t_{DLLK} should be programmed according to the value defined in AC parameter table per operating frequency.

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V_{REFDQ} Training: Range

A6	V_{REFDQ} Range
0	Range 1
1	Range 1

V_{REFDQ} Training: Values

A5-A0	Range 1	Range 2		A5-A0	Range 1	Range 2
00 0000	60.00%	45.00%		01 1010	76.90%	61.90%
00 0001	60.65%	45.65%		01 1011	77.55%	62.55%
00 0010	61.30%	46.30%		01 1100	78.20%	63.20%
00 0011	61.95%	46.95%		01 1101	78.85%	63.85%
00 0100	62.60%	47.60%		01 1110	79.50%	64.50%
00 0101	63.25%	48.25%		01 1111	80.15%	65.15%
00 0110	63.90%	48.90%		10 0000	80.80%	65.80%
00 0111	64.55%	49.55%		10 0001	81.45%	66.45%
00 1000	65.20%	50.20%		10 0010	82.10%	67.10%
00 1001	65.85%	50.85%		10 0011	82.75%	67.75%
00 1010	66.50%	51.50%		10 0100	83.40%	68.40%
00 1011	67.15%	52.15%		10 0101	84.05%	69.05%
00 1100	67.80%	52.80%		10 0110	84.70%	69.70%
00 1101	68.45%	53.45%		10 0111	85.35%	70.35%
00 1110	69.10%	54.10%		10 1000	86.00%	71.00%
00 1111	69.75%	54.75%		10 1001	86.65%	71.65%
01 0000	70.40%	55.40%		10 1010	87.30%	72.30%
01 0001	71.05%	56.05%		10 1011	87.95%	72.95%
01 0010	71.70%	56.70%		10 1100	88.60%	73.60%
01 0011	72.35%	57.35%		10 1101	89.25%	74.25%
01 0100	73.00%	58.00%		10 1110	89.90%	74.90%
01 0101	73.65%	58.65%		10 1111	90.55%	75.55%
01 0110	74.30%	59.30%		11 0000	91.20%	76.20%
01 0111	74.95%	59.95%		11 0001	91.85%	76.85%
01 1000	75.60%	60.60%		11 0010	92.50%	77.50%
01 1001	76.25%	61.25%		11 0011 to 11 1111	Reserved	Reserved

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Truth Tables

Command Truth Table

a. Notes 1-4 apply to the entire Command Truth Table.
b. Note 5 applies to all Read/Write command.
[BG= Bank Group Address, BA= Bank Address, RA= Row Address, CA = Column Address, $\overline{BC}$ = Burst chop, X = Don't care, V = Valid]

Command Truth Table

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/ A16	$\overline{CAS}$/ A15	$\overline{WE}$/ A14	BG0-BG1	BA0-BA1	C2-C0	A12 /$\overline{BC}$	A17, A13, A11	A10 /AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self-Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7, 9
Self-Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7, 8, 9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Pre-charge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge All Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	

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Command Truth Table

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	BG0-BG1	BA0-BA1	C2-C0	A12/$\overline{BC}$	A17, A13, A11	A10/AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power-Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power-Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ Calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ Calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

Notes:

1. All DDR4 SDRAM commands are defined by states of $\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When $\overline{ACT}$ = H; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as command pins $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ respectively. When $\overline{ACT}$ = L; pins $\overline{RAS}$/A16, $\overline{CAS}$/A15, and $\overline{WE}$/A14 are used as address pins A16, A15, and A14 respectively
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
8. Controller guarantees Self-Refresh exit to be synchronous.
9. V_{PP} and $V_{REF}(V_{REFCA})$ must be maintained during Self-Refresh operation.
10. The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit
11. Refer to the CKE Truth Table for more detail with CKE transition.
12. During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

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CKE Truth Table

Current State[2]	CKE		Command (N)[3]	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$		
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	DESELECT	Self-Refresh Exit	8, 12, 16
Bank(s) Activate	H	L	DESELECT	Active Power-Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power-Down Entry	11, 13, 14, 18
	H	L	REFRESH	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on page 32.					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to t_{CKE}min being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are DESELECT only.
12. Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.
13. Self-Refresh can not be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. V_{PP} and V_{REFCA} must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, etc.)

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Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as t_{CKAVG}min are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like t_{AA}min, t_{RCD}min, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

  nCK = ceiling [(parameter_in_ns / application_t_{CK}_in_ns) - 0.025]

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

  nCK = truncate [{(parameter_in_ps x 1000) / (application_t_{CK}_in_ps) + 974} / 1000]

- Either algorithm yields identical results.

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Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-0.3 ~ 1.5	V	1, 3
V_{PP}	Voltage on V_{PP} relative to V_{SS}	-0.3 ~ 3.0	V	1, 4
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3 ~ 1.5	V	1
V_{DDSPD}	Voltage on V_{DDSPD} relative to V_{SS}	-0.5 ~ 4.3	V	1
T_{STG}	Storage Temperature	-55 to +100	℃	1, 2

Notes:
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{REF} must be not greater than 0.6 * V_{DD}. When V_{DD} is less than 500 mV, V_{REF} may be less than or equal to 300 mV.
4. V_{PP} must be equal or greater than V_{DD} at all times.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min	Typical	Max		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1, 2
V_{PP}	Supply Voltage for Output	2.375	2.5	2.75	V	1
V_{DDSPD}	SPD Supply Voltage	2.25	2.5	2.75	V	
V_{TT}	Termination Voltage	0.57	0.6	0.63	V	2
V_{SS}	Ground	0	0	0	V	

Notes:
1. DC bandwidth is limited to 20MHz.
2. $V_{TT} = V_{DD}/2$.

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Operating Temperature Range

Symbol	Parameter	Range	Units	Notes
T_{OPER}	Industrial Operating Temperature Range (Case)	-40 to 85	℃	1, 2
	Extended Operating Temperature Range (Case)	85 to 95	℃	1, 3

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
2. The Industrial Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40 ℃ and 85 ℃ under all operating conditions.
3. Some applications require operation in the Extended Temperature Range between 85 ℃ and 95 ℃. Full specifications are supported in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the Extended Temperature Range. Please refer to the SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and Extended Temperature Range. Please refer to the DIMM SPD for t_{REFI} requirements in the Extended Temperature Range.

Temperature Sensor Characteristics

Symbol	Test Condition[2]	Min	Typical	Max	Units
JEDEC B-Grade	+75 ℃ ≤ T_A ≤ +95 ℃, Active Range	-	±0.5	±1	℃
	+40 ℃ ≤ T_A ≤ +125 ℃, Monitor Range	-	±1	±2	℃
	-40 ℃ ≤ T_A ≤ +125 ℃	-	±2	±3	℃
Resolution		-	0.25	-	℃
Conversion Time[1]	Worst Case Conversion Time	-	-	120	ms

Notes:

1. Assuming 10-bit resolution. Conversion times may range from 62.5 ms for 9-bit to 500 ms for 12-bit accuracy.
2. $V_{DDSPD}min \leq V_{DDSPD} \leq V_{DDSPD}max$

Refresh Parameters

Parameter		Symbol	8Gb	Units
Average periodic refresh interval	-40 ℃ ≤ T_{CASE} ≤ 85 ℃	t_{REFI}	7.8	µs
	85 ℃ ≤ T_{CASE} ≤ 95 ℃		3.9	µs

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Differential AC and DC Input Levels for CK-$\overline{CK}$

Symbol	Parameter	DDR4-2666		Units	Notes
		Min	Max		
V_{IHDIFF}	Differential input logic high	0.150	Note 3	V	1
V_{ILDIFF}	Differential input logic high	Note 3	-0.150	V	1
V_{IHDIFF}(AC)	AC input logic high	2 * (V_{IH}(AC) - V_{REF})	Note 3	V	2
V_{ILDIFF}(AC)	AC input logic low	Note 3	2 * (V_{IL}(AC) - V_{REF})	V	2

Notes:
1. Used to define a differential signal slew-rate.
2. For CK/$\overline{CK}$, use V_{IH}/V_{IL}(AC) of ADD/CMD and V_{REFCA}.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-Ended Levels for CK, $\overline{CK}$

Symbol	Parameter	DDR4-2666		Units	Notes
		Min	Max		
V_{SEH}	Single-ended high-level for CK, $\overline{CK}$	(V_{DD}/2) + 0.100	Note 3	V	1, 2
V_{SEL}	Single-ended low-level for CK, $\overline{CK}$	Note 3	(V_{DD}/2) - 0.100	V	1, 2

Notes:
1. For CK-$\overline{CK}$, use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD.
2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA}.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC) min) for single-ended signals as well as the limitations for overshoot and undershoot.

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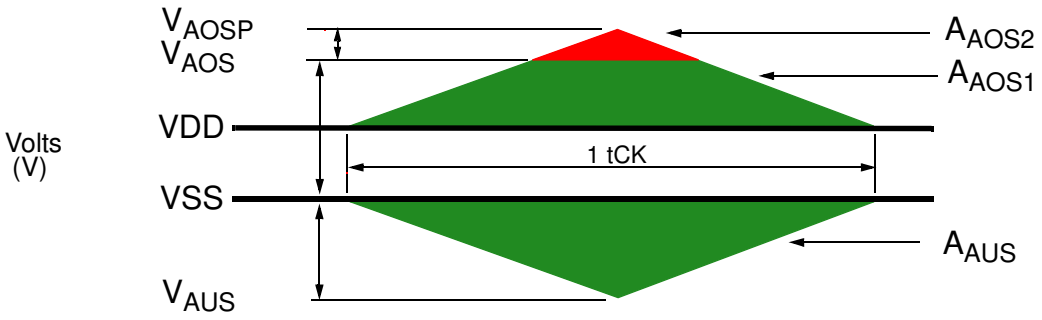
AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	Symbol	DDR4-2666	Units	Notes
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06	V	
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	V_{DD} +0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{AUS}	0.30	V	
Maximum overshoot area per 1 t_{CK} above V_{AOS}	A_{AOS2}	0.0062	V-ns	
Maximum overshoot area per 1 t_{CK} between V_{DD} and V_{AOS}	A_{AOS1}	0.1914	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{AUS}	0.1984	V-ns	
(A0-A13, A17, BG0-BG1, BA0-BA1, $\overline{ACT}$, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{CS}$, CKE, ODT, C0-C2)				

Notes:

1. The value of V_{AOS} matches V_{DD} absolute max as defined in the Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{AOS} remains at V_{DD} absolute max as defined in the Absolute Maximum DC Ratings.



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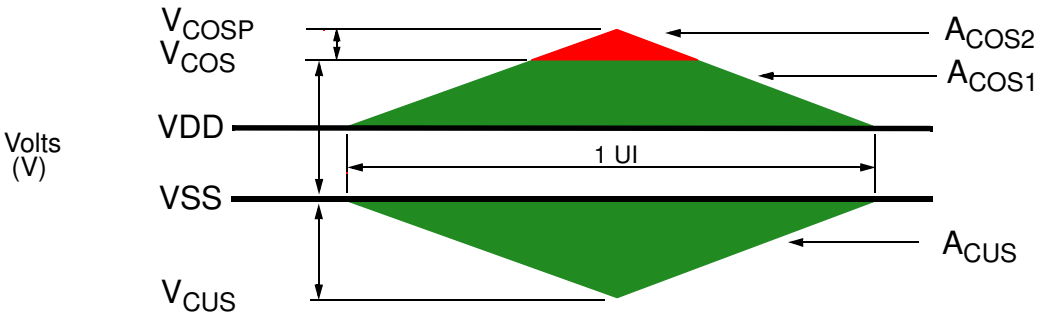
AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	DDR4-2666	Units	Notes
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06	V	
Upper boundary of overshoot area A_{COS1}	V_{COS}	V_{DD} +0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30	V	
Maximum overshoot area per 1 UI above V_{COS}	A_{COS2}	0.0028	V-ns	
Maximum overshoot area per 1 UI between V_{DD} and V_{COS}	A_{COS1}	0.0844	V-ns	
Maximum undershoot area per 1 UI below V_{SS}	A_{CUS}	0.0858	V-ns	
(CK, $\overline{CK}$)				

Notes:

1. The value of V_{COS} matches V_{DD} absolute max as defined in the Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{COS} remains at V_{DD} absolute max as defined in the Absolute Maximum DC Ratings.



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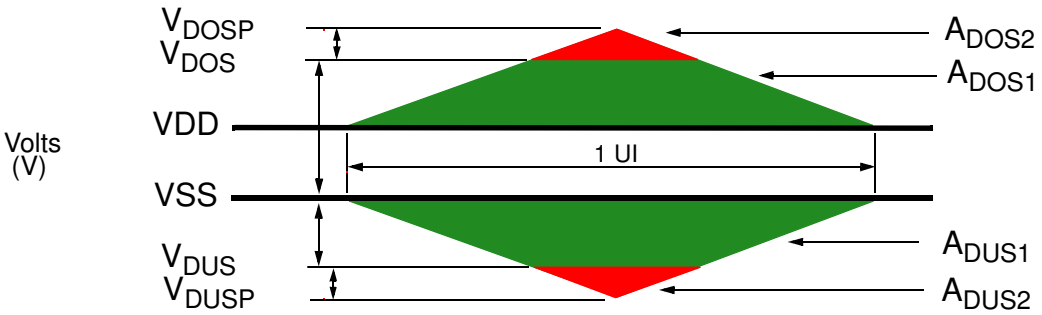
AC Overshoot/Undershoot Specification for Data, Strobe and Mask

Parameter	Symbol	DDR4-2666	Units	Notes
Maximum peak amplitude above V_{AOS}	V_{DOSP}	0.16	V	
Upper boundary of overshoot area A_{AOS1}	V_{DOS}	V_{DD} +0.24	V	1
Maximum peak amplitude allowed for undershoot	V_{DUS}	0.30	V	2
Maximum peak amplitude allowed for undershoot	V_{DUSP}	0.10	V	
Maximum overshoot area per 1 t_{CK} above V_{AOS}	A_{DOS2}	0.0113	V-ns	
Maximum overshoot area per 1 t_{CK} between V_{DD} and V_{AOS}	A_{DOS1}	0.0788	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{DUS1}	0.0788	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{DUS2}	0.0113	V-ns	
(DQ, CB, DQS, $\overline{DQS}$, $\overline{DM}$, $\overline{DBI}$, TDQS, $\overline{TDQS}$)				

Notes:

1. The value of V_{DOS} matches (V_{IN}, V_{OUT}) max as defined in the Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in the Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{DOS} remains at (V_{IN}, V_{OUT}) max as defined in the Absolute Maximum DC Ratings.
2. The value of V_{DUS} matches (V_{IN}, V_{OUT}) min as defined in the Absolute Maximum DC Ratings.



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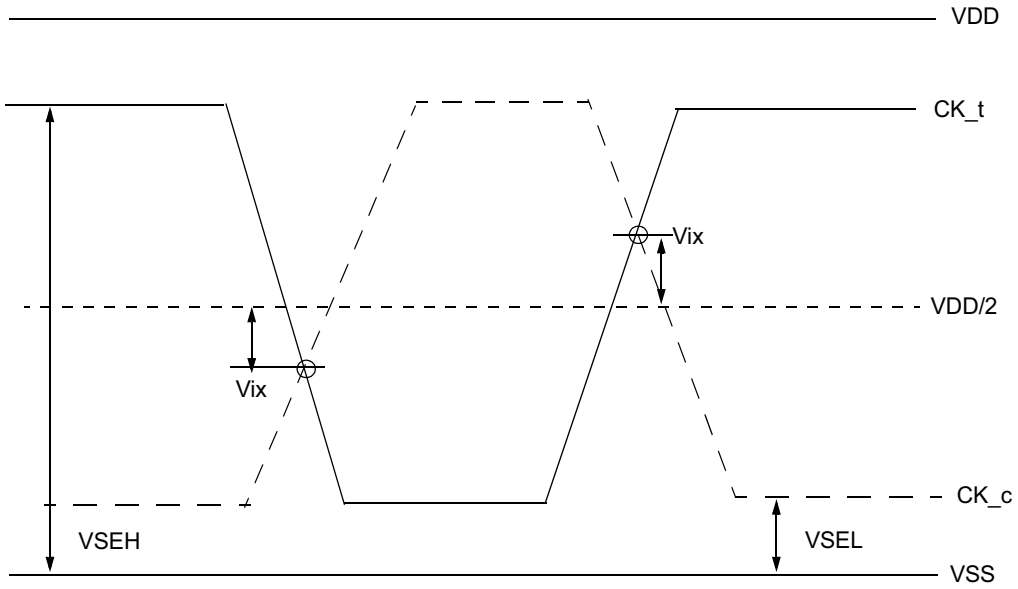
Cross Point Voltage for Differential Input Signals (CK-$\overline{CK}$)

Symbol	Parameter	DDR4-2666			
		Min		Max	
	Area of V_{SEH}, V_{SEL}	$V_{SEL} \leq V_{DD}/2 - 145$ mV	$V_{DD}/2 - 145$ mV $\leq V_{SEL} \leq V_{DD}/2 - 100$ mV	$V_{DD}/2 + 145$ mV $\leq V_{SEL} \leq V_{DD}/2 - 145$ mV	$V_{DD}/2 + 145$ mV $\leq V_{SEH}$
V_{IX}(CK)	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, $\overline{CK}$	-120 mV	- ($V_{DD}/2 - V_{SEL}$) + 25 mV	- ($V_{SEH} - V_{DD}/2$) - 25 mV	120 mV



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Single-Ended AC & DC Output Levels

Symbol	Parameter	DDR4-2666	Units	Notes
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 * V_{DD}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 * V_{DD}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 * V_{DD}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) * V_{DD}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) * V_{DD}	V	1

Notes:

1. The swing of ± 0.15 * V_{DD} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DD}.

Differential AC & DC Output Levels

Symbol	Parameter	DDR4-2666	Units	Notes
		Min		
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	0.3 * V_{DD}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 * V_{DD}	V	1

Notes:

1. The swing of ± 0.3 * V_{DD} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DD} at each of the differential outputs.

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Device Standard Speed Bins

DDR4-2666 Speed Bins

Speed Bin				DDR4-2666		Units	Notes
CL - nRCD - nRP				19-19-19			
Parameter			Symbol	Min	Max		
Internal read command to first data			t_{AA}	13.5	18	ns	7
Internal read command to first data with read DBI enabled			t_{AA_DBI}	t_{AA}(min) + 3nCK	t_{AA}(max) + 3nCK	ns	7
ACT to internal read or write delay time			t_{RCD}	13.5	-	ns	7
PRE command period			t_{RP}	13.5	-	ns	7
ACT to ACT or REF command period			t_{RC}	46.5	-	ns	7
ACT to PRE command period			t_{RAS}	33	9 * t_{REFI}	ns	7
	Normal	Read DBI	$t_{CK(avg)}$				
CWL = 9	CL = 9	CL = 11	$t_{CK(avg)}$	1.5	1.6	ns	1, 2, 3, 5, 6, 8
	CL = 10	CL = 12		Reserved		ns	4
CWL = 9, 11	CL = 11	CL = 13	$t_{CK(avg)}$	Reserved		ns	4
	CL = 12	CL = 14		1.25	< 1.5	ns	1, 2, 3, 5
CWL = 10, 12	CL = 13	CL = 15	$t_{CK(avg)}$	1.071	< 1.25	ns	1, 2, 3, 5
	CL = 14	CL = 16		1.071	< 1.25	ns	1, 2, 3, 5
CWL = 11, 14	CL = 14	CL = TBD	$t_{CK(avg)}$	Reserved		ns	4
	CL = 15	CL = TBD		0.75	< 1.071	ns	1, 2, 3
	CL = 14	CL = TBD		0.75	< 1.071	ns	1, 2, 3
Supported CL Settings				10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20		n_{CK}	
Supported CL Settings with read DBI				12, 13, 14, 15, 17, 18, 19, 20, 21, 22, 23		n_{CK}	
Supported CWL Settings				9, 10, 11, 12, 14, 16,18		n_{CK}	

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Speed Bin Tables Notes

Absolute Specification
- V_{DD} = 1.20V +/- 0.06 V
- V_{PP} = 2.5V +0.25/-0.125 V
- The values defined with the above mentioned table are the case where DLL ON.
- DDR4-2133 Speed Bin Table is valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in $t_{CK(avg)}$min and $t_{CK(avg)}$max requirements. When making a selection of $t_{CK(avg)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(avg)}$min limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from t_{AA} following Rounding Algorithm section
3. $t_{CK(avg)}$max limits: Calculate $t_{CK(avg)} = t_{AA}$max / CL SELECTED and round the resulting $t_{CK(avg)}$ down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns). This result is $t_{CK(avg)}$max corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
7. Parameters apply from $t_{CK(avg)}$min to $t_{CK(avg)}$max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
8. DDR4 SDRAM supports CL = 9 as long as a system meets t_{AA}(min).

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Device Timing Parameters by Speed Bin

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	20	ns	
Average Clock Period	$t_{CK(avg)}$	0.938	<1.071	ns	35, 36
Average HIGH Pulse Width	$t_{CH(avg)}$	0.48	0.52	$t_{CK(avg)}$	
Average LOW Pulse Width	$t_{CL(avg)}$	0.48	0.52	$t_{CK(avg)}$	
Absolute Clock Period	$t_{CK(abs)}$	$t_{CK(avg)}$min + $t_{JIT(per)_tot}$min	$t_{CK(avg)}$max + $t_{JIT(per)_tot}$max	$t_{CK(avg)}$	
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	0.45	-	$t_{CK(avg)}$	23
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	0.45	-	$t_{CK(avg)}$	24
Clock Period Jitter - Total	$t_{JIT(per)\_tot}$	-47	47	ps	25
Clock Period Jitter - Deterministic	$t_{JIT(per)\_dj}$	-23	23	ps	26
Clock Period Jitter during DLL Locking Period	$t_{JIT(per, lck)}$	-38	38	ps	
Cycle to Cycle Period Jitter	$t_{JIT(CC)}$	-	94	ps	
Cycle to Cycle Period Jitter during DLL Locking Period	$t_{JIT(CC, lck)}$	-	75	ps	
Duty Cycle Jitter	$t_{JIT(duty)}$	TBD	TBD	ps	
Cumulative Error across 2 Cycles	$t_{ERR(2per)}$	-69	69	ps	
Cumulative Error across 3 Cycles	$t_{ERR(3per)}$	-82	82	ps	
Cumulative Error across 4 Cycles	$t_{ERR(4per)}$	-91	91	ps	
Cumulative Error across 5 Cycles	$t_{ERR(5per)}$	-98	98	ps	
Cumulative Error across 6 Cycles	$t_{ERR(6per)}$	-104	104	ps	
Cumulative Error across 7 Cycles	$t_{ERR(7per)}$	-109	109	ps	
Cumulative Error across 8 Cycles	$t_{ERR(8per)}$	-113	113	ps	
Cumulative Error across 9 Cycles	$t_{ERR(9per)}$	-117	117	ps	
Cumulative Error across 10 Cycles	$t_{ERR(10per)}$	-120	120	ps	
Cumulative Error across 11 Cycles	$t_{ERR(11per)}$	-123	123	ps	
Cumulative Error across 12 Cycles	$t_{ERR(12per)}$	-126	126	ps	
Cumulative Error across 13 Cycles	$t_{ERR(13per)}$	-129	129	ps	
Cumulative Error across 14 Cycles	$t_{ERR(14per)}$	-131	131	ps	
Cumulative Error across 15 Cycles	$t_{ERR(15per)}$	-133	133	ps	
Cumulative Error across 16 Cycles	$t_{ERR(16per)}$	-135	135	ps	
Cumulative Error across 17 Cycles	$t_{ERR(17per)}$	-137	137	ps	

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Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Cumulative Error across 18 Cycles	$t_{ERR(18per)}$	-139	139	ps	
Cumulative Error across n = 19-50 Cycles	$t_{ERR(nper)}$	((1 + 0.68ln(n)) * $t_{JIT(per)_tot}$min)	((1 + 0.68ln(n)) * $t_{JIT(per)_tot}$max)	ps	
Command and Address Setup Time to CK, $\overline{CK}$ Referenced to V_{IH}(AC) / V_{IL}(AC) Levels	$t_{IS(base)}$	80	-	ps	
Command and Address Setup Time to CK, $\overline{CK}$ Referenced to V_{REF} Levels	$t_{IS(Vref)}$	180	-	ps	
Command and Address Hold Time to CK, $\overline{CK}$ Referenced to V_{IH}(DC) / V_{IL}(DC) Levels	$t_{IH(base)}$	105	-	ps	
Command and Address Hold Time to CK, $\overline{CK}$ Referenced to V_{REF} Levels	$t_{IH(Vref)}$	180	-	ps	
Control and Address Input Pulse Width for Each Input	t_{IPW}	460	-	ps	
Command and Address Timing					
$\overline{CAS}$ to $\overline{CAS}$ Command Delay for Same Bank Group	t_{CCD_L}	Max(5nCK, 5.355ns)	-	nCK	34
$\overline{CAS}$ to $\overline{CAS}$ Command Delay for Different Bank Group	t_{CCD_S}	4	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 2 KB Page Size	$t_{RRD\_S(2K)}$	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 1 KB Page Size	$t_{RRD\_S(1K)}$	Max(4nCK, 3.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 1/2 KB Page Size	$t_{RRD\_S(1/2K)}$	Max(4nCK, 3.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 2 KB Page Size	$t_{RRD\_L(2K)}$	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 1 KB Page Size	$t_{RRD\_L(1K)}$	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 1/2 KB Page Size	$t_{RRD\_L(1/2K)}$	Max(4nCK, 5.3ns)	-	nCK	34
Four Activate Window for 2 KB Page Size	$t_{FAW(2K)}$	Max(28nCK, 30ns)	-	ns	34
Four Activate Window for 1 KB Page Size	$t_{FAW(1K)}$	Max(20nCK, 21ns)	-	ns	34
Four Activate Window for 1/2 KB Page Size	$t_{FAW(1/2K)}$	Max(16nCK, 15ns)	-	ns	34
Delay from Start of Internal Write Transaction to Internal READ Command for Same Bank Group	t_{WTR_S}	Max(2nCK, 2.5ns)	-	ns	1, 2, 34
Delay from Start of Internal Write Transaction to Internal READ Command for Different Bank Group	t_{WTR_L}	Max(4nCK, 7.5ns)	-	ns	1, 34

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Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Internal READ Command to PRECHARGE Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns	34
WRITE Recovery Time	t_{WR}	15	-	ns	1
WRITE Recovery Time when Both CRC and DM are Enabled	$t_{WR\_CRC\_DM}$	t_{WR} + Max(5nCK, 3.75ns)	-	ns	1, 28
Delay from Start of Internal Write Transaction to Internal READ Command for Same Bank Group when Both CRC and DM are Enabled	$t_{WTR\_S\_CRC\_DM}$	t_{WTR_S} + Max(5nCK, 3.75ns)	-	ns	2, 29, 34
Delay from Start of Internal Write Transaction to Internal READ Command for Different Bank Group when Both CRC and DM are Enabled	$t_{WTR\_L\_CRC\_DM}$	t_{WTR_L} + Max(5NCK, 3.75ns)	-	ns	3, 30, 34
DLL locking time	t_{DLLK}	768	-	nCK	
Mode Register Set Command Cycle Time	t_{MRD}	8	-	nCK	
Mode Register Set Command Update Delay	t_{MOD}	Max(24nCK, 15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	t_{WR_MPR}	t_{MOD}min + AL + PL	-	nCK	
Auto Precharge Write Recovery Time + Precharge Time	t_{DAL}	Programmed WR + roundup (t_{RP} / $t_{CK(avg)}$)	-	nCK	
DQ0 or DQL0 Driven to 0 Setup Time to First DQS Rising Edge	t_{PDA_S}	0.5	-	UI	45, 47
DQ0 or DQL0 Driven to 0 Hold Time from Last DQS Falling Edge	t_{PDA_H}	0.5	-	UI	46, 47
CS to Command Address Latency					
$\overline{CS}$ to Command Address Latency	t_{CAL}	Max(3nCK, 3.748ns)	-	nCK	
Mode Register Set Command Cycle Time in CAL Mode	t_{MRD_tCAL}	t_{MOD} + t_{CAL}	-	nCK	
Mode Register Set Update Delay in CAL Mode	t_{MOD_tCAL}	t_{MOD} + t_{CAL}	-	nCK	
DRAM Data Timing					
DQS, $\overline{DQS}$ to DQ Skew, Per Group, Per Access	t_{DQSQ}	-	0.16	UI	13, 18, 39, 49
DQ Output Hold Time from DQS, $\overline{DQS}$	t_{QH}	0.76	-	UI	13, 17, 18, 39, 49
Data Valid Window per Device per UI: (t_{QH} - t_{DQSQ}) of Each UI on a Given DRAM	t_{DVWd}	0.64	-	UI	17, 18, 39, 49

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Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Data Valid Window per Pin per UI: (t_{QH} - t_{DQSQ}) Each UI on a Pin of a Given DRAM	t_{DVWp}	0.69	-	UI	17, 18, 39, 49
DQS, $\overline{DQS}$ Low-Impedance Time from CK, $\overline{CK}$	$t_{LZ(DQ)}$	-360	180	ps	39
DQS, $\overline{DQS}$ High-Impedance Time from CK, $\overline{CK}$	$t_{HZ(DQS)}$	-	180	ps	39
Data Strobe Timing					
DQS, $\overline{DQS}$ Differential READ Preamble (1 Clock)	t_{RPRE}	0.9	Note 44	t_{CK}	39, 40
DQS, $\overline{DQS}$ Differential READ Preamble (2 Clock)	t_{RPRE2}	N/A	N/A	t_{CK}	39, 41
DQS, $\overline{DQS}$ Differential READ Postamble	t_{RPST}	0.33	Note 45	t_{CK}	39
DQS, $\overline{DQS}$ Differential Output High Time	t_{QSH}	0.4	-	t_{CK}	21, 39
DQS, $\overline{DQS}$ Differential Output Low Time	t_{QSL}	0.4	-	t_{CK}	20, 39
DQS, $\overline{DQS}$ Differential WRITE Preamble (1 Clock)	t_{WPRE}	0.9	-	t_{CK}	42
DQS, $\overline{DQS}$ Differential WRITE Preamble (2 Clock)	t_{WPRE2}	N/A	-	t_{CK}	43
DQS, $\overline{DQS}$ Differential WRITE Postamble	t_{WPST}	0.33	-	t_{CK}	
DQS, $\overline{DQS}$ Low-Impedance Time (Referenced from RL-1)	$t_{LZ(DQS)}$	-360	180	t_{CK}	39
DQS, $\overline{DQS}$ High-Impedance Time (Referenced from RL+BL/2)	$t_{HZ(DQS)}$	-	180	t_{CK}	39
DQS, $\overline{DQS}$ Differential Input Low Pulse Width	t_{DQSL}	0.46	0.54	t_{CK}	
DQS, $\overline{DQS}$ Differential Input High Pulse Width	t_{DQSH}	0.46	0.54	t_{CK}	
DQS, $\overline{DQS}$ Rising Edge to CK, $\overline{CK}$ Rising Edge (1 Clock Preamble)	t_{DQSS}	-0.27	0.27	t_{CK}	42
DQS, $\overline{DQS}$ Rising Edge to CK, $\overline{CK}$ Rising Edge (2 Clock Preamble)	t_{DQSS2}	N/A	N/A	t_{CK}	43
DQS, $\overline{DQS}$ Falling Edge Setup Time from CK, $\overline{CK}$ Rising Edge	t_{DSS}	0.18	-	t_{CK}	
DQS, $\overline{DQS}$ Falling Edge Hold Time from CK, $\overline{CK}$ Rising Edge	t_{DSH}	0.18	-	t_{CK}	
DQS, $\overline{DQS}$ Rising Edge Output Timing Location from Rising CK, $\overline{CK}$ with DLL On Mode	t_{DQSCK} (DLL On)	-180	180	ps	37, 38, 39
DQS, $\overline{DQS}$ Rising Edge Output Variance Window per DRAM	t_{DQSCKI} (DLL On)	-	310	ps	37, 38, 39
MPSM Timing					
Command Path Disable Delay upon MPSM Entry	t_{MPED}	t_{MOD}min + t_{CPDED}min	-		
Valid Clock Requirement after MPSM Entry	t_{CKMPE}	t_{MOD}min + t_{CPDED}min	-		

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Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Valid Clock Requirement before MPSM Exit	t_{CKMPX}	t_{CKSRX}min	-		
Exit MPSM to Commands not Requiring a Locked DLL	t_{XMP}	t_{XS}min	-		
Exit MPSM to Commands Requiring a Locked DLL	t_{XMPDLL}	t_{XMP}min + t_{XSDLL}min	-		
$\overline{CS}$ Setup Time to CKE	t_{MPX_S}	t_{IS}min + t_{IH}min	-		
Calibration Timing					
Power-up and $\overline{RESET}$ Calibration Time	t_{ZQinit}	1024	-	nCK	
Normal Operation Full Calibration Time	t_{ZQoper}	512	-	nCK	
Normal Operation Short Calibration Time	t_{ZQCS}	128	-	nCK	
$\overline{RESET}$/Self-Refresh Timing					
Exit $\overline{RESET}$ from CKE HICH to a Valid Command	t_{XPR}	Max(5nCK, t_{RFC}min + 10ns)	-	nCK	
Exit Self-Refresh to Commands not Requiring a Locked DLL	t_{XS}	t_{RFC}min +10ns	-	nCK	
SRX to Commands not Requiring a Locked DLL in Self-Refresh ABORT	t_{XS_ABORT}	t_{RFC4}min +10ns	-	nCK	
Exit Self-Refresh to ZQCL, ZQCS and MRS (CL, CWL, WL, RTP and Geardown)	t_{XS_FAST}	t_{RFC4}min +10ns	-	nCK	
Exit Self Refresh from to Commands Requiring a Locked DLL	t_{XSDLL}	t_{DLLK}min	-	nCK	
Minimum CKE Low Width for Self-Refresh Entry to Exit Timing	t_{CKESR}	t_{CKE}min + 1nCK	-	nCK	
Minimum CKE Low Width for Self-Refresh Entry to Exit Timing with CA Parity Enabled	t_{CKESR_PAR}	t_{CKE}min + 1nCK + PL	-	nCK	
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max(5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE) when CA Parity us Enabled	t_{CKSRE_PAR}	Max(5nCK, 10ns) + PL	-	nCK	
Valid Clock Requirement before Self-Refresh Exit (SRX) or Power-Down Exit (PDX) or $\overline{RESET}$ Exit	t_{CKSRX}	Max(5nCK, 10ns)	-	nCK	
Power Down Timing					
Exit Power Down with DLL on to any Valid Command; Exit Precharge Power Down with DLL Frozen to Commands not Requiring a Locked DLL	t_{XP}	Max(4nCK, 6ns)	-	nCK	
CKE Minimum Pulse Width	t_{CKE}	Max(3nCK, 5ns)	-	nCK	31, 32
Command Pass Disable Delay	t_{CPDED}	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}min	9 * t_{REFI}	nCK	6

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Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Timing of ACT Command to Power Down Entry	$t_{ACTPDEN}$	2	-	nCK	7
Timing of PRE or PREA Command to Power Down Entry	t_{PRPDEN}	2	-	nCK	7
Timing of RD/RDA Command to Power Down Entry	t_{RDPDEN}	RL + 4 + 1	-	nCK	
Timing of WR Command to Power Down Entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + (t_{WR} / $t_{CK(avg)}$)	-	nCK	4
Timing of WRA Command to Power Down Entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	nCK	5
Timing of WR Command to Power Down Entry (BC4MRS)	$t_{WRPBC4DEN}$	WL + 2 + (t_{WR} / $t_{CK(avg)}$)	-	nCK	4
Timing of WRA Command to Power Down Entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL +2 + WR + 1	-	nCK	5
Timing of REF Command to Power Down Entry	$t_{REFPDEN}$	2	-	nCK	7
Timing of MRS Command to Power Down Entry	$t_{MRSPDEN}$	t_{MOD}min	-	nCK	
PDA Timing					
Mode Register Set Command Cycle Time in PDA Mode	t_{MRD_PDA}	Max(16nCK, 10ns)	-	nCK	
Mode Register Set Command Update Delay in PDA Mode	t_{MOD_PDA}	t_{MOD}		nCK	
ODT Timing					
Asynchronous RTT Turn-On Delay (Power Down with DLL Frozen)	t_{AONAS}	1	9	ns	
Asynchronous RTT Turn-Off Delay (Power Down with DLL Frozen)	t_{AOFAS}	1	9	ns	
RTT Dynamic Change Skew	t_{ADC}	0.3	0.7	$t_{CK(avg)}$	
Write Leveling Timing					
First DQS/$\overline{DQS}$ Rising Edge after Write Leveling Mode is Programmed	t_{WLMRD}	40	-	nCK	12
DQS/$\overline{DQS}$ Delay after Write Leveling Mode is Programmed	$t_{WLDQSEN}$	25	-	nCK	12
Write Leveling Setup Time from Rising CK, $\overline{CK}$ Crossing to Rising DQS, $\overline{DQS}$ Crossing	t_{WLS}	0.13	-	$t_{CK(avg)}$	
Write Leveling Hold Time from Rising CK, $\overline{CK}$ Crossing to Rising DQS, $\overline{DQS}$ Crossing	t_{WLH}	0.13	-	$t_{CK(avg)}$	
Write Leveling Output Delay	t_{WLO}	0	9.5	ns	
Write Leveling Output Error	t_{WLOE}	-	-	ns	
CA Parity Timing					
Commands not Guaranteed to be Executed during this Time	$t_{PAR\_UNKNOWN}$	-	PL	nCK	

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Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Delay from Errant Command to $\overline{\text{ALERT}}$ Assertion	$t_{PAR\_ALERT\_ON}$	-	PL + 6ns	nCK	
Pulse Width of $\overline{\text{ALERT}}$ Signal when Asserted	$t_{PAR\_ALERT\_PW}$	64	128	nCK	
Time from when $\overline{\text{ALERT}}$ is Asserted until Controller Must Start Providing DES Commands in Persistent CA Parity Mode	$t_{PAR\_ALERT\_RSP}$	-	57	nCK	
Parity Latency	PL	4		nCK	
CRC Error Reporting					
CRC Error to $\overline{\text{ALERT}}$ Latency	t_{CRC_ALERT}	3	13	ns	
CRC $\overline{\text{ALERT}}$ Pulse Width	$t_{CRC\_ALERT\_PW}$	6	10	nCK	
Refresh Timing					
1x Refresh Cycle Time - 8Gb	t_{RFC1}	260	-	ns	34
2x Refresh Cycle Time - 8Gb	t_{RFC2}	160	-	ns	34
4x Refresh Cycle Time - 8Gb	t_{RFC4}	110	-	ns	34

Device Timing Parameters Notes

UI = $t_{CK(avg)}$min/2

1. Start of internal write transaction is defined as follows:
   For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR}/t_{CK} following the rounding algorithm defined in the Rounding Algorithm Section
5. WR in clock cycles as programmed in MR0.
6. t_{REFI} depends on t_{OPER}.
7. CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports t_{nPARAM} [nCK] = RU {t_{PARAM} [ns]/$t_{CK(avg)}$ [ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.
10. When CRC and DM are both enabled $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.
11. When CRC and DM are both enabled $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing. Measurement method is TBD.
15. DQ to DQ static offset relative to strobe per group. Measurement method is TBD.
16. This parameter will be characterized and guaranteed by design.

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17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock (output deratings are relative to the SDRAM input clock). Example TBD.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. t_{QSL} describes the instantaneous differential output low pulse width on DQS - $\overline{DQS}$, as measured from on falling edge to the next consecutive rising edge.
21. t_{QSH} describes the instantaneous differential output high pulse width on DQS - $\overline{DQS}$, as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval t_{REFI}.
23. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, $t_{WR\_CRC\_DM}$ is used in place of t_{WR}.
29. When CRC and DM are both enabled $t_{WTR\_S\_CRC\_DM}$ is used in place of t_{WTR_S}.
30. When CRC and DM are both enabled $t_{WTR\_L\_CRC\_DM}$ is used in place of t_{WTR_L}.
31. After CKE is registered LOW, CKE signal level shall be maintained below V_{IL}(DC) for t_{CKE} specification (LOW Pulse Width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above V_{IH}(DC) for t_{CKE} specification (HIGH Pulse Width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from $t_{CK(avg)}$min to $t_{CK(avg)}$max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Table.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RZQ/7 RONNOM = 34 ohms.
40. 1 t_{CK} toggle mode with setting MR4:A11 to 0.
41. 2 t_{CK} toggle mode with setting MR4:A11 to 1.
42. 1 t_{CK} mode with setting MR4:A12 to 0.
43. 2 t_{CK} mode with setting MR4:A12 to 1.
44. The maximum read preamble is bounded by $t_{LZ(DQS)}$min on the left side and t_{DQSCK}(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS differential signal cross point.
46. Last falling edge of DQS differential signal cross point to DQ rising signal middle-point of transferring from Low to High.
47. V_{REFDQ} value must be set to either its midpoint or V_{CENT_DQ}(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by t_{DQSCK}(min) plus t_{QSH}(min) on the left side and $t_{HZ(DQS)}$max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * V_{DDQ} as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to V_{TT} = V_{DDQ}.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5 nCK.

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I_{DD} and I_{PP} Measurement-Loop Patterns Timing

Speed Bin		DDR4-2666	Units
Parameter		19-19-19	
t_{CK}		0.75	ns
CL		15	nCK
CWL		14	nCK
nRCD		15	nCK
nRC		51	nCK
nRAS		36	nCK
nRP		15	nCK
nFAW	x4	16	nCK
	x8	23	
	x16	32	
nRRDS	x4	4	nCK
	x8	4	
	x16	6	
nRRDL	x4	6	nCK
	x8	6	
	x16	7	
nRFC		278	nCK

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I_{DD} and I_{PP} Measurement Conditions

- I_{DD} currents (such as I_{DD0}, I_{DD0A}, I_{DD1}, I_{DD1A}, I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3NA}, I_{DD3P}, I_{DD4R}, I_{DD4RA}, I_{DD4W}, I_{DD4WA}, I_{DD5B}, I_{DD5F2}, I_{DD5F4}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7} and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the DDR4 SDRAM under test tied together. Any I_{PP} current is not included in I_{DD} currents.
- I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured.

- "0" and "LOW" is defined as $V_{IN} \leq V_{IL}$(AC)max.
- "1" and "HIGH" is defined as $V_{IN} \geq V_{IH}$(AC)min.
- "MID-LEVEL" is defined as inputs that are $V_{REF} = V_{DD}/2$.
- Timings used for I_{DD} and I_{PP} Measurement-Loop Patterns are provided in the I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54.
- Basic I_{DD} and I_{PP} Measurement Conditions are described on pages 56-61.
- Detailed I_{DD} and I_{PP} Measurement-Loop Patterns are described on pages 63-71.
- I_{DD} and I_{PP} Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting:
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0B (Output Buffer enabled) in MR1;
  TDQS disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3;
  Read/Write DBI disabled in MR5;
  DM disabled in MR5
- Attention: The I_{DD} and I_{PP} Measurement-Loop Patterns need to be executed at least one time before actual I_{DD} and I_{PP} measurement is started.
- Define $\underline{D}$ = {$\overline{CS}$, $\overline{ACT}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}: = {HIGH, LOW, LOW, LOW, LOW}
- Define $\underline{D}$ = {CS, ACT, RAS, CAS, WE}: = {HIGH, HIGH, HIGH, HIGH, HIGH}

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Basic I_{DD} and I_{PP} Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL = 0)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, nRC, nRAS, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** HIGH between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially toggling according to I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern on page 63; **Data I/O:** V_{DD}; **DM:** Stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,... (See I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern on page 63); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern on page 63
I_{DD0A}	**Operating One Bank Active-Precharge Current (AL = CL - 1)** **AL:** CL-1; **Other conditions:** See I_{DD0}
I_{PP0}	**Operating One Bank Active-Precharge IPP Current** Same conditions as I_{DD0}
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL = 0)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, nRC, nRAS, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** HIGH between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data I/O:** Partially toggling according to I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern on page 64; **DM:** Stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,... (See I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern on page 64); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern on page 64
I_{DD1A}	**Operating One Bank Active-Read-Precharge Current (AL = CL - 1)** **AL:** CL - 1; **Other Conditions:** See I_{DD1}
I_{PP1}	**Operating One Bank Active-Read-Precharge IPP Current** Same Conditions as I_{DD1}
I_{DD2N}	**Precharge Standby Current (AL = 0)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs, Data I/O:** Partially Toggling according to I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N} Measurement-Loop Pattern on page 65; **DM:** Stable at 1; **Bank Activity:** All Banks Closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N} Measurement-Loop Pattern on page 65
I_{DD2NA}	**Precharge Standby Current (AL = CL - 1)** **AL:** CL - 1; **Other conditions:** See I_{DD2N}
I_{PP2N}	**Precharge Standby IPP Current** Same Conditions as I_{DD2N}

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Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I_{DD2NT}	**Precharge Standby ODT Current** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD2NT} Measurement-Loop Pattern on page 66; **Data I/O:** V_{SS}; **$\overline{DM}$:** Stable at 1; **Bank Activity:** All Banks Closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Toggling according to I_{DD2NT} Measurement-Loop Pattern on page 66; **Pattern Details:** See I_{DD2NT} Measurement-Loop Pattern on page 66
I_{DD2NL}	**Precharge Standby Current with CAL Enabled** Same Conditions as I_{DD2N}; CAL Enabled[3]
I_{DD2NG}	**Precharge Standby Current with Geardown Mode Enabled** Same Conditions as I_{DD2N}; Geardown Mode Enabled[3]
I_{DD2ND}	**Precharge Standby Current with DLL Disabled** Same Conditions as I_{DD2N}; DLL Disabled[3]
I_{DD2N_par}	**Precharge Standby Current with CA Parity Enabled** Same Conditions as I_{DD2N}; CA Parity Enabled[3]
I_{DD2P}	**Precharge Power-Down Current** **CKE:** LOW; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **DATA I/O:** V_{DD}; **$\overline{DM}$:** Stable at 1; **Bank Activity:** All Banks Closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0
I_{PP2P}	**Precharge Power-Down IPP Current** Same Conditions as I_{DD2P}
I_{DD2Q}	**Precharge Quiet Standby Current** **CKE:** High; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **DATA I/O:** V_{DD}; **$\overline{DM}$:** Stable at 1; **Bank Activity:** All Banks Closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0
I_{DD3N}	**Active Standby Current (AL = 0)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N} Measurement-Loop Pattern on page 65; **DATA I/O:** V_{DD}; **$\overline{DM}$:** Stable at 1; **Bank Activity:** All Banks Closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N} Measurement-Loop Pattern on page 65

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Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I_{DD3NA}	**Active Standby Current (AL = CL - 1)** **AL:** CL - 1; **Other conditions:** See I_{DD3N}
I_{PP3N}	**Active Standby IPP Current** Same Conditions as I_{DD3N}
I_{DD3P}	**Active Power-Down Current** **CKE:** LOW; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** Stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** Stable at 0; **DATA I/O:** V_{DD}; **DM:** Stable at 1; **Bank Activity:** All Banks Open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0
I_{PP3P}	**Active Power-Down IPP Current** Same Conditions as I_{DD3P}
I_{DD4R}	**Operating Burst Read Current (AL = 0)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** HIGH between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern on page 67; **DATA I/O:** Seamless Read Data Burst with Different Data between One Burst and the Next One according to I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern on page 67; **$\overline{DM}$:** Stable at 1; **Bank Activity:** All Banks Open, RD Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern on page 67); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern on page 67
I_{DD4RA}	**Operating Burst Read Current (AL = CL - 1)** **AL:** CL - 1; **Other conditions:** See I_{DD4R}
I_{DD4RB}	**Operating Burst Read Current with Read DBI** Same Conditions as I_{DD4R}; Read DBI Enabled[3]
I_{PP4R}	**Operating Burst Read IPP Current** Same Conditions as I_{DD4R}

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Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I_{DD4W}	**Operating Burst Write Current (AL = 0)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** HIGH between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern on page 68; **DATA I/O:** Seamless Write Data Burst with Different Data between One Burst and the Next One according to I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern on page 68; **$\overline{DM}$:** Stable at 1; **Bank Activity:** All Banks Open, WR Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern on page 68); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at HIGH; **Pattern Details:** See I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern on page 68
I_{DD4WA}	**Operating Burst Write Current (AL = CL - 1)** **AL:** CL - 1; **Other conditions:** See I_{DD4W}
I_{DD4WB}	**Operating Burst Write Current with Write DBI** Same Conditions as I_{DD4W}; Write DBI Enabled[3]
I_{DD4WC}	**Operating Burst Write Current with Write CRC** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$:** HIGH between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD4WC} Measurement-Loop Pattern on page 69; **DATA I/O:** Seamless Write Data Burst with Different Data between One Burst and the Next One according to I_{DD4WC} Measurement-Loop Pattern on page 69; **DM:** Stable at 1; **Bank Activity:** All Banks Open, WR Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I_{DD4WC} Measurement-Loop Pattern on page 69); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at HIGH; **Pattern Details:** See I_{DD4WC} Measurement-Loop Pattern on page 69 Measurement-Loop Pattern on page 68; Write CRC Enabled[3]
I_{DD4W_par}	**Operating Burst Write Current with CA Parity** Same Conditions as I_{DD4W}; CA Parity Enabled[3]
I_{PP4W}	**Operating Burst Write IPP Current** Same Conditions as I_{DD4W}

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Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I_{DD5B}	**Burst Refresh Current (1X REF)** **CKE:** HIGH; **External Clock:** On; **t_{CK}, CL, nRFC:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **CS:** HIGH between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD5B}, I_{PP5B}, I_{DD5F2}, I_{PP5F2} I_{DD5F4}, and I_{PP5F4} Measurement-Loop Pattern on page 70; **DATA I/O:** V_{DD}; **DM:** Stable at 1; **Bank Activity:** REF Command Every nRFC (See I_{DD5B}, I_{PP5B}, I_{DD5F2}, I_{PP5F2} I_{DD5F4}, and I_{PP5F4} Measurement-Loop Pattern on page 70); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD5B}, I_{PP5B}, I_{DD5F2}, I_{PP5F2} I_{DD5F4}, and I_{PP5F4} Measurement-Loop Pattern on page 70
I_{PP5B}	**Burst Refresh IPP Current (1X REF)** Same Conditions as I_{DD5B}
I_{DD5F2}	**Burst Refresh Current (2X REF)** Same Conditions as I_{DD5B}; $t_{RFC} = t_{RFC2}$
I_{PP5F2}	**Burst Refresh IPP Current (2X REF)** Same Conditions as I_{DD5F2}; $t_{RFC} = t_{RFC2}$
I_{DD5F4}	**Burst Refresh Current (4X REF)** Same Conditions as I_{DD5B}; $t_{RFC} = t_{RFC4}$
I_{PP5F4}	**Burst Refresh IPP Current (4X REF)** Same Conditions as I_{DD5F4}; $t_{RFC} = t_{RFC4}$
I_{DD6N}	**Self-Refresh Current: Normal Temperature Range** **T_{CASE}:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR):** Normal[4]; **CKE:** LOW; **External Clock:** Off; **CK and CK:** LOW; **CL:** I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **CS, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM:** Stable at 1; **Bank Activity:** Self-Refresh Operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6N}	**Self-Refresh IPP Current: Normal Temperature Range** Same Conditions as I_{DD6N}
I_{DD6E}	**Self-Refresh Current: Extended Temperature Range** **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR):** Extended[4]; **CKE:** LOW; **External Clock:** Off; **CK and CK:** LOW; **CL:** I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **CS, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM:** Stable at 1; **Bank Activity:** Extended Temperature Self-Refresh Operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6E}	**Self-Refresh IPP Current: Extended Temperature Range** Same Conditions as I_{DD6E}

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Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I_{DD6R}	**Self-Refresh Current: Extended Temperature Range** **T_{CASE}:** 0 - TBD (~35-45)°C; **Low Power Array Self Refresh (LP ASR):** Reduced[4]; **CKE:** LOW; **External Clock:** Off; **CK and CK:** LOW; **CL:** I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **CS, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM:** Stable at 1; **Bank Activity:** Reduced Temperature Self-Refresh Operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6R}	**Self-Refresh IPP Current: Reduced Temperature Range** Same Conditions as I_{DD6R}
I_{DD6A}	**Auto Self-Refresh Current** **T_{CASE}:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR):** Auto[4]; **Partial Array Self-Refresh (PASR):** Full Array; **CKE:** LOW; **External Clock:** Off; **CK and CK:** LOW; **CL:** I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** 0; **CS, Command, Address, Bank Group Address, Bank Address, Data I/O:** HIGH; **DM:** Stable at 1; **Bank Activity:** Auto Self-Refresh Operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
I_{PP6A}	**Auto Self-Refresh IPP Current** Same Conditions as I_{DD6A}
I_{DD7}	**Operating Bank Interleave Read Current** **CKE:** HIGH; **External Clock:** On; **t_{CK}, nRAS, nRCD, nRRD, nFAW, CL:** See I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 54; **BL:** 8[1]; **AL:** CL - 1; **CS:** HIGH between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** Partially Toggling according to I_{DD7} and I_{PP7} Measurement-Loop Pattern on page 71; **Data I/O:** Read Data Bursts with Different Data between One Burst and the Next One according to I_{DD7} and I_{PP7} Measurement-Loop Pattern on page 71; **DM:** Stable at 1; **Bank Activity:** Two Times Interleaved Cycling through Banks (0, 1,...7) with Different Addressing, See I_{DD7} and I_{PP7} Measurement-Loop Pattern on page 71; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** Stable at 0; **Pattern Details:** See I_{DD7} and I_{PP7} Measurement-Loop Pattern on page 71
I_{PP7}	**Operating Bank Interleave Read IPP Current** Same Conditions as I_{DD7}
I_{DD8}	**Maximum Power-Down Read Current** TBD
I_{PP8}	**Maximum Power-Down IPP Current** Same Conditions as I_{DD8}

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Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enabled:
   - Set MR1 [A12 = 0]: Qoff = Output buffer enabled
   - Set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7

   RTT_Nom Enabled:
   - Set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6

   RTT_WR Enabled:
   - Set MR2 [A10:9 = 01]: RTT_WR = RZQ/2

   RTT_PARK Disabled:
   - Set MR5 [A8:6 = 000]
3. CAL Enabled:
   - Set MR4 [A8:6 = 001]: 1600MT/s
   - Set MR4 [A8:6 = 010]: 1866MT/s, 2133MT/s
   - Set MR4 [A8:6 = 011]: 2400MT/s

   Geardown Mode Enabled:
   - Set MR3 [A3 = 1]: 1/4 Rate

   DLL Disabled:
   - Set MR1 [A0 = 0]

   CA Parity Enabled:
   - Set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
   - Set MR5 [A2:0 = 010]: 2400MT/s

   Read DBI Enabled:
   - Set MR5 [A12 = 1]

   Write DBI Enabled:
   - Set MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR):
   - Set MR2 [A7:6 = 00]: Normal Temperature Range
   - Set MR2 [A7:6 = 01]: Reduced Temperature Range
   - Set MR2 [A7:6 = 10]: Extended Temperature Range
   - Set MR2 [A7:6 = 11]: Auto Self Refresh.

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I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if Necessary																
		1	1*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 1 instead																
		2	2*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	3*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	4*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	5*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	6*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	7*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	8*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	10*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	11*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	12*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	13*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	14*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	15*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																

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I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1-2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3-4	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			...	Repeat pattern 1-4 until nRCD - 1. Truncate if Necessary																
			nRCD - AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if Necessary																
			1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	-
			1*nRC + 1-2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3-4	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRCD - 1. Truncate if Necessary																
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if Necessary																
		2	2*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	3*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	4*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	5*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	6*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	7*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	8*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	9*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	10*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	11*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	12*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	13*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	14*nRC	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	15*nRC	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																

I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	0
			3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	0
		1	4-7	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 1 instead																
		2	8-11	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	12-15	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 0, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 0, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																

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I_{DD2NT} Measurement-Loop Pattern

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4-7	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 1 and BA[1:0] = 1 instead																
		2	8-11	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	12-15	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, but ODT = 0, BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 0, but ODT = 1, BG[1:0][2] = 3 and BA[1:0] = 0 instead																

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I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2-3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	RD	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6-7	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	12-15	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																

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I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2-3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6-7	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	12-15	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																

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I_{DD4WC} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF D8 = CRC
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2-3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		1	4	WR	0	1	1	0	1	0	0	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00 D8 = CRC
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6-7	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
		2	8-11	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	12-15	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	16-19	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		5	20-23	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		6	24-27	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		7	28-31	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		8	32-35	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		9	36-39	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		10	40-43	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		11	44-47	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		12	48-51	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		13	52-55	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		14	56-59	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		15	60-63	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																

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I_{DD5B}, I_{PP5B}, I_{DD5F2}, I_{PP5F2}, I_{DD5F4} and I_{PP5F4} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4	$\overline{D}$, $\overline{D}$	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			4-7	Repeat Pattern 1-4, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
			8-11	Repeat Pattern 1-4, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
			12-15	Repeat Pattern 1-4, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
			16-19	Repeat Pattern 1-4, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
			20-23	Repeat Pattern 1-4, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
			24-27	Repeat Pattern 1-4, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
			28-31	Repeat Pattern 1-4, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
			32-35	Repeat Pattern 1-4, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
			36-39	Repeat Pattern 1-4, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
			40-43	Repeat Pattern 1-4, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
			44-47	Repeat Pattern 1-4, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
			48-51	Repeat Pattern 1-4, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
			52-55	Repeat Pattern 1-4, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
			56-59	Repeat Pattern 1-4, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
			60-63	Repeat Pattern 1-4, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																
		2	64-nRFC - 1	Repeat Sub-Loop 1. Truncate if Necessary																

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I_{DD7} and I_{PP7} Measurement-Loop Pattern[1]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{ACT}$	$\overline{RAS}$/A16	$\overline{CAS}$/A15	$\overline{WE}$/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[2:0]	A[12]/$\overline{BC}$	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	ACT	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	-
			1	RDA	0	0	1	0	1	0	0	0	0	0	0	1	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	$\overline{D}$	1	1	1	1	1	0	0	3^2	3	0	0	0	7	F	0	-
			...	Repeat pattern 2-3 until nRRD - 1, if nRCD > 4. Truncate if Necessary																
		1	nRRD	ACT	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0	0	1	1	0	0	1	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			...	Repeat pattern 2-3 until 2*nRRD - 1, if nRCD > 4. Truncate if Necessary																
		2	2*nRRD	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 2 instead																
		3	3*nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 3 instead																
		4	4*nRRD	Repeat pattern 2-3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if Necessary																
		5	nFAW	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 1 instead																
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 2 instead																
		7	nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0][2] = 0 and BA[1:0] = 3 instead																
		8	nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 1 and BA[1:0] = 0 instead																
		9	nFAW + 4*nRRD	Repeat Sub-Loop 4																
		10	2*nFAW	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 0 instead																For x4 and x8 only
		11	2*nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 1 instead																
		12	2*nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 2 instead																
		13	2*nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 3 instead																
		14	2*nFAW + 4*nRRD	Repeat Sub-Loop 4																
		15	3*nFAW	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 1 instead																
		16	3*nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 2 instead																
		17	3*nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0][2] = 2 and BA[1:0] = 3 instead																
		18	3*nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0][2] = 3 and BA[1:0] = 0 instead																
		19	3*nFAW + 4*nRRD	Repeat Sub-Loop 4																
		20	4*nFAW	Repeat pattern 2-3 until nRC - 1, if nRC > 4*nFAW. Truncate if Necessary																

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Notes:
1. DQS, $\overline{DQS}$ are V_{DD}.
2. BG1 is don't care for a x16 device.
3. C[2:0] are used only for a 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V_{DD}.

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I_{DD} Specifications

Parameter	DDR4-2666	Units
	19-19-19	
I_{DD0}	TBD	mA
I_{DD0A}	TBD	mA
I_{DD1}	TBD	mA
I_{DD1A}	TBD	mA
I_{DD2N}	TBD	mA
I_{DD2NA}	TBD	mA
I_{DD2NT}	TBD	mA
I_{DD2NL}	TBD	mA
I_{DD2NG}	TBD	mA
I_{DD2ND}	TBD	mA
I_{DD2N_par}	TBD	mA
I_{DD2P}	TBD	mA
I_{DD2Q}	TBD	mA
I_{DD3N}	TBD	mA
I_{DD3NA}	TBD	mA
I_{DD3P}	TBD	mA
I_{DD4R}	TBD	mA
I_{DD4RA}	TBD	mA
I_{DD4RB}	TBD	mA
I_{DD4W}	TBD	mA
I_{DD4WA}	TBD	mA
I_{DD4WB}	TBD	mA
I_{DD4WC}	TBD	mA
I_{DD4W_PAR}	TBD	mA

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I_{DD} Specifications (Continued)

Parameter	DDR4-2666	Units
	19-19-19	
I_{DD5B}	TBD	mA
I_{DD5F2}	TBD	mA
I_{DD5F4}	TBD	mA
I_{DD6N}	TBD	mA
I_{DD6E}	TBD	mA
I_{DD6R}	TBD	mA
I_{DD6A}	TBD	mA
I_{DD7}	TBD	mA
I_{DD8}	TBD	mA

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I_{PP} Specifications

Parameter	DDR4-2666	Units
	19-19-19	
I_{PP0}	TBD	mA
I_{PP1}	TBD	mA
I_{PP2N}	TBD	mA
I_{PP2P}	TBD	mA
I_{PP3N}	TBD	mA
I_{PP3P}	TBD	mA
I_{PP4R}	TBD	mA
I_{PP4W}	TBD	mA
I_{PP5B}	TBD	mA
I_{PP5F2}	TBD	mA
I_{PP5F4}	TBD	mA
I_{PP6N}	TBD	mA
I_{PP6E}	TBD	mA
I_{PP6R}	TBD	mA
I_{PP6A}	TBD	mA
I_{PP7}	TBD	mA
I_{PP8}	TBD	mA

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Input/Output Capacitance

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Input/output capacitance	C_{IO}	0.55	1.15	pF	1, 2
Input/output capacitance delta	C_{DIO}	-0.1	0.1	pF	1, 2, 8
Input/output capacitance delta, DQS and $\overline{DQS}$	C_{DDQS}	-	0.05	pF	1, 2, 4
Input capacitance, CK and $\overline{CK}$	C_{CK}	0.8	1.0	pF	1
Input capacitance delta, CK and $\overline{CK}$	C_{DCK}	-	0.1	pF	1, 3
Input capacitance, ADD, CMD, CTRL input-only pins	C_I	0.8	1.0	pF	1, 5
Input capacitance delta, ADD, CMD, CTRL input-only pins	C_{DI}	-	0.2	pF	1, 6, 7
Input capacitance of ALERT	C_{ALERT}	0.5	2	pF	1

Notes:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, $\overline{DM}$, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS
3. Absolute value CK - $\overline{CK}$
4. Absolute value of C_{IO}(DQS) - C_{IO}($\overline{DQS}$)
5. C_I applies to ODT, $\overline{CS}$, CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.
6. C_{DI} applies to ODT, $\overline{CS}$, CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}$/A16, $\overline{CAS}$/A15, $\overline{WE}$/A14, $\overline{ACT}$ and PAR.
7. $C_{DI} = C_I - 0.5 * (C_I(CLK) + C_I(\overline{CLK}))$
8. $C_{DIO} = C_{IO}(DQ, \overline{DM}) - 0.5 * (C_{IO}(DQS) + C_{IO}(\overline{DQS}))$.

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Serial Presence Detect (SPD)

Serial Presence Detect Table

Byte No.	Byte Description	Supported Value	Hex Value
0	Number of Serial PD Bytes Written / SPD Device Size / CRC Coverage	512 Total Bytes / 384 Bytes Used	23h
1	SPD Revision	Revision 1.2	12h
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0Ch
3	Key Byte / Module Type	RDIMM	01h
4	SDRAM Density and Banks	4 Bank Groups / 4 Banks / 8 Gb	85h
5	SDRAM Addressing	16 Row / 10 Column	21h
6	SDRAM Package Type	Monolithic	00h
7	SDRAM Optional Features	tMAW = 8192*tREFI / MAC = Unlimited	08h
8	SDRAM Thermal and Refresh Options	Reserved	00h
9	Other SDRAM Optional Features	Hard & Soft PPR	60h
10	Secondary SDRAM Package Type	Symmetrical Devices	00h
11	Module Nominal Voltage (VDD)	1.2V	03h
12	Module Organization	1 Rank / x8	01h
13	Module Memory Bus Width	ECC / 64 bits	0Bh
14	Module Thermal Sensor	Thermal Sensor	80h
15-16	Extended Module Type	Reserved	00h
17	Timebases	MTB = 125 ps / FTB = 1 ps	00h
18	SDRAM Minimum Cycle Time (tCKAVGmin)	0.75 ns	06h
19	SDRAM Maximum Cycle Time (tCKAVGmax)	1.6 ns	0Dh
20	CAS Latencies Supported (First Byte)	10 / 11 / 12 / 13 / 14	F8h
21	CAS Latencies Supported (Second Byte)	15 / 16 / 17 / 18 / 19 / 20 / 21 / 22	FFh
22	CAS Latencies Supported (Third Byte)	-	01h
23	CAS Latencies Supported (Fourth Byte)	-	00h
24	Minimum CAS Latency Time (tAAmin)	13.75 ns	6Eh
25	Minimum RAS to CAS Delay Time (tRCDmin)	13.75 ns	6Eh
26	Minimum Row Precharge Delay Time (tRPmin)	13.75 ns	6Eh

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Byte No.	Byte Description	Supported Value	Hex Value
27	Upper Nibbles for tRASmin and tRCmin	tRAS = 32 ns / tRC = 45.75 ns	11h
28	Minimum Active to Precharge Delay Time (tRASmin) (LSB)	32 ns	00h
29	Minimum Active to Active/Refresh Delay Time (tRCmin) (LSB)	45.75 ns	6Eh
30	Minimum Refresh Recovery Delay Time (tRFC1min) (LSB)	350 ns	F0h
31	Minimum Refresh Recovery Delay Time (tRFC1min) (MSB)	350 ns	0Ah
32	Minimum Refresh Recovery Delay Time (tRFC2min) (LSB)	260 ns	20h
33	Minimum Refresh Recovery Delay Time (tRFC2min) (MSB)	260 ns	08h
34	Minimum Refresh Recovery Delay Time (tRFC4min) (LSB)	160 ns	00h
35	Minimum Refresh Recovery Delay Time (tRFC4min) (MSB)	160 ns	05h
36	Minimum Four Activate Window Time (tFAWmin) (MSB)	21 ns	00h
37	Minimum Four Activate Window Time (tFAWmin) (LSB)	21 ns	A8h
38	Minimum Activate to Activate Delay Time (tRRD_Smin) (different bank group)	3 ns	18h
39	Minimum Activate to Activate Delay Time (tRRD_Lmin) (same bank group)	4.9 ns	28h
40	Minimum CAS to CAS Delay Time (tCCD_Lmin) (same bank group)	5 ns	28h
41	Upper Nibble for tWRmin	15 ns	00h
42	Minimum Write Recovery Time (tWRmin)	15 ns	78h
43	Upper Nibbles for tWTRmin	tWTR_S = 2.5 ns / tWTR_L = 7.5 ns	00h
44	Minimum Write to Read Time (tWTR_Smin) (different bank group)	2.5 ns	14h
45	Minimum Write to Read Time (tWTR_Lmin) (same bank group)	7.5 ns	3Ch
46-59	Reserved	-	00h
60	Connector to SDRAM Bit Mapping	DQ0-DQ3	24h
61	Connector to SDRAM Bit Mapping	DQ4-DQ7	03h

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Byte No.	Byte Description	Supported Value	Hex Value
62	Connector to SDRAM Bit Mapping	DQ8-DQ11	15h
63	Connector to SDRAM Bit Mapping	DQ12-DQ15	2Ch
64	Connector to SDRAM Bit Mapping	DQ16-DQ19	24h
65	Connector to SDRAM Bit Mapping	DQ20-DQ23	03h
66	Connector to SDRAM Bit Mapping	DQ24-DQ27	15h
67	Connector to SDRAM Bit Mapping	DQ28-DQ31	2Ch
68	Connector to SDRAM Bit Mapping	CB0-CB3	24h
69	Connector to SDRAM Bit Mapping	CB4-CB7	03h
70	Connector to SDRAM Bit Mapping	DQ32-DQ35	24h
71	Connector to SDRAM Bit Mapping	DQ36-DQ39	03h
72	Connector to SDRAM Bit Mapping	DQ40-DQ43	15h
73	Connector to SDRAM Bit Mapping	DQ44-DQ47	2Ch
74	Connector to SDRAM Bit Mapping	DQ48-DQ51	24h
75	Connector to SDRAM Bit Mapping	DQ52-DQ55	03h
76	Connector to SDRAM Bit Mapping	DQ56-DQ59	15h
77	Connector to SDRAM Bit Mapping	DQ60-DQ63	77h
78-116	Reserved	-	00h
117	Fine Offset for Minimum CAS to CAS Delay Time (tCCD_Lmin) (same bank group)	5 ns	00h
118	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Lmin) (same bank group)	4.9 ns	9Ch
119	Fine Offset for Minimum Activate to Activate Delay Time (tRRD_Smin) (different bank group)	3 ns	00h
120	Fine Offset for Minimum Activate to Activate/Refresh Delay Time (tRCmin)	45.75 ns	00h
121	Fine Offset for Minimum Row Precharge Delay Time (tRPmin)	13.75 ns	00h
122	Fine Offset for Minimum RAS to CAS Delay Time (tRCD-min)	13.75 ns	00h
123	Fine Offset for Minimum CAS Latency Time (tAAmin)	13.75 ns	00h
124	Fine Offset for SDRAM Maximum Cycle Time (tCKAVG-max)	1.6 ns	E7h
125	Fine Offset for SDRAM Minimum Cycle Time (tCKAVG-min)	0.75 ns	00h

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Byte No.	Byte Description	Supported Value	Hex Value
126	CRC for Base Configuration Section (LSB)	CRC for bytes 0-125	B6h
127	CRC for Base Configuration Section (MSB)	CRC for bytes 0-125	A4h
128	Raw Card Extension / Module Nominal Height	31.25mm	11h
129	Module Maximum Thickness	Front = 1.3mm / Back = 1.2 mm	11h
130	Reference Raw Card Used	R/C D / Revision 1	23h
131	DIMM Module Attributes	DDR4RCD02 / 1 Row / 1 Register	15h
132	RDIMM Thermal Heat Spreader Solution	No Heatspreader	00h
133	Register Manufacturer ID Code (LSB)	IDT	80h
134	Register Manufacturer ID Code (MSB)	IDT	B3h
135	Register Revision Number	4RCD0229KB1	51h
136	Address Mapping from Register to DRAM	Standard	00h
137	Register Output Drive Strength for Control	Address/Control Drive Strength	00h
138	Register Output Drive Strength for CK	CK Drive Strength	00h
139-253	Reserved	-	00h
254	CRC for Module Specific Section (LSB)	CRC for bytes 128-253	91h
255	CRC for Module Specific Section (MSB)	CRC for bytes 128-253	36h
256-319	Reserved	-	00h
320	Module Manufacturer's ID Code (LSB)	1 Continuation Code	01h
321	Module Manufacturer's ID Code (MSB)	SMART's ID Code	94h
322	Module Manufacturing Location	See Note 1	xxh
323	Module Manufacturing Date	Date (Year)	xxh
324	Module Manufacturing Date	Date (Week)	xxh
325-328	Module Serial Number	Serial Number	xxh
329	Module Part Number	S	53h
330	Module Part Number	T	54h
331	Module Part Number	I	49h
332	Module Part Number	1	31h
333	Module Part Number	0	30h
334	Module Part Number	2	32h
335	Module Part Number	7	37h

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Byte No.	Byte Description	Supported Value	Hex Value
336	Module Part Number	R	52h
337	Module Part Number	D	44h
338	Module Part Number	4	34h
339	Module Part Number	1	31h
340	Module Part Number	0	30h
341	Module Part Number	8	38h
342	Module Part Number	9	39h
343	Module Part Number	3	33h
344	Module Part Number	S	53h
345	Module Part Number	C	43h
346	Module Part Number		20h
347	Module Part Number		20h
348	Module Part Number		20h
349	Module Revision Code	Revision 0	00h
350	DRAM Manufacturer's ID Code (LSB)	Samsung	80h
351	DRAM Manufacturer's ID Code (MSB)	Samsung	CEh
352	DRAM Stepping	Revision C	00h
353	Module Manufacturer's Specific Data	S	53h
354	Module Manufacturer's Specific Data	M	4Dh
355	Module Manufacturer's Specific Data	A	41h
356	Module Manufacturer's Specific Data	R	52h
357	Module Manufacturer's Specific Data	T	54h
358	Module Manufacturer's Specific Data	M	4Dh
359	Module Manufacturer's Specific Data	o	6Fh
360	Module Manufacturer's Specific Data	d	64h
361	Module Manufacturer's Specific Data	u	75h
362	Module Manufacturer's Specific Data	l	6Ch
363	Module Manufacturer's Specific Data	a	61h
364	Module Manufacturer's Specific Data	r	72h
365	Module Manufacturer's Specific Data	T	54h
366	Module Manufacturer's Specific Data	e	65h
367	Module Manufacturer's Specific Data	c	63h

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Byte No.	Byte Description	Supported Value	Hex Value
368	Module Manufacturer's Specific Data	h	68h
369	Module Manufacturer's Specific Data	n	6Eh
370	Module Manufacturer's Specific Data	o	6Fh
371	Module Manufacturer's Specific Data	l	6Ch
372	Module Manufacturer's Specific Data	o	6Fh
373	Module Manufacturer's Specific Data	g	67h
374	Module Manufacturer's Specific Data	i	69h
375	Module Manufacturer's Specific Data	e	65h
376	Module Manufacturer's Specific Data	s	73h
377	Module Manufacturer's Specific Data	For Internal Use	xxh
378-381	Module Manufacturer's Specific Data	-	00h
382-383	Reserved	-	00h
384-511	End User Programmable	-	00h

Notes:

1. Manufacturing Location:
   00h - Undefined,
   01h - Newark, CA, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

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Declaration of Conformity

CE

Responsible Party Name:	SMART Modular Technologies, Inc.
Address:	39870 Eureka Drive Newark, CA 94560-4809, USA
Phone:	+1-510-623-1231

hereby declares that the products:

STI1027RD410893SC

to which this declaration relates are in conformity with the following Directives and other normative documents:

RoHS Directive 2011/65/EU

Restriction of the use of certain hazardous substances in electrical and electronic equipment

- **EN 50581:2012**
  Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Name: Jeffrey Milano
Title: Director, Worldwide Quality
Date: March 27, 2018

Representative in the European Union (for regulatory topics only):
Mr. Graham Kyle
SMART Modular Technologies (Europe) Ltd.
312 Nasmyth Building, Nasmyth Avenue
Scottish Enterprise Technology Park
East Kilbride, Scotland, G75 0QR

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