

Ordering Information

Part Number	Description	Device Vendor
ST1026MP41W693HC	1Gx64 (8GB), DDR4, 216-Pin Unbuffered Module in Package (MIP), Non-ECC, 1Gx16 Based (SR DDP - two 1Gx8), DDR4-2666-19-19-19, 22.25mm, 1.2V, Halogen-Free & RoHS Compliant.	Hynix, Rev. C H5ANAG6NCMR-VKC

(All specifications of this module are subject to change without notice.)

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Part Number Decode

S	T	102	6	MP4	1W6	9	3	H	C
1	2	3	4	5	6	7	8	9	10

1	SMART Modular Technologies
2	Module Process Technology T: RoHS Compliant DDR4 Enterprise
3	Module Address Depth 102: 1G
4	Module Data Bus Width 6: x64
5	Module Configuration MP4: 1.2V DDR4 216-Pin Unbuffered Module in Package (MIP)
6	Device Configuration 1W6: 1Gx16 SR DDP Based
7	CAS Latency 9: CL 19
8	Device Speed 3: DDR4-2666
9	Device Vendor H: Hynix
10	Device Revision C: Revision C

Revision History

Date	Description
January 31, 2019	Datasheet released.
February 12, 2019	Added the ECC Block Diagram on page 8.

8GB (1Gx64) DDR4 SDRAM Module - 1Gx16 Based (SR DDP - two 1Gx8) 216-Pin Unbuffered Module in Package (MIP), Non-ECC

Features

- Standard = Custom
- Configuration = Non-ECC
- Number of Module Ranks = 1 Rank
- Number of Devices = 8
- $V_{DD} = V_{DDQ} = 1.2V$
- $V_{PP} = 2.5V$
- $V_{DDSPD} = 1.4V$ to $3.6V$
- Cycle Time = 0.833ns
- CAS Latency = 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20
- CAS Latency with Read DBI = 12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23
- Additive Latency = 0, CL - 1, and CL - 2
- CAS Write Latency (CWL) = 9, 10, 11, 12, 14, 16, 18
- Burst Length (BL) switch on-the-fly BL8 or BC4 (Burst Chop)
- Burst Type = Sequential & Interleave
- Bi-Directional Differential Data Strobe
- On-Die Termination (ODT)
- 8 bit pre-fetch
- Device Package = DDP FBGA
- Ball Finish = SAC305 (SnAgCu)
- Length x Height = 22.25mm x 22.25mm
- No. of sides = Double-sided
- Bank Grouping is applied, and \overline{CAS} to \overline{CAS} latency (t_{CCD_L} , t_{CCD_S}) for the banks in the same or different bank group accesses are available
- Temperature sensor
- Per DRAM Addressability is supported
- Internal V_{REF} for data inputs
- Write CRC is supported
- DBI (Data Bus Inversion) is supported
- CA parity (Command/Address Parity) mode is supported

Addressing

Device Configuration	1Gx16 SR DDP*
Number of Bank Groups	4
Bank Groups	BG0 - BG1
Bank Address	BA0 - BA1
Row Address	A0 - A15
Column Address	A0 - A9
Page size - per array	1KB
Page size - package	2KB

* x16 Single Rank (SR) Dual Die Package (DDP) is comprised of two x8 devices connected in parallel.

Pin Description Table

Symbol	Type	Function
CK0, $\overline{\text{CK0}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$.
CKE0	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After V_{REFCA} and Internal DQ V_{REF} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{\text{CS0}}$	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT0	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ and $\overline{\text{DM/DBI/TDQS}}$, NU/ $\overline{\text{TDQS}}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
$\overline{\text{ACT}}$	Input	Activation Command Input: $\overline{\text{ACT}}$ defines the Activation command being entered along with $\overline{\text{CS}}$. The input into RAS/A16, CAS/A15 and WE/A14 will be considered as Row Address A16, A15 and A14.
$\overline{\text{RAS/A16}}$, $\overline{\text{CAS/A15}}$, $\overline{\text{WE/A14}}$	Input	Command Inputs: $\overline{\text{RAS/A16}}$, $\overline{\text{CAS/A15}}$ and $\overline{\text{WE/A14}}$ (along with $\overline{\text{CS}}$) define the command being entered. Those pins have multi function. For example, for activation with $\overline{\text{ACT}}$ Low, those are Addressing like A16, A15 and A14 but for non-activation command with $\overline{\text{ACT}}$ High, those are Command pins for Read, Write and other command defined in command truth table.
$\overline{\text{DM0/DBI0-}}$ $\overline{\text{DM7/DBI7}}$	Input/ Output	Input Data Mask and Data Bus Inversion: $\overline{\text{DM}}$ is an input mask signal for write data. Input data is masked when $\overline{\text{DM}}$ is sampled LOW coincident with that input data during a Write access. $\overline{\text{DM}}$ is sampled on both edges of DQS. $\overline{\text{DM}}$ is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. The function of $\overline{\text{DM}}$ is enabled by Mode Register A11 setting in MR1. DBI is an input/output identifying whether to store/output the true or inverted data. If DBI is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI is HIGH.
BG0-BG1	Input	Bank Group Inputs: BG0 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0-BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0-A15	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC, RAS/A16, CAS/A15 and WE/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands.
A10/AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12/ $\overline{\text{BC}}$	Input	Burst Chop: A12/ $\overline{\text{BC}}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} .

Pin Description Table (Continued)

Symbol	Type	Function
DQ0-DQ63	Input/ Output	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal V_{REF} level during test via Mode Register Setting MR4 A4 = HIGH.
$\overline{DQS0-DQS7}$, DQS0-DQS7	Input/ Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PARITY	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT, RAS/A16, CAS/A15, WE/A14, BG0-BG1, BA0-BA1, A16-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS LOW.
\overline{ALERT}	Input/ Output	Alert: It has multiple functions, such as CRC error flag, or Command and Address Parity error flag. If there is error in the CRC, then \overline{ALERT} goes LOW for a period of time and goes back HIGH. If there is error in the Command Address Parity Check, then \overline{ALERT} goes LOW for a relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case it is not connected, \overline{ALERT} Pin must be connected to V_{DD} on the board.
SA0	Input	This signal is tied at the system to either V_{SS} or V_{DDSPD} to configure the serial temperature sensor address range.
SDA	Input/ Output	This bidirectional pin is used to transfer data into or out of the temperature sensor. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pull-up on the system board.
SCL	Input	This signal is used to clock data into and out of the temperature sensor. An external resistor may be connected from the SDA bus line to V_{DDSPD} to act as a pull-up on the system board.
\overline{EVENT}	Output	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the \overline{EVENT} pin on thermal sensing part. No pull-up resistor is provided on the MIP.
NC	-	No Connect.
RFU	-	Reserved for Future Use
V_{DD}	Supply	Power Supply.
V_{SS}	Supply	Ground.
V_{PP}	Supply	DRAM Activating Power Supply.
V_{REFCA}	Supply	Reference voltage for address/command inputs.
V_{DDSPD}	Supply	Power supply for the Temperature Sensor.
V_{TT}	Supply	Termination voltage for address/command/control/clock nets.

DDR4 216-Pin Unbuffered Module in Package (MIP) Pin List

	1	2	3	4	5	6	7	8
A	V _{TT}	A16/ <u>RAS</u>	ODT0	V _{DD}	V _{SS}	RFU	V _{SS}	V _{DD}
B	<u>CKE0</u>	V _{DD}	<u>CK0</u>	V _{SS}	DQ30	V _{DD}	DQ28	V _{SS}
C	A14/ <u>WE</u>	<u>CS0</u>	CK0	DQ24	DQ26	<u>DM6/DBI6</u>	DQ54	DQ48
D	A15/ <u>CAS</u>	V _{SS}	BG0	<u>DQS3</u>	DQS3	V _{SS}	DQ52	DQ50
E	A6	V _{DD}	BA1	<u>DQS7</u>	DQS7	V _{DD}	DQ17	V _{SS}
F	BG1	A0	PARITY	V _{SS}	DQ19	<u>DM2/DBI2</u>	DQ61	DQ57
G	A10	V _{SS}	A13	DQ23	DQ21	V _{SS}	DQ63	DQ59
H	A8	V _{DD}	A2	V _{SS}	DQ31	V _{DD}	DQ29	V _{SS}
J	BA0	A11	A3	DQ25	DQ27	<u>DM3/DBI3</u>	DQ55	DQ51
K	A9	A1	A5	<u>DQS2</u>	DQS2	V _{SS}	DQ53	DQ49
L	A7	V _{DD}	A4	<u>DQS6</u>	DQS6	V _{DD}	DQ18	V _{SS}
M	A12	V _{TT}	ACT	V _{SS}	DQ16	<u>DM7/DBI7</u>	DQ60	DQ58
N	<u>EVENT</u>	V _{SS}	SCL	DQ22	DQ20	V _{SS}	DQ62	DQ56
P	<u>ALERT</u>	V _{REFCA}	<u>RESET</u>	V _{PP}	V _{SS}	V _{DD}	V _{SS}	V _{PP}
R	SA0	V _{DDSPD}	SDA	DQ14	DQ12	V _{SS}	DQ46	DQ40
T	A12	V _{TT}	ACT	V _{SS}	DQ8	<u>DM5/DBI5</u>	DQ44	DQ42
U	A7	V _{DD}	A4	<u>DQS4</u>	DQS4	V _{DD}	DQ10	V _{SS}
V	A9	A1	A5	<u>DQS1</u>	DQS1	V _{SS}	DQ37	DQ33
W	BA0	A11	A3	DQ1	DQ3	<u>DM0/DBI0</u>	DQ39	DQ35
Y	A8	V _{DD}	A2	V _{SS}	DQ7	V _{DD}	DQ5	V _{SS}
AA	A10	V _{SS}	A13	DQ15	DQ13	V _{SS}	DQ47	DQ43
AB	BG1	A0	PARITY	V _{SS}	DQ11	<u>DM1/DBI1</u>	DQ45	DQ41
AC	A6	V _{DD}	BA1	<u>DQS5</u>	DQS5	V _{DD}	DQ9	V _{SS}
AD	A15/ <u>CAS</u>	V _{SS}	BG0	<u>DQS0</u>	DQS0	V _{SS}	DQ36	DQ34
AE	A14/ <u>WE</u>	<u>CS0</u>	CK0	DQ0	DQ2	<u>DM4/DBI4</u>	DQ38	DQ32
AF	<u>CKE0</u>	V _{DD}	<u>CK0</u>	V _{SS}	DQ6	V _{DD}	DQ4	V _{SS}
AG	V _{TT}	A16/ <u>RAS</u>	ODT0	V _{DD}	V _{SS}	RFU	V _{SS}	V _{DD}

Notes:

1. The pins in blue are not used on this part number. They should be left unconnected.

Routing Guidelines

- Point-to-point connection. All signals should be connected directly from the controller to the MIP unless ECC is used. See the ECC section below for more details on how to route the signals when ECC is used.
- Signal matching should follow the recommendations of the controller for a solder-down device.
- Address/control/command and clock signals should be matched together and referenced to V_{DD} .
- Each data byte should be matched together. Data signals should be referenced to V_{SS} .
- Data byte lanes can be swapped byte to byte. Bit swapping is only allowed at the nibble level.
- Signals on the MIP are 60Ω for single-ended and 100Ω for differential with a tolerance of $\pm 10\%$.
- All termination resistors are already placed on the MIP.
- R_{TT} termination is not required to be placed on the system.
- Decoupling and bulk capacitors placed near the MIP are required for all voltages.
- If Address, Command, Control and Clock signals are referenced to V_{SS} on the system, capacitors must be placed near the powers pins at the address inputs to provide a V_{SS} to V_{DD} return path.
- The voltage rails on the MIP are connected by capacitors as follows:

$V_{DD} - V_{SS}$
 $V_{TT} - V_{DD}$
 $V_{REFCA} - V_{DD}$
 $V_{PP} - V_{SS}$
 $V_{DDSPD} - V_{SS}$

ECC

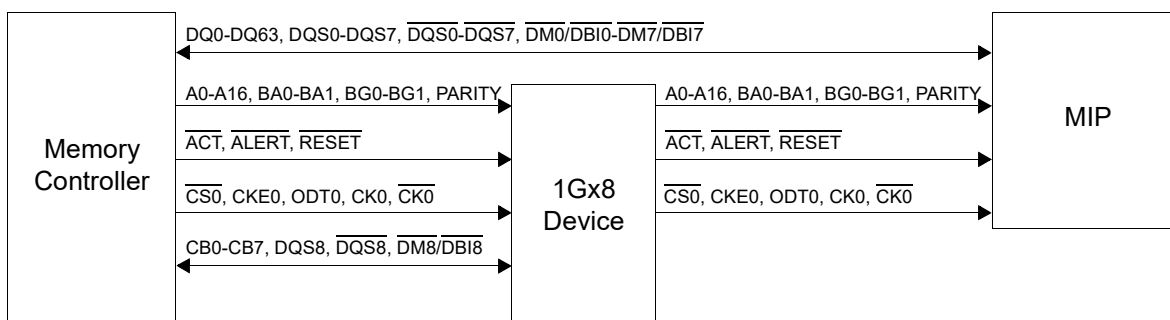
It is possible to use ECC with the MIP. An additional ECC device should be installed on the opposite side of the PCB. See the below image for an example.

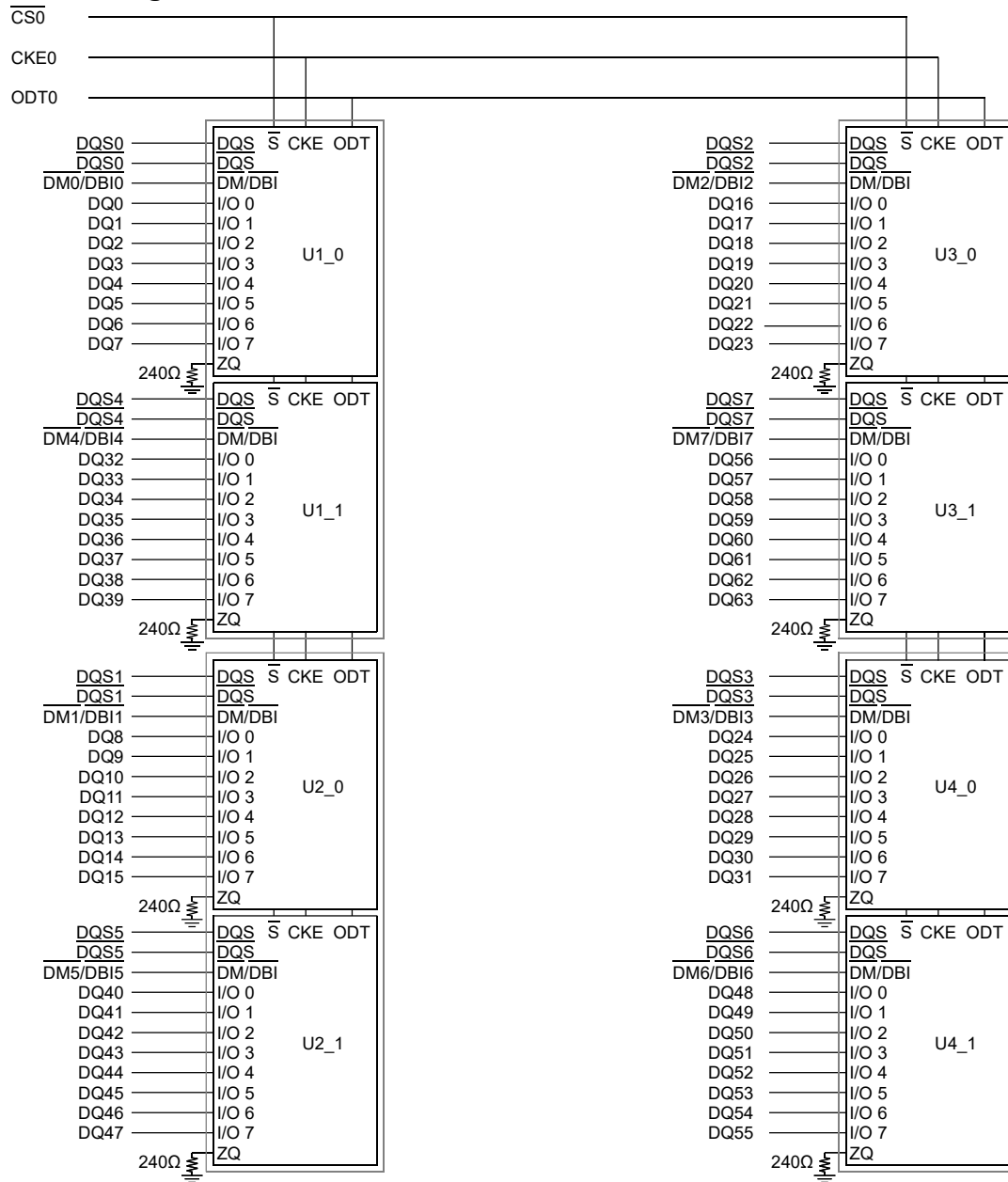


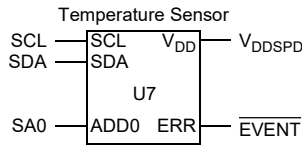
ECC on Opposite Side of the MIP

ECC Block Diagram

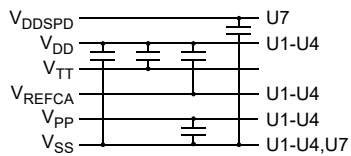
The recommended routing procedure is to connect the controller in a daisy chain fashion first to the ECC device and then to the MIP. Signal matching should follow the above Routing Guidelines.



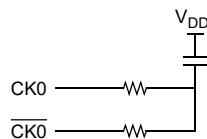
Block Diagram


Block Diagram (Continued)


- A0-A15 → to all SDRAMs (U1-U4)
- WE/A14 → to all SDRAMs (U1-U4)
- CAS/A15 → to all SDRAMs (U1-U4)
- RAS/A16 → to all SDRAMs (U1-U4)
- BG0-BG1 → to all SDRAMs (U1-U4)
- BA0-BA1 → to all SDRAMs (U1-U4)
- ACT → to all SDRAMs (U1-U4)
- ALERT → to ball location B1
- PARITY → to all SDRAMs (U1-U4)
- RESET → to all SDRAMs (U1-U4)
- CS0 → to all SDRAMs (U1-U4)
- ODT0 → to all SDRAMs (U1-U4)
- CKE0 → to all SDRAMs (U1-U4)


Clock Wiring

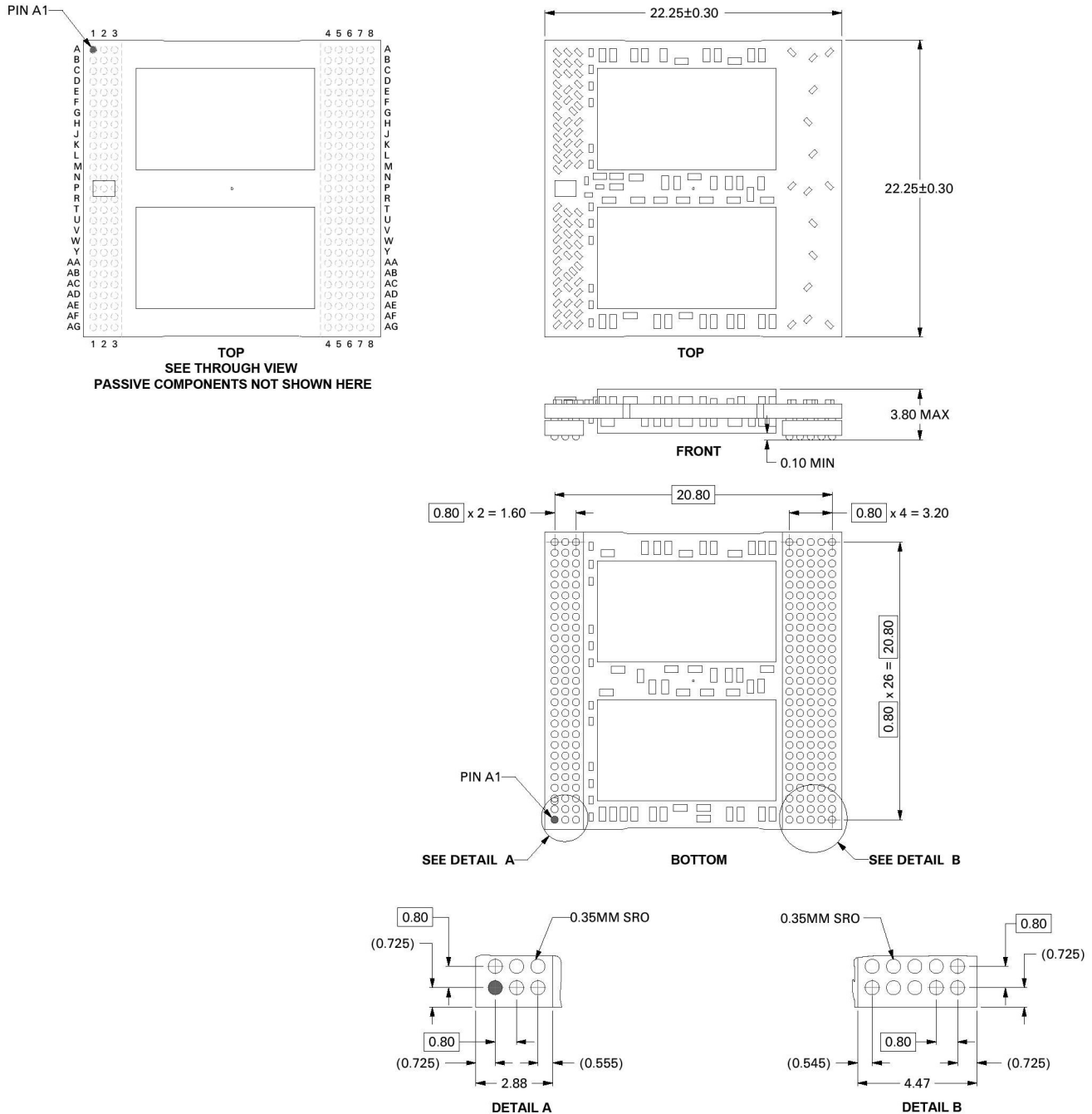
CK Signals	Clock Wiring
CK0/ <u>CK0</u>	4 SDRAMs (U1-U4)


Notes:

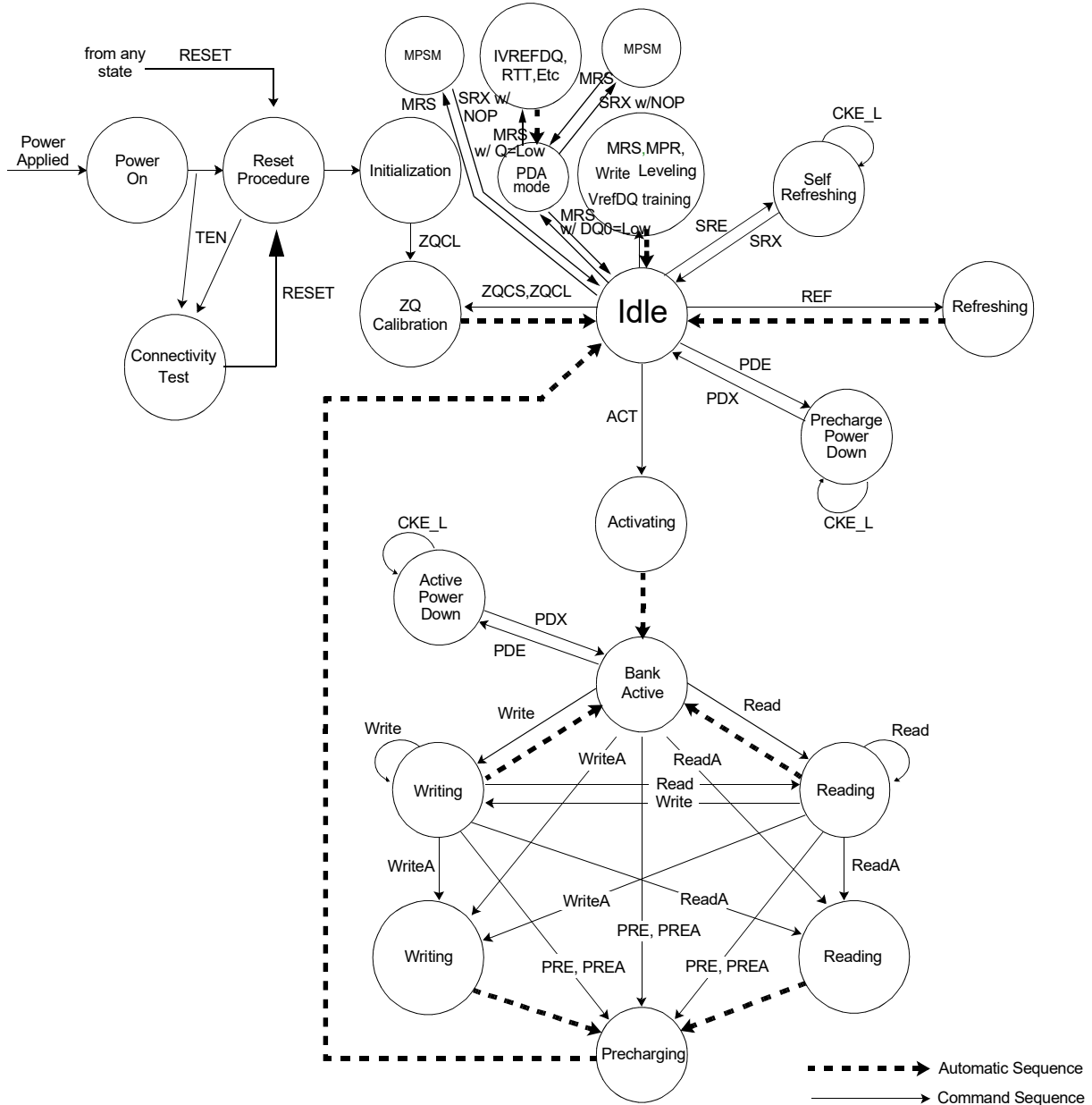
- All address, command and control signal lines are terminated through a series resistor to V_{TT} .
- U_x_0 and U_x_1 represent the lower and upper dies in the DDP U_x . For example, $U1_0$ and $U1_1$ represent lower and upper dies in the DDP U1.
- Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 9.

Physical Dimensions

216-Pin Unbuffered Module in Package (MIP)



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

State Diagram


Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD, RDS4, RDS8	PDE	Enter Power-Down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Enter Power-Down
PREA	Precharge All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh Entry
MRS	Mode Register Set	Write A	WRA, WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh Exit
REF	Refresh, Fine Granularity Refresh	$\overline{\text{RESET}}$	Start RESET Procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

Mode Registers

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13, A11-A9	WR and RTP ^{2, 3}	Write Recovery and Read to Precharge for auto-precharge (See Write Recovery and Read to Precharge (cycles) table)
A8	DLL Reset	0 = No 1 = Yes
A7	TM	0 = Normal 1 = Test
A12, A6-A4, A2	$\overline{\text{CAS}}$ Latency ⁴	(See $\overline{\text{CAS}}$ Latency table)
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1-A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

Notes:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
- WR (write recovery for auto-precharge)min in clock cycles is calculated following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL} .
- The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
- The table only shows the encodings for a given $\overline{\text{CAS}}$ Latency. For actual supported $\overline{\text{CAS}}$ Latencies, please refer to the Speed Bin tables.
- A13 for WR and RTP setting is optional for 4Gb.



Write Recovery and Read to Precharge (Cycles)

A13	A11	A10	A9	WR	RTP
0	0	0	0	10	5
0	0	0	1	12	6
0	0	1	0	14	7
0	0	1	1	16	8
0	1	0	0	18	9
0	1	0	1	20	10
0	1	1	0	24	12
0	1	1	1	22	11
1	0	0	0	26	13
1	0	0	1	Reserved	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved



CAS Latency

A12	A11	A10	A9	WR	CAS Latency
0	0	0	0	0	9
0	0	0	0	1	10
0	0	0	1	0	11
0	0	0	1	1	12
0	0	1	0	0	13
0	0	1	0	1	14
0	0	1	1	0	15
0	0	1	1	1	16
0	1	0	0	0	18
0	1	0	0	1	20
0	1	0	1	0	22
0	1	0	1	1	24
0	1	1	0	0	23
0	1	1	0	1	17
0	1	1	1	0	19
0	1	1	1	1	21
1	0	0	0	0	25
1	0	0	0	1	26
1	0	0	1	0	27
1	0	0	1	1	28
1	0	1	0	0	Reserved for 29
1	0	1	0	1	30
1	0	1	1	0	Reserved for 29
1	0	1	1	1	32
1	1	0	0	0	Reserved

MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff ²	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10-A8	RTT_NOM	(See RTT_NOM table)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6-A5	RFU	0 = must be programmed to 0 during MRS
A4-A3	Additive Latency	00 = 0 (AL disabled) 10 = CL - 2 01 = CL - 1 11 = Reserved
A2-A1	Output Driver Impedance Control	(See Output Driver Impedance Control table)
A0	DLL Enable	0 = Disable ³ 1 = Enable

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR_code setting is inputted, DRAM operation is not defined.
2. Outputs disabled - DQs, DQSs, DQSs.
3. States reversed to "0 as Disable" with respect to DDR4.

RTT_NOM

A11	A10	A9	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
	RFU	0 = must be programmed to 0 during MRS
A11-A9	RTT_WR	(See RTT_WR table)
A8, A2	RFU	0 = must be programmed to 0 during MRS
A7-A6	Low Power Auto Self-Refresh (LP ASR)	00 = Manual Mode (Normal Operating Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self-Refresh)
A5-A3	CAS Write Latency (CWL)	(See CAS Write Latency table)
A1-A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT off
0	0	1	RZQ/2
0	1	0	RZQ/1
0	1	1	Hi-Z
1	0	0	RZQ/3
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CWL (CAS Write Latency)

A5	A4	A3	CWL	Speed Grade in MT/s for 1 t _{CK} Write Preamble		Speed Grade in MT/s for 2 t _{CK} Write Preamble	
0	0	0	9	1600			
0	0	1	10	1866			
0	1	0	11	2133	1600		
0	1	1	12	2400	1866		
1	0	0	14	2666	2133	2400	
1	0	1	16	3200	2400	2666	2400
1	1	0	18		2666	3200	2666
1	1	1	20		3200		3200

Notes:

1. The 2 t_{CK} Write Preamble is valid for DDR4-2400/2666/3200 Speed Grade. For the 2nd Set of 2 t_{CK} Write Preamble, no additional CWL is needed.

MR3

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12-A11	MPR Read Format	00 = Serial 10 = Staggered 01 = Parallel 11 = Reserved Temperature
A10-A9	Write CMD Latency when CRC and DM are enabled	(See Write Command Latency when CRC and DM are both Enabled table)
A8-A6	Fine Granularity Refresh Mode	(See Fine Granularity Refresh Mode table)
A5	Temperature Sensor Readout	0 = Disabled 1 = Enabled
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1-A0	MPR Page Selection	00 = Serial 10 = Staggered 01 = Parallel 11 = Reserved Temperature (See MPR Data Format section)

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

Write Command Latency when CRC and DM are both Enabled

A10	A9	CRC + DM Write Command Latency	Speed Bin (in MT/s)
0	0	4 nCK	1600
0	0	5 nCK	1866, 2133, 2400
0	1	6 nCK	TBD
0	1	RFU	RFU

MPR Data Format
MPR page 0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page 1 (C/A Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-Only
	01 = MPR1	CAS/A15	$\overline{WE}/A14$	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	\overline{ACT}	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS/A16	
	11 = MPR3	CRC Error Status	C/A Parity Error Status	C/A Parity Latency ⁴			C[2]	C[1]	C[0]	
				MR5. A[2]	MR5. A[1]	MR5. A[0]				

Notes:

- MPR used for C/A parity error log readout is enabled by setting A[2] in MR3.
- For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
- If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.
- MPR3 bit 0~2 (C/A parity latency) reflects the latest programmed C/A parity latency values.

MPR page 2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note	
BA1-BA0	00 = MPR0	PPR	sPPR	RTT_WR	Temperature Sensor Status (See table below)		CRC Write Enable	RTT_WR		Read-Only	
		-	-	MR2	-	-	MR2	MR2			
		-	-	A11	-	-	A12	A10	A9		
	01 = MPR1	V _{REF} DQ Training Range	V _{REF} DQ Training Value						Gear-down Enable		
		MR6	MR6						MR3		
		A6	A5	A4	A3	A2	A1	A0	A3		
	10 = MPR2	CAS Latency			RFU		CAS Write Latency				
		MR0						MR2			
		A6	A5	A4	A2	A12	A5	A4	A3		
	11 = MPR3	RTT_NOM			RTT_PARK			Driver Impedance			
		MR1			MR5			MR2			
		A10	A9	A6	A8	A7	A6	A2	A1		

MR bit for Temperature

MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X Refresh ($> t_{REFI}$)
0	1	1X Refresh Rate ($= t_{REFI}$)
1	0	2X Refresh Rate ($1/2 * t_{REFI}$)
1	1	Reserved

MPR page 3 (Vendor Use Only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1-BA0	00 = MPR0	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Read-Only
	01 = MPR1	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	
	10 = MPR2	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	Don't Care	
	11 = MPR3	Don't Care	Don't Care	Don't Care	Don't Care	MAC	MAC	MAC	MAC	

Notes:

- MPR page 3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

MR4

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	PPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self-Refresh Abort	0 = Disable 1 = Enable
A8-A6	\overline{CS} to CMD/ADDR Latency Mode (cycles)	000 = Disable 100 = 6 001 = 3 101 = 8 010 = 4 110 = Reserved 011 = 5 111 = Reserved (See \overline{CS} to CMD/ADDR Latency Mode Setting table)
A5	sPPR	0 = Disable 1 = Enable
A4	Internal V _{REF} Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

Notes:

1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.



$\overline{\text{CS}}$ to CMD/ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	C/A Parity Persistent Error	0 = Disable 1 = Enable
A8-A6	RTT_PARK	(See RTT_PARK table)
A5	ODT Input Buffer during Power Down Mode	0 = ODT Input Buffer is activated 1 = ODT Input Buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2-A0	C/A Parity Latency Mode	(See C/A Parity Latency Mode table)

Notes:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
- When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

C/A Parity Latency Mode

A5	A4	A3	PL	Speed Bin (in MT/s)
0	0	0	Disable	
0	0	1	4	1600, 1866, 2133
0	1	0	5	2400
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

Notes:

1. Parity latency must be programmed according to the timing parameters in the speed grade table.

MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG, BA1-BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW ¹
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12-A10	t _{CCD_L}	(See t _{CCD_L} table)
A9-A8	RFU	0 = must be programmed to 0 during MRS
A7	V _{REFDQ} Training Enable	0 = Disable (Normal Operation Mode) 1 = Enable (Training Mode)
A6	V _{REFDQ} Training Range	(See V _{REFDQ} Training: Range table)
A5-A0	V _{REFDQ} Training Value	(See V _{REFDQ} Training: Values table)

Notes:

- Reserved for Register control word setting. DRAM ignores MR command with BG0, BA1-BA0 = 111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

t_{CCD_L} & t_{DLLK}

A12	A11	A10	t _{CCD_L} min (nCK) ¹	t _{DLLK} min (nCK) ¹	Note
0	0	0	4	597	Data rate ≤ 1333Mbps
0	0	1	5		1333Mbps < Data rate ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	1866Mbps < Data rate ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	≤ TBD
1	0	0	8		≤ TBD
1	0	1	Reserved		
1	1	0			
1	1	1			

Notes:

- t_{CCD_L}/t_{DLLK} should be programmed according to the value defined in AC parameter table per operating frequency.

V_{REFDQ} Training: Range

A6	V _{REFDQ} Range
0	Range 1
1	Range 1

V_{REFDQ} Training: Values

A5-A0	Range 1	Range 2		A5-A0	Range 1	Range 2
00 0000	60.00%	45.00%		01 1010	76.90%	61.90%
00 0001	60.65%	45.65%		01 1011	77.55%	62.55%
00 0010	61.30%	46.30%		01 1100	78.20%	63.20%
00 0011	61.95%	46.95%		01 1101	78.85%	63.85%
00 0100	62.60%	47.60%		01 1110	79.50%	64.50%
00 0101	63.25%	48.25%		01 1111	80.15%	65.15%
00 0110	63.90%	48.90%		10 0000	80.80%	65.80%
00 0111	64.55%	49.55%		10 0001	81.45%	66.45%
00 1000	65.20%	50.20%		10 0010	82.10%	67.10%
00 1001	65.85%	50.85%		10 0011	82.75%	67.75%
00 1010	66.50%	51.50%		10 0100	83.40%	68.40%
00 1011	67.15%	52.15%		10 0101	84.05%	69.05%
00 1100	67.80%	52.80%		10 0110	84.70%	69.70%
00 1101	68.45%	53.45%		10 0111	85.35%	70.35%
00 1110	69.10%	54.10%		10 1000	86.00%	71.00%
00 1111	69.75%	54.75%		10 1001	86.65%	71.65%
01 0000	70.40%	55.40%		10 1010	87.30%	72.30%
01 0001	71.05%	56.05%		10 1011	87.95%	72.95%
01 0010	71.70%	56.70%		10 1100	88.60%	73.60%
01 0011	72.35%	57.35%		10 1101	89.25%	74.25%
01 0100	73.00%	58.00%		10 1110	89.90%	74.90%
01 0101	73.65%	58.65%		10 1111	90.55%	75.55%
01 0110	74.30%	59.30%		11 0000	91.20%	76.20%
01 0111	74.95%	59.95%		11 0001	91.85%	76.85%
01 1000	75.60%	60.60%		11 0010	92.50%	77.50%
01 1001	76.25%	61.25%		11 0011 to 11 1111	Reserved	Reserved

Truth Tables

Command Truth Table

a. Notes 1-4 apply to the entire Command Truth Table.

b. Note 5 applies to all Read/Write command.

 [BG= Bank Group Address, BA= Bank Address, RA= Row Address, CA = Column Address, \overline{BC} = Burst chop, X = Don't care, V = Valid]

Command Truth Table

Function	Abbreviation	CKE		\overline{CS}	\overline{ACT}	$\overline{RAS}/A16$	$\overline{CAS}/A15$	$\overline{WE}/A14$	BG0-BG1	BA0-BA1	C2-C0	$\overline{A12}/\overline{BC}$	A17, A13, A11	A10/AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code			12	
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V		
Self-Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7, 9
Self-Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7, 8, 9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Pre-charge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge All Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address (RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	

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Command Truth Table

Function	Abbreviation	CKE		$\overline{\text{CS}}$	$\overline{\text{ACT}}$	$\overline{\text{RAS/A16}}$	$\overline{\text{CAS/A15}}$	$\overline{\text{WE/A14}}$	BG0-BG1	BA0-BA1	C2-C0	A12/BC	A17, A13, A11	A10/AP	A0-A9	Notes
		Previous Cycle	Current Cycle													
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power-Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power-Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ Calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ Calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

Notes:

- All DDR4 SDRAM commands are defined by states of $\overline{\text{CS}}$, $\overline{\text{ACT}}$, $\overline{\text{RAS/A16}}$, $\overline{\text{CAS/A15}}$, $\overline{\text{WE/A14}}$ and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When $\overline{\text{ACT}} = \text{H}$; pins $\overline{\text{RAS/A16}}$, $\overline{\text{CAS/A15}}$, and $\overline{\text{WE/A14}}$ are used as command pins RAS, CAS, and WE respectively. When $\overline{\text{ACT}} = \text{L}$; pins RAS/A16, CAS/A15, and WE/A14 are used as address pins A16, A15, and A14 respectively
- $\overline{\text{RESET}}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
- Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
- "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
- Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
- The Power Down Mode does not perform any refresh operation.
- The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
- Controller guarantees Self-Refresh exit to be synchronous.
- V_{PP} and $V_{\text{REF}}(V_{\text{REFCA}})$ must be maintained during Self-Refresh operation.
- The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit
- Refer to the CKE Truth Table for more detail with CKE transition.
- During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State ²	CKE		Command (N) ³ RAS, CAS, WE, CS	Action (N) ³	Notes
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	DESELECT	Self-Refresh Exit	8, 12, 16
Bank(s) Activate	H	L	DESELECT	Active Power-Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power-Down Entry	11, 13, 14, 18
	H	L	REFRESH	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on page 31.					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to t_{CKEmin} being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the t_{Xs} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are DESELECT only.
12. Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.
13. Self-Refresh can not be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. V_{PP} and V_{REFCA} must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. 'Idle state' is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{Xs}, t_{XP}, etc.)

Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as $t_{CKAVGmin}$ are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like t_{AAmin} , t_{RCDmin} , etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

$$nCK = \text{ceiling} [(parameter_in_ns / application_t_{CK_in_ns}) - 0.025]$$

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

$$nCK = \text{truncate} [\{ (parameter_in_ps \times 1000) / (application_t_{CK_in_ps}) + 974 \} / 1000]$$

- Either algorithm yields identical results.

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-0.3 ~ 1.5	V	1, 3
V_{PP}	Voltage on V_{PP} relative to V_{SS}	-0.3 ~ 3.0	V	1, 4
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.3 ~ 1.5	V	1
V_{DDSPD}	Voltage on V_{DDSPD} relative to V_{SS}	-0.5 ~ 4	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Notes:

- Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM.
- V_{REF} must be not greater than $0.6 * V_{DD}$. When V_{DD} is less than 500 mV, V_{REF} may be less than or equal to 300 mV.
- V_{PP} must be equal or greater than V_{DD} at all times.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min	Typical	Max		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1, 2
V_{PP}	Supply Voltage for Output	2.375	2.5	2.75	V	1
V_{DDSPD}	Temperature Sensor Supply Voltage	1.4	2.5 or 3.3	3.6	V	
V_{TT}	Termination Voltage	0.57	0.6	0.63	V	2
V_{SS}	Ground	0	0	0	V	

Notes:

- DC bandwidth is limited to 20MHz.
- $V_{TT} = V_{DD}/2$

Operating Temperature Range

Symbol	Parameter	Range	Units	Notes
T _{OPER}	Normal Operating Temperature Range (Case)	0 to 85	°C	1, 2
	Extended Operating Temperature Range (Case)	85 to 95	°C	1, 3

Notes:

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 °C and 85 °C under all operating conditions.
- Some applications require operation in the Extended Temperature Range between 85 °C and 95 °C. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the Extended Temperature Range.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and Extended Temperature Range.

Temperature Sensor Characteristics

Symbol	Test Condition	Min	Typical	Max	Units
Range		-40	-	125	°C
Accuracy	-25 °C to 85 °C	-	±0.5	±2	°C
	-40 °C to 125 °C	-	±1	±3	°C
Resolution		-	0.0625	-	°C
Conversion Time ¹	Worst Case Conversion Time	-	26	35	ms

Notes:

- Using a 12-bit resolution.

Refresh Parameters

Parameter	Symbol	8Gb	Units
Average periodic refresh interval	t _{REFI}	7.8	µs
		3.9	µs

Differential AC and DC Input Levels for CK- $\overline{\text{CK}}$

Symbol	Parameter	DDR4-2666		Units	Notes
		Min	Max		
V_{IHDIFF}	Differential input logic high	TBD	Note 3	V	1
V_{ILDIFF}	Differential input logic high	Note 3	TBD	V	1
$V_{\text{IHDIFF}}(\text{AC})$	AC input logic high	$2 * (V_{\text{IH}}(\text{AC}) - V_{\text{REF}})$	Note 3	V	2
$V_{\text{ILDIFF}}(\text{AC})$	AC input logic low	Note 3	$2 * (V_{\text{IL}}(\text{AC}) - V_{\text{REF}})$	V	2

Notes:

- Used to define a differential signal slew-rate.
- For CK/CK, use $V_{\text{IH}}/V_{\text{IL}}(\text{AC})$ of ADD/CMD and V_{REFCA} .
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, need to be within the respective limits ($V_{\text{IH}}(\text{DC})$ max, $V_{\text{IL}}(\text{DC})$ min) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-Ended Levels for CK- $\overline{\text{CK}}$

Symbol	Parameter	DDR4-2666		Units	Notes
		Min	Max		
V_{SEH}	Single-ended high-level for CK- $\overline{\text{CK}}$	TBD	Note 3	V	1, 2
V_{SEL}	Single-ended low-level for CK- $\overline{\text{CK}}$	Note 3	TBD	V	1, 2

Notes:

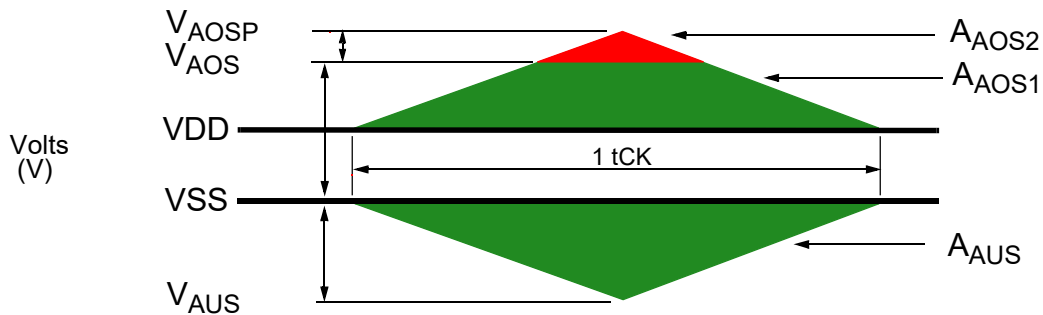
- For CK/CK, use $V_{\text{IH}}/V_{\text{IL}}(\text{AC})$ of ADD/CMD.
- $V_{\text{IH}}(\text{AC})/V_{\text{IL}}(\text{AC})$ for ADD/CMD is based on V_{REFCA} .
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, need to be within the respective limits ($V_{\text{IH}}(\text{DC})$ max, $V_{\text{IL}}(\text{DC})$ min) for single-ended signals as well as the limitations for overshoot and undershoot.

AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	Symbol	DDR4-2666	Units	Notes
Maximum peak amplitude above V_{AOS}	V_{AOSP}	0.06	V	
Upper boundary of overshoot area A_{AOS1}	V_{AOS}	$V_{DD} + 0.24$	V	1
Maximum peak amplitude allowed for undershoot	V_{AUS}	0.30	V	
Maximum overshoot area per 1 t_{CK} above V_{AOS}	A_{AOS2}	0.0055	V-ns	
Maximum overshoot area per 1 t_{CK} between V_{DD} and V_{AOS}	A_{AOS1}	0.1699	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{AUS}	0.1762	V-ns	
(A0-A13, A17, BG0-BG1, BA0-BA1, ACT, RAS/A16, CAS/A15, WE/A14, CS, CKE, ODT, C0-C2)				

Notes:

- The value of V_{AOS} matches V_{DD} absolute max as defined in the Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{AOS} remains at V_{DD} absolute max as defined in the Absolute Maximum DC Ratings.

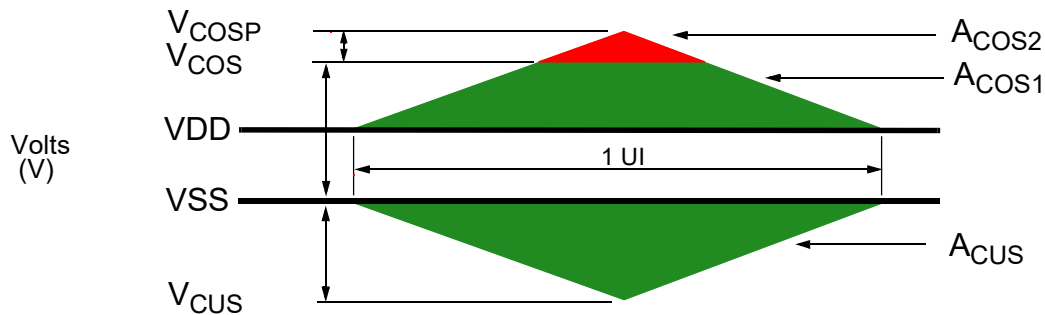


AC Overshoot/Undershoot Specification for Clock

Parameter	Symbol	DDR4-2666	Units	Notes
Maximum peak amplitude above V_{COS}	V_{COSP}	0.06	V	
Upper boundary of overshoot area A_{COS1}	V_{COS}	$V_{DD} + 0.24$	V	1
Maximum peak amplitude allowed for undershoot	V_{CUS}	0.30	V	
Maximum overshoot area per 1 UI above V_{COS}	A_{COS2}	0.0025	V-ns	
Maximum overshoot area per 1 UI between V_{DD} and V_{COS}	A_{COS1}	0.0750	V-ns	
Maximum undershoot area per 1 UI below V_{SS}	A_{CUS}	0.0762	V-ns	
(CK, CK)				

Notes:

- The value of V_{COS} matches V_{DD} absolute max as defined in the Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{COS} remains at V_{DD} absolute max as defined in the Absolute Maximum DC Ratings.



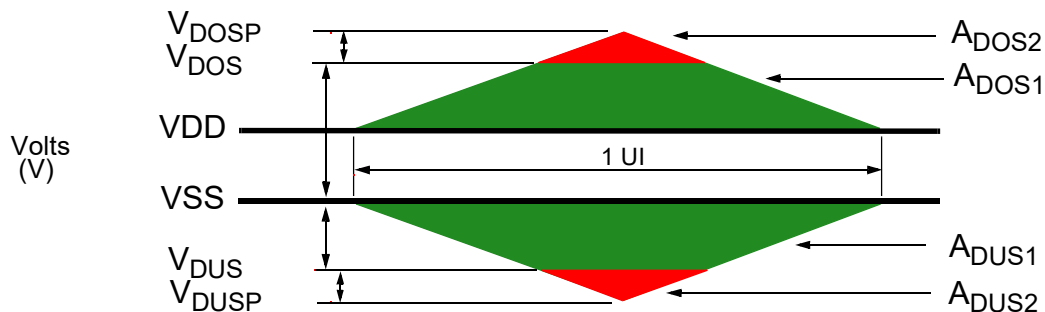
AC Overshoot/Undershoot Specification for Data, Strobe and Mask

Parameter	Symbol	DDR4-2666	Units	Notes
Maximum peak amplitude above V_{AOS}	V_{DOSP}	0.16	V	
Upper boundary of overshoot area A_{DOS1}	V_{DOS}	$V_{DD} + 0.24$	V	1
Maximum peak amplitude allowed for undershoot	V_{DUS}	0.30	V	2
Maximum peak amplitude allowed for undershoot	V_{DUSP}	0.10	V	
Maximum overshoot area per 1 t_{CK} above V_{AOS}	A_{DOS2}	0.0100	V-ns	
Maximum overshoot area per 1 t_{CK} between V_{DD} and V_{AOS}	A_{DOS1}	0.0700	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{DUS1}	0.0700	V-ns	
Maximum undershoot area per 1 t_{CK} below V_{SS}	A_{DUS2}	0.0100	V-ns	

(DQ, CB, DQS, DQS, DM, DBI, TDQS, TDQS)

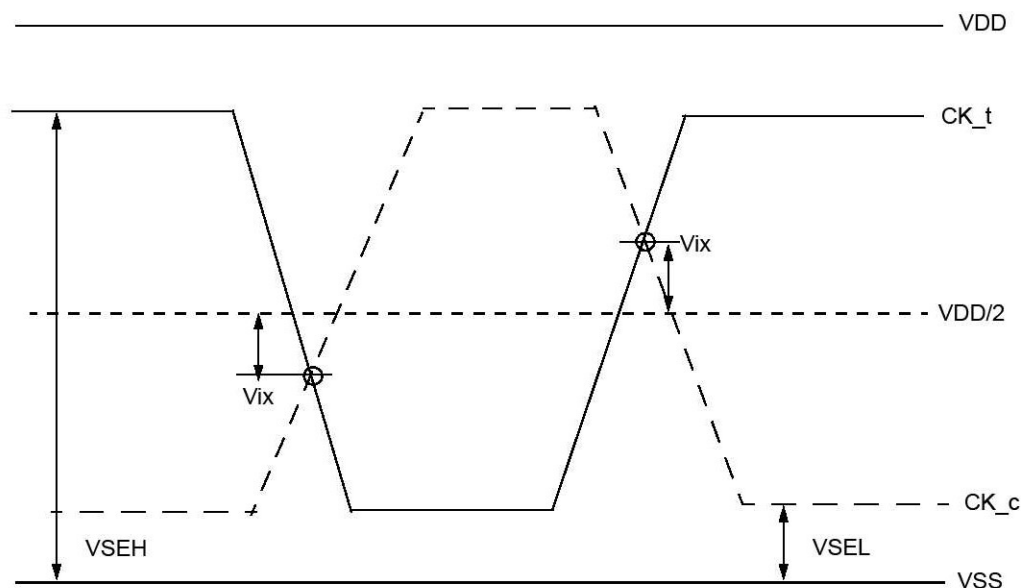
Notes:

- The value of V_{DOS} matches (V_{IN}, V_{OUT}) max as defined in the Absolute Maximum DC Ratings if V_{DD} equals V_{DD} max as defined in the Recommended DC Operating Conditions. If V_{DD} is above the recommended operating conditions, V_{DOS} remains at (V_{IN}, V_{OUT}) max as defined in the Absolute Maximum DC Ratings.
- The value of V_{DUS} matches (V_{IN}, V_{OUT}) min as defined in the Absolute Maximum DC Ratings.



Cross Point Voltage for Differential Input Signals (CK- $\overline{\text{CK}}$)

Symbol	Parameter	DDR4-2666			
		Min		Max	
	Area of V_{SEH} , V_{SEL}	TBD	TBD	TBD	TBD
$V_{\text{IX}}(\text{CK})$	Differential Input Cross Point Voltage relative to $V_{\text{DD}}/2$ for CK, $\overline{\text{CK}}$	TBD	TBD	TBD	TBD



Single-Ended AC & DC Output Levels

Symbol	Parameter	DDR4-2666	Units	Notes
V _{OH} (DC)	DC output high measurement level (for IV curve linearity)	1.1 * V _{DD}	V	
V _{OM} (DC)	DC output mid measurement level (for IV curve linearity)	0.8 * V _{DD}	V	
V _{OL} (DC)	DC output low measurement level (for IV curve linearity)	0.5 * V _{DD}	V	
V _{OH} (AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) * V _{DD}	V	1
V _{OL} (AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) * V _{DD}	V	1

Notes:

- The swing of $\pm 0.15 * V_{DD}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DD}$.

Differential AC & DC Output Levels

Symbol	Parameter	DDR4-2666	Units	Notes
		Min		
V _{OHdiff} (AC)	AC differential output high measurement level (for output SR)	0.3 * V _{DD}	V	1
V _{OLdiff} (AC)	AC differential output low measurement level (for output SR)	-0.3 * V _{DD}	V	1

Notes:

- The swing of $\pm 0.3 * V_{DD}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of $RZQ/7\Omega$ and an effective test load of 50Ω to $V_{TT} = V_{DD}$ at each of the differential outputs.

Device Standard Speed Bins
DDR4-2666 Speed Bins

Speed Bin			DDR4-2666		Units	Notes	
CL - nRCD - nRP			19-19-19				
Parameter	Symbol		Min	Max			
Internal read command to first data	t_{AA}		13.75	18	ns	7	
Internal read command to first data with read DBI enabled	t_{AA_DBI}		$t_{AA}(\min) + 3nCK$	$t_{AA}(\max) + 3nCK$	ns	7	
ACT to internal read or write delay time	t_{RCD}		13.75	-	ns	7	
PRE command period	t_{RP}		13.75	-	ns	7	
ACT to ACT or REF command period	t_{RC}		45.75	-	ns	7	
ACT to PRE command period	t_{RAS}		32	$9 * t_{REFI}$	ns	7	
	Normal	Read DBI	$t_{CK(avg)}$				
CWL = 9	CL = 9	CL = 11	$t_{CK(avg)}$	Reserved		ns	4
	CL = 10	CL = 12		1.5	1.6	ns	1, 2, 3, 5, 6, 8
CWL = 9, 11	CL = 10	CL = 12	$t_{CK(avg)}$	Reserved		ns	4
	CL = 11	CL = 13		1.25	< 1.5	ns	1, 2, 3, 5
	CL = 12	CL = 14		1.25	< 1.5	ns	1, 2, 3, 5
CWL = 10, 12	CL = 12	CL = 14	$t_{CK(avg)}$	Reserved		ns	4
	CL = 13	CL = 15		1.071	< 1.25	ns	1, 2, 3, 5
	CL = 14	CL = 16		1.071	< 1.25	ns	1, 2, 3, 5
CWL = 11, 14	CL = 14	CL = 17	$t_{CK(avg)}$	Reserved		ns	4
	CL = 15	CL = 18		0.937	< 1.071	ns	1, 2, 3, 5
	CL = 16	CL = 19		0.937	< 1.071	ns	1, 2, 3, 5
CWL = 12, 16	CL = 15	CL = 18	$t_{CK(avg)}$	Reserved		ns	4
	CL = 16	CL = 19		Reserved		ns	4
	CL = 17	CL = 20		0.833	< 0.937	ns	1, 2, 3
	CL = 18	CL = 21		0.833	< 0.937	ns	1, 2, 3
Supported CL Settings			10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20		n_{CK}		
Supported CL Settings with read DBI			12, 13, 14, 15, 16, 18, 19, 20, 21, 22, 23		n_{CK}		
Supported CWL Settings			9, 10, 11, 12, 14, 16, 18		n_{CK}		

Speed Bin Tables Notes

Absolute Specification

- $V_{DD} = 1.20V \pm 0.06 V$

- $V_{PP} = 2.5V +0.25/-0.125 V$

- The values defined with the above mentioned table are the case where DLL ON.

- DDR4-2400 Speed Bin Table is valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in $t_{CK(avg)min}$ and $t_{CK(avg)max}$ requirements. When making a selection of $t_{CK(avg)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(avg)min}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. CL in clock cycle is calculated from t_{AA} following Rounding Algorithm section
3. $t_{CK(avg)max}$ limits: Calculate $t_{CK(avg)} = t_{AAmax} / CL \text{ SELECTED}$ and round the resulting $t_{CK(avg)}$ down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.937 ns or 0.833 ns). This result is $t_{CK(avg)max}$ corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
7. Parameters apply from $t_{CK(avg)min}$ to $t_{CK(avg)max}$ at all standard JEDEC clock period values as stated in the Speed Bin Tables.
8. DDR4 SDRAM supports CL = 9 as long as a system meets $t_{AA}(min)$.

Device Timing Parameters by Speed Bin

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Clock Timing					
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL_OFF)}$	8	20	ns	
Average Clock Period	$t_{CK(avg)}$	0.833	<0.937	ns	35, 36
Average HIGH Pulse Width	$t_{CH(avg)}$	0.48	0.52	$t_{CK(avg)}$	
Average LOW Pulse Width	$t_{CL(avg)}$	0.48	0.52	$t_{CK(avg)}$	
Absolute Clock Period	$t_{CK(abs)}$	$t_{CK(avg)min} + t_{JIT(per_tot)min}$	$t_{CK(avg)max} + t_{JIT(per_tot)max}$	$t_{CK(avg)}$	
Absolute Clock HIGH Pulse Width	$t_{CH(abs)}$	0.45	-	$t_{CK(avg)}$	23
Absolute Clock LOW Pulse Width	$t_{CL(abs)}$	0.45	-	$t_{CK(avg)}$	24
Clock Period Jitter - Total	$t_{JIT(per_tot)}$	-42	42	ps	25
Clock Period Jitter - Deterministic	$t_{JIT(per_dj)}$	-21	21	ps	26
Clock Period Jitter during DLL Locking Period	$t_{JIT(per, lck)}$	-33	33	ps	
Cycle to Cycle Period Jitter	$t_{JIT(CC)}$	-	83	ps	
Cycle to Cycle Period Jitter during DLL Locking Period	$t_{JIT(CC, lck)}$	-	67	ps	
Duty Cycle Jitter	$t_{JIT(duty)}$	TBD	TBD	ps	
Cumulative Error across 2 Cycles	$t_{ERR(2per)}$	-61	61	ps	
Cumulative Error across 3 Cycles	$t_{ERR(3per)}$	-73	73	ps	
Cumulative Error across 4 Cycles	$t_{ERR(4per)}$	-81	81	ps	
Cumulative Error across 5 Cycles	$t_{ERR(5per)}$	-87	87	ps	
Cumulative Error across 6 Cycles	$t_{ERR(6per)}$	-92	92	ps	
Cumulative Error across 7 Cycles	$t_{ERR(7per)}$	-97	97	ps	
Cumulative Error across 8 Cycles	$t_{ERR(8per)}$	-101	101	ps	
Cumulative Error across 9 Cycles	$t_{ERR(9per)}$	-104	104	ps	
Cumulative Error across 10 Cycles	$t_{ERR(10per)}$	-107	107	ps	
Cumulative Error across 11 Cycles	$t_{ERR(11per)}$	-110	110	ps	
Cumulative Error across 12 Cycles	$t_{ERR(12per)}$	-112	112	ps	
Cumulative Error across 13 Cycles	$t_{ERR(13per)}$	-114	114	ps	
Cumulative Error across 14 Cycles	$t_{ERR(14per)}$	-116	116	ps	
Cumulative Error across 15 Cycles	$t_{ERR(15per)}$	-118	118	ps	
Cumulative Error across 16 Cycles	$t_{ERR(16per)}$	-120	120	ps	
Cumulative Error across 17 Cycles	$t_{ERR(17per)}$	-122	122	ps	

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Cumulative Error across 18 Cycles	$t_{ERR(18per)}$	-124	124	ps	
Cumulative Error across n = 19-50 Cycles	$t_{ERR(nper)}$	$((1 + 0.68\ln(n)) * t_{JIT(per_tot)min})$	$((1 + 0.68\ln(n)) * t_{JIT(per_tot)max})$	ps	
Command and Address Setup Time to CK, CK Referenced to $V_{IH(AC)} / V_{IL(AC)}$ Levels	$t_{IS(base)}$	62	-	ps	
Command and Address Setup Time to CK, CK Referenced to V_{REF} Levels	$t_{IS(Vref)}$	162	-	ps	
Command and Address Hold Time to CK, CK Referenced to $V_{IH(DC)} / V_{IL(DC)}$ Levels	$t_{IH(base)}$	87	-	ps	
Command and Address Hold Time to CK, CK Referenced to V_{REF} Levels	$t_{IH(Vref)}$	162	-	ps	
Control and Address Input Pulse Width for Each Input	t_{IPW}	410	-	ps	
Command and Address Timing					
\overline{CAS} to \overline{CAS} Command Delay for Same Bank Group	t_{CCD_L}	Max(5nCK, 5ns)	-	nCK	34
\overline{CAS} to \overline{CAS} Command Delay for Different Bank Group	t_{CCD_S}	4	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 2 KB Page Size	$t_{RRD_S(2K)}$	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 1 KB Page Size	$t_{RRD_S(1K)}$	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Different Bank Group for 1/2 KB Page Size	$t_{RRD_S(1/2K)}$	Max(4nCK, 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 2 KB Page Size	$t_{RRD_L(2K)}$	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 1 KB Page Size	$t_{RRD_L(1K)}$	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command Delay to Same Bank Group for 1/2 KB Page Size	$t_{RRD_L(1/2K)}$	Max(4nCK, 4.9ns)	-	nCK	34
Four Activate Window for 2 KB Page Size	$t_{FAW(2K)}$	Max(28nCK, 30ns)	-	ns	34
Four Activate Window for 1 KB Page Size	$t_{FAW(1K)}$	Max(20nCK, 21ns)	-	ns	34
Four Activate Window for 1/2 KB Page Size	$t_{FAW(1/2K)}$	Max(16nCK, 13ns)	-	ns	34
Delay from Start of Internal Write Transaction to Internal READ Command for Same Bank Group	t_{WTR_S}	Max(2nCK, 2.5ns)	-	ns	1, 2, 34
Delay from Start of Internal Write Transaction to Internal READ Command for Different Bank Group	t_{WTR_L}	Max(4nCK, 7.5ns)	-	ns	1, 34
Internal READ Command to PRECHARGE Command Delay	t_{RTP}	Max(4nCK, 7.5ns)	-	ns	34

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
WRITE Recovery Time	t_{WR}	15	-	ns	1
WRITE Recovery Time when Both CRC and DM are Enabled	$t_{WR_CRC_DM}$	$t_{WR} + \text{Max}(5nCK, 3.75ns)$	-	ns	1, 28
Delay from Start of Internal Write Transaction to Internal READ Command for Same Bank Group when Both CRC and DM are Enabled	$t_{WTR_S_CRC_DM}$	$t_{WTR_S} + \text{Max}(5nCK, 3.75ns)$	-	ns	2, 29, 34
Delay from Start of Internal Write Transaction to Internal READ Command for Different Bank Group when Both CRC and DM are Enabled	$t_{WTR_L_CRC_DM}$	$t_{WTR_L} + \text{Max}(5nCK, 3.75ns)$	-	ns	3, 30, 34
DLL locking time	t_{DLLK}	768	-	nCK	
Mode Register Set Command Cycle Time	t_{MRD}	8	-	nCK	
Mode Register Set Command Update Delay	t_{MOD}	$\text{Max}(24nCK, 15ns)$	-	nCK	50
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	nCK	33
Multi-Purpose Register Write Recovery Time	t_{WR_MPR}	$t_{MODmin} + AL + PL$	-	nCK	
Auto Precharge Write Recovery Time + Precharge Time	t_{DAL}	Programmed WR + roundup ($t_{RP} / t_{CK(avg)}$)	-	nCK	
DQ0 or DQL0 Driven to 0 Setup Time to First DQS Rising Edge	t_{PDA_S}	0.5	-	UI	45, 47
DQ0 or DQL0 Driven to 0 Hold Time from Last DQS Falling Edge	t_{PDA_H}	0.5	-	UI	46, 47
CS to Command Address Latency					
\overline{CS} to Command Address Latency	t_{CAL}	$\text{Max}(3nCK, 3.748ns)$	-	nCK	
Mode Register Set Command Cycle Time in CAL Mode	t_{MRD_tCAL}	$t_{MOD} + t_{CAL}$	-	nCK	
Mode Register Set Update Delay in CAL Mode	t_{MOD_tCAL}	$t_{MOD} + t_{CAL}$	-	nCK	
DRAM Data Timing					
DQS, \overline{DQS} to DQ Skew, Per Group, Per Access	t_{DQSQ}	-	0.17	UI	13, 18, 39, 49
DQ Output Hold Time from DQS, \overline{DQS}	t_{QH}	0.74	-	UI	13, 17, 18, 39, 49
Data Valid Window per Device per UI: ($t_{QH} - t_{DQSQ}$) of Each UI on a Given DRAM	t_{DVWd}	0.64	-	UI	17, 18, 39, 49
Data Valid Window per Pin per UI: ($t_{QH} - t_{DQSQ}$) Each UI on a Pin of a Given DRAM	t_{DVWp}	0.72	-	UI	17, 18, 39, 49

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
DQS, $\overline{\text{DQS}}$ Low-Impedance Time from CK, $\overline{\text{CK}}$	$t_{LZ(DQ)}$	-330	175	ps	39
DQS, $\overline{\text{DQS}}$ High-Impedance Time from CK, $\overline{\text{CK}}$	$t_{HZ(DQS)}$	-	175	ps	39
Data Strobe Timing					
DQS, $\overline{\text{DQS}}$ Differential READ Preamble (1 Clock)	t_{RPRE}	0.9	Note 44	t_{CK}	39, 40
DQS, $\overline{\text{DQS}}$ Differential READ Preamble (2 Clock)	t_{RPRE2}	1.8	Note 44	t_{CK}	39, 41
DQS, $\overline{\text{DQS}}$ Differential READ Postamble	t_{RPST}	0.33	Note 45	t_{CK}	39
DQS, $\overline{\text{DQS}}$ Differential Output High Time	t_{QSH}	0.4	-	t_{CK}	21, 39
DQS, $\overline{\text{DQS}}$ Differential Output Low Time	t_{QSL}	0.4	-	t_{CK}	20, 39
DQS, $\overline{\text{DQS}}$ Differential WRITE Preamble (1 Clock)	t_{WPRE}	0.9	-	t_{CK}	42
DQS, $\overline{\text{DQS}}$ Differential WRITE Preamble (2 Clock)	t_{WPRE2}	1.8	-	t_{CK}	43
DQS, $\overline{\text{DQS}}$ Differential WRITE Postamble	t_{WPST}	0.33	-	t_{CK}	
DQS, $\overline{\text{DQS}}$ Low-Impedance Time (Referenced from RL-1)	$t_{LZ(DQS)}$	-330	175	t_{CK}	39
DQS, $\overline{\text{DQS}}$ High-Impedance Time (Referenced from RL+BL/2)	$t_{HZ(DQS)}$	-	175	t_{CK}	39
DQS, $\overline{\text{DQS}}$ Differential Input Low Pulse Width	t_{DQSL}	0.46	0.54	t_{CK}	
DQS, $\overline{\text{DQS}}$ Differential Input High Pulse Width	t_{DQSH}	0.46	0.54	t_{CK}	
DQS, $\overline{\text{DQS}}$ Rising Edge to CK, $\overline{\text{CK}}$ Rising Edge (1 Clock Preamble)	t_{DQSS}	-0.27	0.27	t_{CK}	42
DQS, $\overline{\text{DQS}}$ Rising Edge to CK, $\overline{\text{CK}}$ Rising Edge (2 Clock Preamble)	t_{DQSS2}	TBD	TBD	t_{CK}	43
DQS, $\overline{\text{DQS}}$ Falling Edge Setup Time from CK, $\overline{\text{CK}}$ Rising Edge	t_{DSS}	0.18	-	t_{CK}	
DQS, $\overline{\text{DQS}}$ Falling Edge Hold Time from CK, $\overline{\text{CK}}$ Rising Edge	t_{DSH}	0.18	-	t_{CK}	
DQS, $\overline{\text{DQS}}$ Rising Edge Output Timing Location from Rising CK, $\overline{\text{CK}}$ with DLL On Mode	t_{DQSCK} (DLL On)	-175	175	ps	37, 38, 39
DQS, $\overline{\text{DQS}}$ Rising Edge Output Variance Window per DRAM	t_{DQSCKI} (DLL On)	-	290	ps	37, 38, 39
MPSM Timing					
Command Path Disable Delay upon MPSM Entry	t_{MPED}	$t_{MODmin} + t_{CPDEDmin}$	-		
Valid Clock Requirement after MPSM Entry	t_{CKMPE}	$t_{MODmin} + t_{CPDEDmin}$	-		
Valid Clock Requirement before MPSM Exit	t_{CKMPX}	$t_{CKSRXmin}$	-		
Exit MPSM to Commands not Requiring a Locked DLL	t_{XMP}	t_{XSmin}	-		

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Exit MPSM to Commands Requiring a Locked DLL	t_{XMPDLL}	$t_{XMPmin} + t_{XSDLLmin}$	-		
CS Setup Time to CKE	t_{MPX_S}	$t_{Smin} + t_{Hmin}$	-		
Calibration Timing					
Power-up and \overline{RESET} Calibration Time	t_{ZQinit}	1024	-	nCK	
Normal Operation Full Calibration Time	t_{ZQoper}	512	-	nCK	
Normal Operation Short Calibration Time	t_{ZQCS}	128	-	nCK	
RESET/Self-Refresh Timing					
Exit \overline{RESET} from CKE HIGH to a Valid Command	t_{XPR}	Max(5nCK, $t_{RFCmin} + 10ns$)	-	nCK	
Exit Self-Refresh to Commands not Requiring a Locked DLL	t_{XS}	$t_{RFCmin} + 10ns$	-	nCK	
SRX to Commands not Requiring a Locked DLL in Self-Refresh ABORT	t_{XS_ABORT}	$t_{RFC4min} + 10ns$	-	nCK	
Exit Self-Refresh to ZQCL, ZQCS and MRS (CL, CWL, WL, RTP and Geardown)	t_{XS_FAST}	$t_{RFC4min} + 10ns$	-	nCK	
Exit Self Refresh from to Commands Requiring a Locked DLL	t_{XSDLL}	$t_{DLLkmin}$	-	nCK	
Minimum CKE Low Width for Self-Refresh Entry to Exit Timing	t_{CKESR}	$t_{CKEmin} + 1nCK$	-	nCK	
Minimum CKE Low Width for Self-Refresh Entry to Exit Timing with CA Parity Enabled	t_{CKESR_PAR}	$t_{CKEmin} + 1nCK + PL$	-	nCK	
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	Max(5nCK, 10ns)	-	nCK	
Valid Clock Requirement after Self-Refresh Entry (SRE) or Power-Down Entry (PDE) when CA Parity us Enabled	t_{CKSRE_PAR}	Max(5nCK, 10ns) + PL	-	nCK	
Valid Clock Requirement before Self-Refresh Exit (SRX) or Power-Down Exit (PDX) or \overline{RESET} Exit	t_{CKSRX}	Max(5nCK, 10ns)	-	nCK	
Power Down Timing					
Exit Power Down with DLL on to any Valid Command; Exit Precharge Power Down with DLL Frozen to Commands not Requiring a Locked DLL	t_{XP}	Max(4nCK, 6ns)	-	nCK	
CKE Minimum Pulse Width	t_{CKE}	Max(3nCK, 5ns)	-	nCK	31, 32
Command Pass Disable Delay	t_{CPDED}	4	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKEmin}	$9 * t_{REFI}$	nCK	6
Timing of ACT Command to Power Down Entry	$t_{ACTPDEN}$	2	-	nCK	7
Timing of PRE or PREA Command to Power Down Entry	t_{PRPDEN}	2	-	nCK	7

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Timing of RD/RDA Command to Power Down Entry	t_{RDPDEN}	RL + 4 + 1	-	nCK	
Timing of WR Command to Power Down Entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + ($t_{WR} / t_{CK(avg)}$)	-	nCK	4
Timing of WRA Command to Power Down Entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	nCK	5
Timing of WR Command to Power Down Entry (BC4MRS)	$t_{WRPBC4DEN}$	WL + 2 + ($t_{WR} / t_{CK(avg)}$)	-	nCK	4
Timing of WRA Command to Power Down Entry (BC4MRS)	$t_{WRAPBC4DEN}$	WL + 2 + WR + 1	-	nCK	5
Timing of REF Command to Power Down Entry	$t_{REFPDEN}$	2	-	nCK	7
Timing of MRS Command to Power Down Entry	$t_{MRSPDEN}$	t_{MODmin}	-	nCK	
PDA Timing					
Mode Register Set Command Cycle Time in PDA Mode	t_{MRD_PDA}	Max(16nCK, 10ns)	-	nCK	
Mode Register Set Command Update Delay in PDA Mode	t_{MOD_PDA}	t_{MOD}		nCK	
ODT Timing					
Asynchronous RTT Turn-On Delay (Power Down with DLL Frozen)	t_{AONAS}	1	9	ns	
Asynchronous RTT Turn-Off Delay (Power Down with DLL Frozen)	t_{AOFAS}	1	9	ns	
RTT Dynamic Change Skew	t_{ADC}	0.3	0.7	$t_{CK(avg)}$	
Write Leveling Timing					
First DQS/ \overline{DQS} Rising Edge after Write Leveling Mode is Programmed	t_{WLMRD}	40	-	nCK	12
DQS/ \overline{DQS} Delay after Write Leveling Mode is Programmed	$t_{WLDQSEN}$	25	-	nCK	12
Write Leveling Setup Time from Rising CK, \overline{CK} Crossing to Rising DQS, \overline{DQS} Crossing	t_{WLS}	0.13	-	$t_{CK(avg)}$	
Write Leveling Hold Time from Rising CK, \overline{CK} Crossing to Rising DQS, \overline{DQS} Crossing	t_{WLH}	0.13	-	$t_{CK(avg)}$	
Write Leveling Output Delay	t_{WLO}	0	9.5	ns	
Write Leveling Output Error	t_{WLOE}	0	2	ns	
CA Parity Timing					
Commands not Guaranteed to be Executed during this Time	$t_{PAR_UNKNOWN}$	-	PL	nCK	
Delay from Errant Command to \overline{ALERT} Assertion	$t_{PAR_ALERT_ON}$	-	PL + 6ns	nCK	
Pulse Width of \overline{ALERT} Signal when Asserted	$t_{PAR_ALERT_PW}$	72	144	nCK	

Device Timing Parameters by Speed Bin (Continued)

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Time from when ALERT is Asserted until Controller Must Start Providing DES Commands in Persistent CA Parity Mode	$t_{\text{PAR_ALERT_RSP}}$	-	64	nCK	
Parity Latency	PL	5		nCK	
CRC Error Reporting					
CRC Error to ALERT Latency	$t_{\text{CRC_ALERT}}$	3	13	ns	
CRC ALERT Pulse Width	$t_{\text{CRC_ALERT_PW}}$	6	10	nCK	
Refresh Timing					
1x Refresh Cycle Time - 8Gb	t_{RFC1}	350	-	ns	34
2x Refresh Cycle Time - 8Gb	t_{RFC2}	260	-	ns	34
4x Refresh Cycle Time - 8Gb	t_{RFC4}	160	-	ns	34

Device Timing Parameters Notes

$$UI = t_{\text{CK(avg)min}}/2$$

- Start of internal write transaction is defined as follows:
 For BL8 (Fixed by MRS and on-the-fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (on-the-fly): Rising clock edge 4 clock cycles after WL.
 For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
- A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
- Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
- t_{WR} is defined in ns, for calculation of $t_{\text{WRP DEN}}$ it is necessary to round up $t_{\text{WR}}/t_{\text{CK}}$ following the rounding algorithm defined in the Rounding Algorithm Section
- WR in clock cycles as programmed in MRO.
- t_{REFI} depends on t_{OPER} .
- CKE is allowed to be registered low while operations such as row activation, precharge, auto-precharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
- For these parameters, the DDR4 SDRAM device supports $t_{\text{nPARAM}} [\text{nCK}] = \text{RU} \{t_{\text{PARAM}} [\text{ns}]/t_{\text{CK(avg)}} [\text{ns}]\}$, which is in clock cycles assuming all input clock jitter specifications are satisfied.
- When CRC and DM are both enabled, $t_{\text{WR_CRC_DM}}$ is used in place of t_{WR} .
- When CRC and DM are both enabled $t_{\text{WTR_S_CRC_DM}}$ is used in place of $t_{\text{WTR_S}}$.
- When CRC and DM are both enabled $t_{\text{WTR_L_CRC_DM}}$ is used in place of $t_{\text{WTR_L}}$.
- The max values are system dependent.
- DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
- The deterministic component of the total timing. Measurement method is TBD.
- DQ to DQ static offset relative to strobe per group. Measurement method is TBD.
- This parameter will be characterized and guaranteed by design.
- When the device is operated with the input clock jitter, this parameter needs to be derated by the actual $t_{\text{jit(per_total)}}$ of the input clock (output deratings are relative to the SDRAM input clock). Example TBD.
- DRAM DBI mode is off.
- DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.

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20. t_{QSL} describes the instantaneous differential output low pulse width on DQS - \overline{DQS} , as measured from on falling edge to the next consecutive rising edge.
21. t_{QSH} describes the instantaneous differential output high pulse width on DQS - \overline{DQS} , as measured from on falling edge to the next consecutive rising edge.
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval t_{REFI} .
23. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, $t_{WR_CRC_DM}$ is used in place of t_{WR} .
29. When CRC and DM are both enabled $t_{WTR_S_CRC_DM}$ is used in place of t_{WTR_S} .
30. When CRC and DM are both enabled $t_{WTR_L_CRC_DM}$ is used in place of t_{WTR_L} .
31. After CKE is registered LOW, CKE signal level shall be maintained below $V_{IL}(DC)$ for t_{CKE} specification (LOW Pulse Width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above $V_{IH}(DC)$ for t_{CKE} specification (HIGH Pulse Width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from $t_{CK(avg)min}$ to $t_{CK(avg)max}$ at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Table.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
37. Applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RZQ/7 RONNOM = 34 ohms.
40. 1 t_{CK} toggle mode with setting MR4:A11 to 0.
41. 2 t_{CK} toggle mode with setting MR4:A11 to 1.
42. 1 t_{CK} mode with setting MR4:A12 to 0.
43. 2 t_{CK} mode with setting MR4:A12 to 1.
44. The maximum read preamble is bounded by $t_{LZ(DQS)min}$ on the left side and $t_{DQSCk(max)}$ on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS differential signal cross point.
46. Last falling edge of DQS differential signal cross point to DQ rising signal middle-point of transferring from Low to High.
47. V_{REFDQ} value must be set to either its midpoint or $V_{CENT_DQ}(midpoint)$ in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by $t_{DQSCk(min)}$ plus $t_{QSH(min)}$ on the left side and $t_{HZ(DQS)max}$ on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately $0.7 * V_{DDQ}$ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to $V_{TT} = V_{DDQ}$.
50. For MR7 commands, the minimum delay to a subsequent non-MRS command is 5 nCK.

I_{DD} and I_{PP} Measurement-Loop Patterns Timing

Speed Bin		DDR4-2666	Units
Parameter		19-19-19	
t _{CK}		0.833	ns
CL		17	nCK
CWL		16	nCK
nRCD		17	nCK
nRC		56	nCK
nRAS		39	nCK
nRP		17	nCK
nFAW	x4	16	nCK
	x8	26	
	x16	36	
nRRDS	x4	4	nCK
	x8	4	
	x16	7	
nRRDL	x4	6	nCK
	x8	6	
	x16	8	
nRFC		421	nCK

I_{DD} and I_{PP} Measurement Conditions

- I_{DD} currents (such as I_{DD0}, I_{DD0A}, I_{DD1}, I_{DD1A}, I_{DD2N}, I_{DD2NA}, I_{DD2NL}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3NA}, I_{DD3P}, I_{DD4R}, I_{DD4RA}, I_{DD4W}, I_{DD4WA}, I_{DD5B}, I_{DD5F2}, I_{DD5F4}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7} and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the DDR4 SDRAM under test tied together. Any I_{PP} current is not included in I_{DD} currents.
- I_{PP} currents have the same definition as I_{DD} except that the current on the V_{PP} supply is measured.
- “0” and “LOW” is defined as V_{IN} ≤ V_{IL(AC)}max.
- “1” and “HIGH” is defined as V_{IN} ≥ V_{IH(AC)}min.
- “MID-LEVEL” is defined as inputs that are V_{REF} = V_{DD}/2.
- Timings used for I_{DD} and I_{PP} Measurement-Loop Patterns are provided in the I_{DD} and I_{PP} Measurement-Loop Patterns Timing on page 53.
- Basic I_{DD} and I_{PP} Measurement Conditions are described on pages 55-60.
- Detailed I_{DD} and I_{PP} Measurement-Loop Patterns are described on pages 62-70.
- I_{DD} and I_{PP} Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting:
 - RON = RZQ/7 (34 Ohm in MR1);
 - RTT_NOM = RZQ/6 (40 Ohm in MR1);
 - RTT_WR = RZQ/2 (120 Ohm in MR2);
 - RTT_PARK = Disable;
 - Qoff = 0B (Output Buffer enabled) in MR1;
 - TDQS disabled in MR1;
 - CRC disabled in MR2;
 - CA parity feature disabled in MR5;
 - Gear down mode disabled in MR3;
 - Read/Write DBI disabled in MR5;
 - DM disabled in MR5
- Attention: The I_{DD} and I_{PP} Measurement-Loop Patterns need to be executed at least one time before actual I_{DD} and I_{PP} measurement is started.
- Define $\overline{D} = \{\overline{CS}, \overline{ACT}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{\text{HIGH}, \text{LOW}, \text{LOW}, \text{LOW}, \text{LOW}\}$
- Define $\overline{D} = \{\overline{CS}, \overline{ACT}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{\text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}, \text{HIGH}\}$



Basic I_{DD} and I_{PP} Measurement Conditions

Symbol	Description
I _{DD0}	Operating One Bank Active-Precharge Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, nRC, nRAS, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: HIGH between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: Partially toggling according to I _{DD0} , I _{DD0A} and I _{PP0} Measurement-Loop Pattern on page 62; Data I/O: V _{DD} ; DM: Stable at 1; Bank Activity: Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,... (See I _{DD0} , I _{DD0A} and I _{PP0} Measurement-Loop Pattern on page 62); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD0} , I _{DD0A} and I _{PP0} Measurement-Loop Pattern on page 62
I _{DD0A}	Operating One Bank Active-Precharge Current (AL = CL - 1) AL: CL-1; Other conditions: See I _{DD0}
I _{PP0}	Operating One Bank Active-Precharge IPP Current Same conditions as I _{DD0}
I _{DD1}	Operating One Bank Active-Read-Precharge Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, nRC, nRAS, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: HIGH between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data I/O: Partially toggling according to I _{DD1} , I _{DD1A} and I _{PP1} Measurement-Loop Pattern on page 63; DM: Stable at 1; Bank Activity: Cycling with one bank active at a time: 0, 0, 1, 1, 2, 2,... (See I _{DD1} , I _{DD1A} and I _{PP1} Measurement-Loop Pattern on page 63); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD1} , I _{DD1A} and I _{PP1} Measurement-Loop Pattern on page 63
I _{DD1A}	Operating One Bank Active-Read-Precharge Current (AL = CL - 1) AL: CL - 1; Other Conditions: See I _{DD1}
I _{PP1}	Operating One Bank Active-Read-Precharge IPP Current Same Conditions as I _{DD1}
I _{DD2N}	Precharge Standby Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs, Data I/O: Partially Toggling according to I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 64; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 64
I _{DD2NA}	Precharge Standby Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD2N}
I _{PP2N}	Precharge Standby IPP Current Same Conditions as I _{DD2N}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD2NT}	Precharge Standby ODT Current CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD2NT} Measurement-Loop Pattern on page 65; Data I/O: V _{SS} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Toggling according to I _{DD2NT} Measurement-Loop Pattern on page 65; Pattern Details: See I _{DD2NT} Measurement-Loop Pattern on page 65
I _{DD2NL}	Precharge Standby Current with CAL Enabled Same Conditions as I _{DD2N} ; CAL Enabled ³
I _{DD2NG}	Precharge Standby Current with Geardown Mode Enabled Same Conditions as I _{DD2N} ; Geardown Mode Enabled ³
I _{DD2ND}	Precharge Standby Current with DLL Disabled Same Conditions as I _{DD2N} ; DLL Disabled ³
I _{DD2N_par}	Precharge Standby Current with CA Parity Enabled Same Conditions as I _{DD2N} ; CA Parity Enabled ³
I _{DD2P}	Precharge Power-Down Current CKE: LOW; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Stable at 0; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0
I _{PP2P}	Precharge Power-Down IPP Current Same Conditions as I _{DD2P}
I _{DD2Q}	Precharge Quiet Standby Current CKE: High; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Stable at 0; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0
I _{DD3N}	Active Standby Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 64; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: All Banks Closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD2N} , I _{DD2NA} , I _{PP2N} , I _{DD2NL} , I _{DD2NG} , I _{DD2ND} , I _{DD2N_par} , I _{DD3N} , I _{DD3NA} and I _{PP3N} Measurement-Loop Pattern on page 64

Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD3NA}	Active Standby Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD3N}
I _{PP3N}	Active Standby IPP Current Same Conditions as I _{DD3N}
I _{DD3P}	Active Power-Down Current CKE: LOW; External Clock: On; t _{CK} , CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; $\overline{\text{CS}}$: Stable at 1; Command, Address, Bank Group Address, Bank Address Inputs : Stable at 0; DATA I/O : V _{DD} ; DM : Stable at 1; Bank Activity : All Banks Open; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : Stable at 0
I _{PP3P}	Active Power-Down IPP Current Same Conditions as I _{DD3P}
I _{DD4R}	Operating Burst Read Current (AL = 0) CKE: HIGH; External Clock: On; t _{CK} , CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; $\overline{\text{CS}}$: HIGH between RD; Command, Address, Bank Group Address, Bank Address Inputs : Partially Toggling according to I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 66; DATA I/O : Seamless Read Data Burst with Different Data between One Burst and the Next One according to I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 66; DM : Stable at 1; Bank Activity : All Banks Open, RD Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 66); Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : Stable at 0; Pattern Details : See I _{DD4R} , I _{DD4RA} , I _{DD4RB} and I _{PP4R} Measurement-Loop Pattern on page 66
I _{DD4RA}	Operating Burst Read Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD4R}
I _{DD4RB}	Operating Burst Read Current with Read DBI Same Conditions as I _{DD4R} ; Read DBI Enabled ³
I _{PP4R}	Operating Burst Read IPP Current Same Conditions as I _{DD4R}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD4W}	Operating Burst Write Current (AL = 0) CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: HIGH between WR; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 67; DATA I/O: Seamless Write Data Burst with Different Data between One Burst and the Next One according to I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 67; DM: Stable at 1; Bank Activity: All Banks Open, WR Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 67); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at HIGH; Pattern Details: See I _{DD4W} , I _{DD4WA} , I _{DD4WB} , I _{DD4W_par} and I _{PP4W} Measurement-Loop Pattern on page 67
I _{DD4WA}	Operating Burst Write Current (AL = CL - 1) AL: CL - 1; Other conditions: See I _{DD4W}
I _{DD4WB}	Operating Burst Write Current with Write DBI Same Conditions as I _{DD4W} ; Write DBI Enabled ³
I _{DD4WC}	Operating Burst Write Current with Write CRC CKE: HIGH; External Clock: On; t_{CK}, CL: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: HIGH between WR; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD4WC} Measurement-Loop Pattern on page 68; DATA I/O: Seamless Write Data Burst with Different Data between One Burst and the Next One according to I _{DD4WC} Measurement-Loop Pattern on page 68; DM: Stable at 1; Bank Activity: All Banks Open, WR Commands Cycling through Banks: 0, 0, 1, 1, 2, 2,... (See I _{DD4WC} Measurement-Loop Pattern on page 68); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at HIGH; Pattern Details: See I _{DD4WC} Measurement-Loop Pattern on page 68 Measurement-Loop Pattern on page 67; Write CRC Enabled ³
I _{DD4W_par}	Operating Burst Write Current with CA Parity Same Conditions as I _{DD4W} ; CA Parity Enabled ³
I _{PP4W}	Operating Burst Write IPP Current Same Conditions as I _{DD4W}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD5B}	Burst Refresh Current (1X REF) CKE: HIGH; External Clock: On; t_{CK}, CL, nRFC: See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS: HIGH between REF; Command, Address, Bank Group Address, Bank Address Inputs: Partially Toggling according to I _{DD5B} , I _{PP5B} , I _{DD5F2} , I _{PP5F2} , I _{DD5F4} , and I _{PP5F4} Measurement-Loop Pattern on page 69; DATA I/O: V _{DD} ; DM: Stable at 1; Bank Activity: REF Command Every nRFC (See I _{DD5B} , I _{PP5B} , I _{DD5F2} , I _{PP5F2} , I _{DD5F4} , and I _{PP5F4} Measurement-Loop Pattern on page 69); Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: Stable at 0; Pattern Details: See I _{DD5B} , I _{PP5B} , I _{DD5F2} , I _{PP5F2} , I _{DD5F4} , and I _{PP5F4} Measurement-Loop Pattern on page 69
I _{PP5B}	Burst Refresh IPP Current (1X REF) Same Conditions as I _{DD5B}
I _{DD5F2}	Burst Refresh Current (2X REF) Same Conditions as I _{DD5B} ; t _{RFC} = t _{RFC2}
I _{PP5F2}	Burst Refresh IPP Current (2X REF) Same Conditions as I _{DD5F2} ; t _{RFC} = t _{RFC2}
I _{DD5F4}	Burst Refresh Current (4X REF) Same Conditions as I _{DD5B} ; t _{RFC} = t _{RFC4}
I _{PP5F4}	Burst Refresh IPP Current (4X REF) Same Conditions as I _{DD5F4} ; t _{RFC} = t _{RFC4}
I _{DD6N}	Self-Refresh Current: Normal Temperature Range T _{CASE} : 0 - 85°C; Low Power Array Self Refresh (LP ASR): Normal ⁴ ; CKE: LOW; External Clock: Off; CK and CK: LOW; CL: I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O: HIGH; DM: Stable at 1; Bank Activity: Self-Refresh Operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
I _{PP6N}	Self-Refresh IPP Current: Normal Temperature Range Same Conditions as I _{DD6N}
I _{DD6E}	Self-Refresh Current: Extended Temperature Range T _{CASE} : 0 - 95°C; Low Power Array Self Refresh (LP ASR): Extended ⁴ ; CKE: LOW; External Clock: Off; CK and CK: LOW; CL: I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL: 8 ¹ ; AL: 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O: HIGH; DM: Stable at 1; Bank Activity: Extended Temperature Self-Refresh Operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL
I _{PP6E}	Self-Refresh IPP Current: Extended Temperature Range Same Conditions as I _{DD6E}



Basic I_{DD} and I_{PP} Measurement Conditions (Continued)

Symbol	Description
I _{DD6R}	Self-Refresh Current: Extended Temperature Range T _{CASE} : 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE : LOW; External Clock : Off; CK and CK : LOW; CL : I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL : 8 ¹ ; AL : 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O : HIGH; DM : Stable at 1; Bank Activity : Reduced Temperature Self-Refresh Operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
I _{PP6R}	Self-Refresh IPP Current: Reduced Temperature Range Same Conditions as I _{DD6R}
I _{DD6A}	Auto Self-Refresh Current T _{CASE} : 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; Partial Array Self-Refresh (PASR) : Full Array; CKE : LOW; External Clock : Off; CK and CK : LOW; CL : I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL : 8 ¹ ; AL : 0; CS, Command, Address, Bank Group Address, Bank Address, Data I/O : HIGH; DM : Stable at 1; Bank Activity : Auto Self-Refresh Operation; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : MID-LEVEL
I _{PP6A}	Auto Self-Refresh IPP Current Same Conditions as I _{DD6A}
I _{DD7}	Operating Bank Interleave Read Current CKE : HIGH; External Clock : On; t _{CK} , nRAS, nRCD, nRRD, nFAW, CL : See I _{DD} and I _{PP} Measurement-Loop Patterns Timing on page 53; BL : 8 ¹ ; AL : CL - 1; CS : HIGH between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs : Partially Toggling according to I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 70; Data I/O : Read Data Bursts with Different Data between One Burst and the Next One according to I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 70; DM : Stable at 1; Bank Activity : Two Times Interleaved Cycling through Banks (0, 1,...7) with Different Addressing, See I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 70; Output Buffer and RTT : Enabled in Mode Registers ² ; ODT Signal : Stable at 0; Pattern Details : See I _{DD7} and I _{PP7} Measurement-Loop Pattern on page 70
I _{PP7}	Operating Bank Interleave Read IPP Current Same Conditions as I _{DD7}
I _{DD8}	Maximum Power-Down Read Current TBD
I _{PP8}	Maximum Power-Down IPP Current Same Conditions as I _{DD8}

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enabled:
 - Set MR1 [A12 = 0]: Qoff = Output buffer enabled
 - Set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7RTT_Nom Enabled:
 - Set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6RTT_WR Enabled:
 - Set MR2 [A10:9 = 01]: RTT_WR = RZQ/2RTT_PARK Disabled:
 - Set MR5 [A8:6 = 000]
3. CAL Enabled:
 - Set MR4 [A8:6 = 001]: 1600MT/s
 - Set MR4 [A8:6 = 010]: 1866MT/s, 2133MT/s
 - Set MR4 [A8:6 = 011]: 2400MT/sGeardown Mode Enabled:
 - Set MR3 [A3 = 1]: 1/4 RateDLL Disabled:
 - Set MR1 [A0 = 0]CA Parity Enabled:
 - Set MR5 [A2:0 = 001]: 1600MT/s, 1866MT/s, 2133MT/s
 - Set MR5 [A2:0 = 010]: 2400MT/sRead DBI Enabled:
 - Set MR5 [A12 = 1]Write DBI Enabled:
 - Set MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR):
 - Set MR2 [A7:6 = 00]: Normal Temperature Range
 - Set MR2 [A7:6 = 01]: Reduced Temperature Range
 - Set MR2 [A7:6 = 10]: Extended Temperature Range
 - Set MR2 [A7:6 = 11]: Auto Self Refresh.



I_{DD0}, I_{DD0A} and I_{PP0} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			3, 4	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if Necessary																			
		1	1*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 1 instead																			
		2	2*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	3*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	4*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	5*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	6*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	7*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	8*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		9	9*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
10	10*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																					
11	11*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																					
12	12*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
13	13*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
14	14*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
15	15*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																					

For x4 and x8 only



I_{DD1}, I_{DD1A} and I_{PP1} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1-2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3-4	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	Repeat pattern 1-4 until nRCD - 1. Truncate if Necessary																			
			nRCD - AL	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																			
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1-4 until nRC - 1. Truncate if Necessary																			
			1*nRC + 0	ACT	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	-
			1*nRC + 1-2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1*nRC + 3-4	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	0	7	F	0	-	
			...	Repeat pattern nRC + 1-4 until 1*nRC + nRCD - 1. Truncate if Necessary																			
			1*nRC + nRCD - AL	RD	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			...	Repeat pattern 1-4 until nRAS - 1. Truncate if Necessary																			
			1*nRC + nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		...	Repeat pattern nRC + 1-4 until 2*nRC - 1. Truncate if Necessary																				
		2	2*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	3*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	4*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	5*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	6*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	7*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	8*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		9	9*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		10	10*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
		11	11*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																			
		12	12*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																			
		13	13*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																			
		14	14*nRC	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																			
		15	15*nRC	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																			

For x4 and x8 only

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**I_{DD2N}, I_{DD2NA}, I_{PP2N}, I_{DD2NL}, I_{DD2NG}, I_{DD2ND}, I_{DD2N_par}, I_{DD3N}, I_{DD3NA} and I_{PP3N}
 Measurement-Loop Pattern¹**

CK, CK	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	\overline{ACT}	RAS/A16	CAS/A15	$\overline{WE}/A14$	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			2	\overline{D} , \overline{D}	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	0
			3	\overline{D} , \overline{D}	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	0
		1	4-7	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 1 instead																		
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																		
		3	12-15	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																		
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																		
		5	20-23	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																		
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																		
		7	28-31	Repeat Sub-Loop 0, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																		
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																		
		9	36-39	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																		
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																		
		11	44-47	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																		
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																				
13	52-55	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																				
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																				
15	60-63	Repeat Sub-Loop 0, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																				

For x4 and x8 only



I_{DD2NT} Measurement-Loop Pattern

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-		
			1	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
			3	$\overline{D}, \overline{D}$	1	1	1	1	1	0	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		1	4-7	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 1 and BA[1:0] = 1 instead																			
		2	8-11	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	12-15	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	16-19	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	20-23	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	24-27	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	28-31	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	32-35	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 2 and BA[1:0] = 0 instead																			For x4 and x8 only
		9	36-39	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		10	40-43	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
		11	44-47	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 3 and BA[1:0] = 3 instead																			
12	48-51	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
13	52-55	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
14	56-59	Repeat Sub-Loop 0, but ODT = 0, BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
15	60-63	Repeat Sub-Loop 0, but ODT = 1, BG[1:0] ² = 3 and BA[1:0] = 0 instead																					



I_{DD4R}, I_{DD4RA}, I_{DD4RB} and I_{PP4R} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	RD	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2-3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		1	4	RD	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00	
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6-7	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	12-15	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	20-23	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	28-31	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		9	36-39	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
11	44-47	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																					
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
13	52-55	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
15	60-63	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																					

For x4 and x8 only



I_{DD4W}, I_{DD4WA}, I_{DD4WB}, I_{DD4W_par} and I_{PP4W} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴			
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF		
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2-3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		1	4	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00	
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			6-7	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-	
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		3	12-15	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		5	20-23	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		7	28-31	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		9	36-39	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
11	44-47	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																					
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																					
13	52-55	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																					
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																					
15	60-63	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																					
																				For x4 and x8 only			



I_{DD4WC} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
Toggling	Static High	0	0	WR	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF D8 = CRC	
			1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
			2-3	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-	
		1	4	WR	0	1	1	0	1	0	0	0	1	1	0	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00 D8 = CRC
			5	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			6-7	$\overline{D}, \overline{D}$	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	-	
		2	8-11	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																		
		3	12-15	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																		
		4	16-19	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																		
		5	20-23	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																		
		6	24-27	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																		
		7	28-31	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																		
		8	32-35	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																		
		9	36-39	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																		
		10	40-43	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																		
11	44-47	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																				
12	48-51	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																				
13	52-55	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																				
14	56-59	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																				
15	60-63	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																				

For x4 and x8 only



I_{DD5B}, I_{PP5B}, I_{DD5F2}, I_{PP5F2}, I_{DD5F4} and I_{PP5F4} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]BC	A[17,13,11]	A[10]AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
toggling	Static High	0	0	REF	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-	
		1	1	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		2	2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
		3	3	D, D	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
		4	4	D, D	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
		4-7	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		8-11	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																			
		12-15	Repeat Pattern 1-4, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																			
		16-19	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																			
		20-23	Repeat Pattern 1-4, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																			
		24-27	Repeat Pattern 1-4, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																			
		28-31	Repeat Pattern 1-4, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																			
		32-35	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																			
		36-39	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																			
		40-43	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																			
		44-47	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																			
		48-51	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																			
		52-55	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																			
		56-59	Repeat Pattern 1-4, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																			
		60-63	Repeat Pattern 1-4, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																			
		2	64-nRFC - 1 Repeat Sub-Loop 1. Truncate if Necessary																			

For x4 and x8 only



I_{DD7} and I_{PP7} Measurement-Loop Pattern¹

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	ACT	RAS/A16	CAS/A15	WE/A14	ODT	C[2:0] ³	BG[1:0] ²	BA[2:0]	A[12]/BC	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data ⁴		
Toggling	Static High	0	0	ACT	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	-	
			1	RDA	0	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	D0 = 00, D1 = FF D2 = FF, D3 = 00 D4 = FF, D5 = 00 D6 = 00, D7 = FF
			2	D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3	\overline{D}	1	1	1	1	1	1	0	0	3 ²	3	0	0	0	7	F	0	0	-
			...	Repeat pattern 2-3 until nRRD - 1, if nRCD > 4. Truncate if Necessary																		
		1	nRRD	ACT	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	-
			nRRD + 1	RDA	0	1	1	0	1	0	0	0	1	1	0	0	1	0	0	0	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D6 = FF, D7 = 00
			...	Repeat pattern 2-3 until 2*nRRD - 1, if nRCD > 4. Truncate if Necessary																		
		2	2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 2 instead																		
		3	3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 3 instead																		
		4	4*nRRD	Repeat pattern 2-3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if Necessary																		
		5	nFAW	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 1 instead																		
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 2 instead																		
		7	nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 0 and BA[1:0] = 3 instead																		
		8	nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 1 and BA[1:0] = 0 instead																		
		9	nFAW + 4*nRRD	Repeat Sub-Loop 4																		
		10	2*nFAW	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 0 instead																		
		11	2*nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 1 instead																		
		12	2*nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 2 instead																		
		13	2*nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 3 instead																		
14	2*nFAW + 4*nRRD	Repeat Sub-Loop 4																				
15	3*nFAW	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 1 instead																				
16	3*nFAW + nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 2 instead																				
17	3*nFAW + 2*nRRD	Repeat Sub-Loop 0, but BG[1:0] ² = 2 and BA[1:0] = 3 instead																				
18	3*nFAW + 3*nRRD	Repeat Sub-Loop 1, but BG[1:0] ² = 3 and BA[1:0] = 0 instead																				
19	3*nFAW + 4*nRRD	Repeat Sub-Loop 4																				
20	4*nFAW	Repeat pattern 2-3 until nRC - 1, if nRC > 4*nFAW. Truncate if Necessary																				

For x4 and x8 only

Notes:

1. DQS, $\overline{\text{DQS}}$ are V_{DD} .
2. BG1 is don't care for a x16 device.
3. C[2:0] are used only for a 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are V_{DD} .

I_{DD} Specifications

Parameter	DDR4-2666	Units
	19-19-19	
I _{DD0}	296	mA
I _{DD0A}	304	mA
I _{DD1}	376	mA
I _{DD1A}	400	mA
I _{DD2N}	224	mA
I _{DD2NA}	224	mA
I _{DD2NT}	264	mA
I _{DD2NL}	168	mA
I _{DD2NG}	224	mA
I _{DD2ND}	216	mA
I _{DD2N_par}	224	mA
I _{DD2P}	160	mA
I _{DD2Q}	200	mA
I _{DD3N}	304	mA
I _{DD3NA}	304	mA
I _{DD3P}	248	mA
I _{DD4R}	1008	mA
I _{DD4RA}	1032	mA
I _{DD4RB}	1024	mA
I _{DD4W}	864	mA
I _{DD4WA}	896	mA
I _{DD4WB}	816	mA
I _{DD4WC}	848	mA
I _{DD4W_par}	1000	mA

I_{DD} Specifications (Continued)

Parameter	DDR4-2666	Units
	19-19-19	
I _{DD5B}	1800	mA
I _{DD5F2}	1352	mA
I _{DD5F4}	1200	mA
I _{DD6N}	200	mA
I _{DD6E}	256	mA
I _{DD6R}	120	mA
I _{DD6A}	256	mA
I _{DD7}	1168	mA
I _{DD8}	96	mA

I_{PP} Specifications

Parameter	DDR4-2666	Units
	19-19-19	
I _{PP0}	44	mA
I _{PP1}	52	mA
I _{PP2N}	25.6	mA
I _{PP2P}	25.6	mA
I _{PP3N}	128	mA
I _{PP3P}	128	mA
I _{PP4R}	152	mA
I _{PP4W}	152	mA
I _{PP5B}	600	mA
I _{PP5F2}	400	mA
I _{PP5F4}	336	mA
I _{PP6N}	46.4	mA
I _{PP6E}	62.4	mA
I _{PP6R}	37.4	mA
I _{PP6A}	62.4	mA
I _{PP7}	144	mA
I _{PP8}	25.6	mA

Input/Output Capacitance

Parameter	Symbol	DDR4-2666		Units	Notes
		Min	Max		
Input/output capacitance	C_{IO}	0.55	1.15	pF	1, 2
Input/output capacitance delta	C_{DIO}	-0.1	0.1	pF	1, 2, 8
Input/output capacitance delta, DQS and \overline{DQS}	C_{DDQS}	-	0.05	pF	1, 2, 4
Input capacitance, CK and \overline{CK}	C_{CK}	0.8	2.8	pF	1
Input capacitance delta, CK and \overline{CK}	C_{DCK}	-	0.2	pF	1, 3
Input capacitance, ADD, CMD, CTRL input-only pins	C_I	0.8	2.8	pF	1, 5
Input capacitance delta, ADD, CMD, CTRL input-only pins	C_{DI}	-0.4	0.4	pF	1, 6, 7
Input capacitance of ALERT	C_{ALERT}	2	6	pF	1

Notes:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM, DQS, \overline{DQS} , TDQS, \overline{TDQS} . Although the DM, TDQS and \overline{TDQS} pins have different functions, the loading matches DQ and \overline{DQS}
3. Absolute value CK - \overline{CK}
4. Absolute value of $C_{IO}(DQS) - C_{IO}(\overline{DQS})$
5. C_I applies to ODT, \overline{CS} , CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}/A16$, $\overline{CAS}/A15$, $\overline{WE}/A14$, \overline{ACT} and PAR.
6. C_{DI} applies to ODT, \overline{CS} , CKE, A0-A17, BA0-BA1, BG0-BG1, $\overline{RAS}/A16$, $\overline{CAS}/A15$, $\overline{WE}/A14$, \overline{ACT} and PAR.
7. $C_{DI} = C_I - 0.5 * (C_I(\overline{CLK}) + C_I(\overline{CLK}))$
8. $C_{DIO} = C_{IO}(DQ, DM) - 0.5 * (C_{IO}(DQS) + C_{IO}(\overline{DQS}))$.

Declaration of Conformity



Responsible Party Name: SMART Modular Technologies, Inc.
Address: 39870 Eureka Drive
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hereby declares that the products:

ST1026MP41W693HC

to which this declaration relates are in conformity with the following Directives and other normative documents:

RoHS Directive 2011/65/EU

Restriction of the use of certain hazardous substances in electrical and electronic equipment

• **EN 50581:2012**

Technical documentation for the assessment of electrical and electronic products with respect to the restriction of hazardous substances

Name: Jeffrey Milano
Title: Director, Worldwide Quality
Date: February 12, 2019

Representative in the European Union (for regulatory topics only):

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