SiT5001

1-80 MHz MEMS TCXO and VCTCXO

Advanced Information

Features, Benefits and Applications

- Any frequency between 1 and 80 MHz with 6 decimal places of accuracy
- 100% pin-to-pin drop-in replacement to quartz-based TCXO
- Excellent total frequency stability as low as ±1 PPM (see SiT5003 for ±0.5 PPM option)
- Ultra low phase jitter: 0.5 ps (12 kHz to 20 MHz)
- Voltage control option with pull range of ±12.5 PPM, ±25 PPM or ±50 PPM
- LVCMOS/HCMOS compatible output
- Voltage control, standby, output enable or no connect modes
- Three industry-standard 4-pin packages: 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm (For 6-pin, contact SiTime)
- Outstanding silicon reliability of 2 FIT (10x improvement over quartz-based devices)
- Ultra short lead time
- Ideal for telecom, networking, smart meter, GPS and wireless applications

Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	80	MHz	
Frequency Stability						
Initial tolerance	F_init	-1	–	1	PPM	at 25°C
Stability over temperature	F_stab	-1	–	+1	PPM	Over operating temperature range at rated nominal power supply voltage (1.8V, 2.5V, 2.8V, 3.3V or 3.3V) and nominal load (15 pF).
		-1.5	–	+1.5	PPM	
		-2.5	–	+2.5	PPM	
		-5	–	+5	PPM	
Supply Voltage	F_vdd	–	0.05	–	PPM	±10% Vdd (±5% for Vdd = 1.8V)
Output Load	F_load	–	0.1	–	PPM	±10% of 15 pF load
Aging	F_aging	–1.0	–	1.0	PPM	1st year, 25°C
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.70	3.0	3.3	V	
		2.97	3.3	3.63	V	
Pull Range	PR	±12.5, ±25, ±50			PPM	
Control Voltage	VC	10	–	90	%VDD	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage -3dB Bandwidth	V_BW	–	–	8	kHz	
Current Consumption	Idd	–	32	TBD	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V, 3.0 V or 3.3 V
		–	31	TBD	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_stby	–	10	TBD	µA	$\overline{ST}$ = GND, All Vdd, Weak internal pull down
Duty Cycle	DC	45	–	55	%	All Vdds.
Rise/Fall Time	Tr, Tf	–	1.5	–	ns	15 pF load, 10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	IOH = TBD mA
Output Voltage Low	VOL	–	–	10%	Vdd	IOL = TBD mA
Output Load	Load	–	–	15	pF	At maximum frequency and supply voltage. Contact SiTime for higher output load option
Input Voltage High	VIH	70%	–	–	Vdd	Pin 1, OE or $\overline{ST}$
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 1, OE or $\overline{ST}$
Startup Time	T_start	–	–	10	ms	Measured from the time Vdd reaches its rated minimum value
OE Enable/Disable Time	T_oe	–	–	TBD	ms	
Resume Time	T_resume	–	6	TBD	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	1.7	–	ps	f = 10 MHz, all Vdds
RMS Phase Jitter (random)	T_phj	–	0.5	–	ps	f = 10 MHz, Integration bandwidth = 12 kHz to 20MHz, All Vdds

■ Specifications (Cont.)

Pin Description Tables

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change
OE
H or Open[1]: specified frequency output
L: output is high impedance
$\overline{ST}$
H or Open[1]: specified frequency output
L: output is low level (weak pull down). Oscillation stops
NC
H or L or Open: No effect on device functions

Pin Map	
Pin	**Connection**
1	OE/$\overline{ST}$/NC/VC
2	GND
3	CLK
4	VDD

Absolute Maximum Ratings

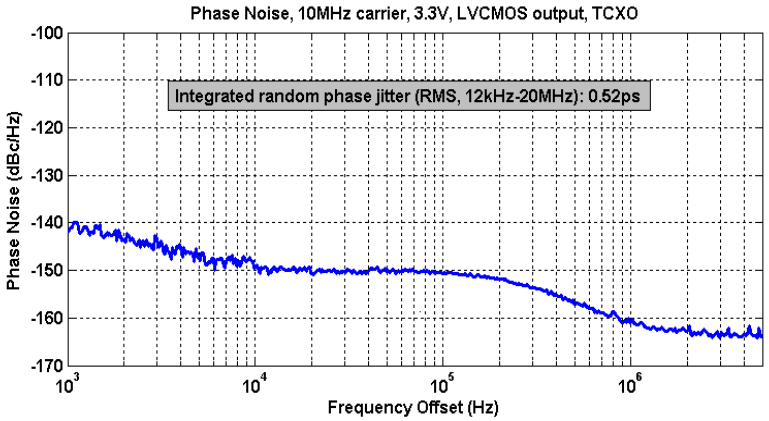
Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge (Human Body Model)	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65 V)	1,000+	–	years

Environmental Compliance

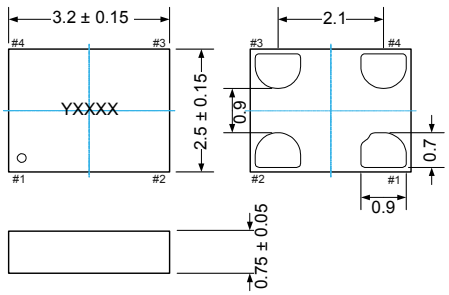
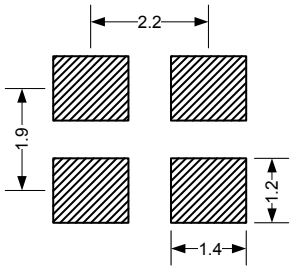
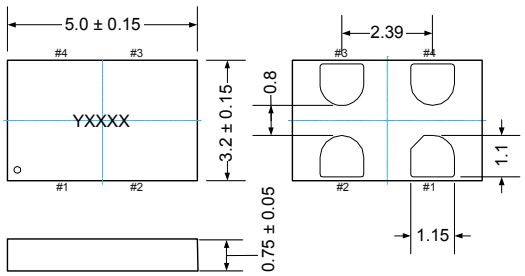
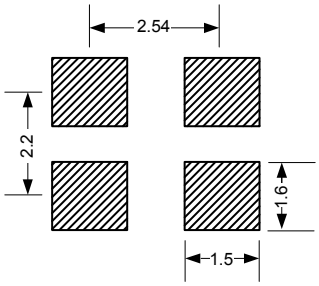
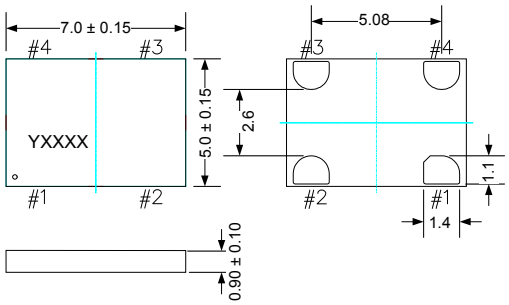
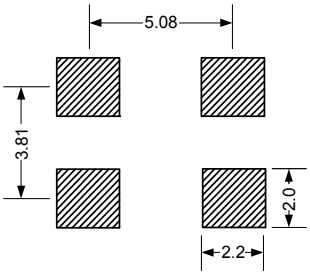
Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level (MSL)	MSL1 @ 260°C

Phase Noise Plot



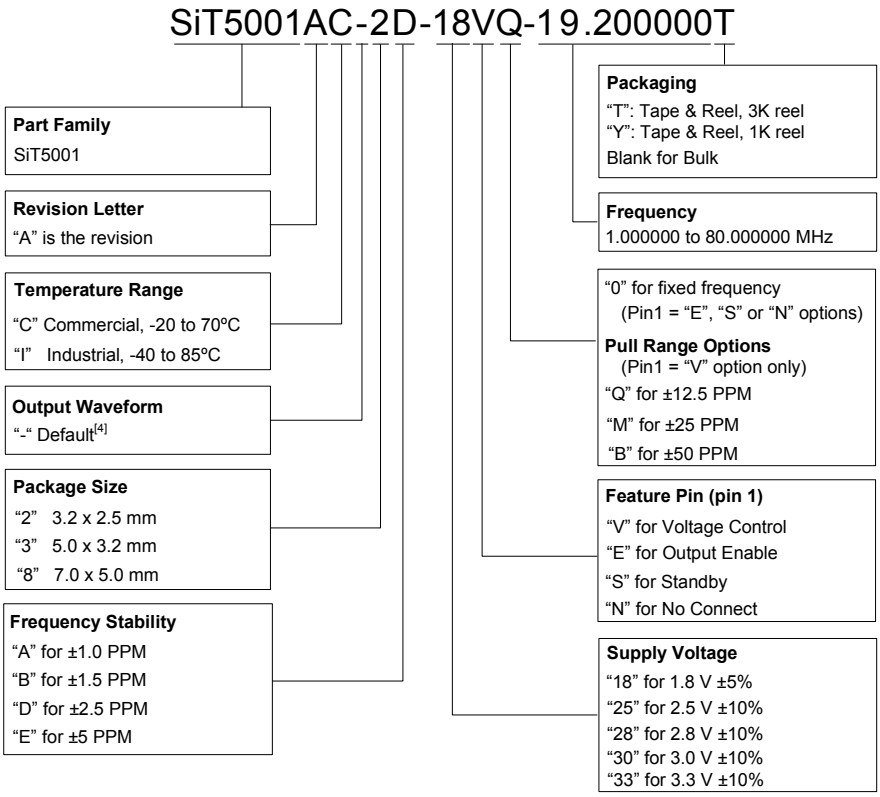
Note:
1. In 1.8V mode, a resistor of <100 kΩ between OE pin and Vdd is required. For other supply voltage options, SiTime recommends using a similar pull-up resistor.

Dimensions and Land Patterns

Package Size – Dimensions (Unit: mm)[2]	Recommended Land Pattern (Unit: mm)[3]
3.2 x 2.5 x 0.75 mm 	
5.0 x 3.2 x 0.75 mm 	
7.0 x 5.0 x 0.90 mm 	

Notes:
2. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
3. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Part No. Guide - How to Order



Notes:

4. Contact SiTime for SoftEdge™ output waveform that reduces EMI and is similar to clipped sinewave in functionality