SiT3808

High Performance MEMS VCXO

Advanced information

Features, Benefits and Applications

- Any frequency between 1 MHz and 80 MHz with 6 decimal places of accuracy
- 100% pin-to-pin compatible with and direct replacement of quartz based VCXO
- Widest pull range options: ±25, ±50, ±100, ±150, ±200, ±400, ±800, ±1600 PPM
- Superior pull range linearity of <= 1%, 10 times better than quartz
- LVCMOS/LVTTL compatible output
- Typical tuning voltage: 0 V to Vdd
- Three industry-standard packages: 3.2 mm x2.5 mm (4-pin), 5.0 mm x 3.2 mm (6-pin), 7.0 mm x 5.0 mm (6-pin)
- Outstanding siicon reliability of 2 FIT (10x improvement over quartz-based devices)
- Ultra short lead time
- Ideal for telecom clock synchronization, instrumentation, low bandwidth analog PLL, jitter cleaner, clock recovery, audio, video, FPGA, broadband and networking

Specifications

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Frequency Range	f	1	–	80	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of initial tolerance (F_init), operating temperature, rated power, supply voltage change, load change
		-25	–	+25	PPM	
		-50	–	+50	PPM	Select stability option in part number ordering (see back page)
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial
Supply Voltage	Vdd	1.71	1.8	1.89	V	
		2.25	2.5	2.75	V	
		2.52	2.8	3.08	V	
		2.97	3.3	3.63	V	
Pull Range[1,2]	PR	±25, ±50, ±100,±150, ±200, ±400, ±800, ±1600			PPM	
Upper Control Voltage	VC_U	1.62	–	1.7	V	Vdd = 1.8 V, Voltage at which maximum deviation is guaranteed.
		2.25	–	2.3	V	Vdd = 2.5 V, Voltage at which maximum deviation is guaranteed.
		2.52	–	2.6	V	Vdd = 2.8 V, Voltage at which maximum deviation is guaranteed.
		3	–	3.1	V	Vdd = 3.3 V, Voltage at which maximum deviation is guaranteed.
Lower Control Voltage	VC_L	0	–	0.1	V	Voltage at which maximum deviation is guaranteed.
Linearity	Lin	–	–	1	%	
Frequency Change Polarity	–	Positive slope			–	
Control Voltage Bandwidth(-3dB)	V_BW	–	8	–	kHz	Contact SiTime for 16 kHz bandwidth
		2.97	3.3	3.63	V	
Current Consumption	Idd	–	29	33	mA	No load condition, f = 20 MHz, Vdd = 2.5 V, 2.8 V or 3.3 V
		–	31	31	mA	No load condition, f = 20 MHz, Vdd = 1.8 V
Standby Current	I_std	–	–	TBD	µA	$\overline{ST}$ = GND, All Vdd, Output is Weakly Pulled Down
Duty Cycle	DC	45	–	55	%	All Vdds
Rise/Fall Time	Tr, Tf	–	1.0	2.2	ns	Vdd = 1.8, 2.5, 2.8 or 3.3 V, 10% - 90% Vdd level
Output Voltage High	VOH	90	–	–	%Vdd	IOH = TBD
Output Voltage Low	VOL	–	–	10	%Vdd	IOL = TBD
Output Load	Ld	–	–	15	pF	
Start-up Time	T_start	–	6	10	ms	
OE Enable/Disable Time	T_oe	–	–	TBD	ms	
Resume Time	T_resume	–	–	10	ms	Measured from the time ST pin crosses 50% threshold
RMS Period Jitter	T_jitt	–	1.7	–	ps	f = 10 MHz, all Vdds
RMS Phase Jitter (random)	T_phj	–	0.51	–	ps	f = 10 MHz, Pull range = 100 PPM, Integration bandwidth = 12kHz to 20MHz, all Vdds
Aging	F_aging	–	–	±5	PPM	10 years

Notes:
1. Absolute Pull Range (APR) is defined as the guaranteed pull range over temperature and voltage.
2. APR = pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

■ Specifications (Cont.)

Pin Description Tables (4-pin device)

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change

Pin Map	
Pin	**Connection**
1	VIN
2	GND
3	CLK
4	Vdd

Pin Description Tables (6-pin device)

Pin #1 Functionality
VIN
0 - Vdd: produces voltage dependent frequency change
Pin #2 Functionality
NC
H or L or Open: No effect on output frequency or other device functions
OE
H or Open[3]: specified frequency output
L: output is high impedance
$\overline{ST}$
H or Open[3]: specified frequency output
L: output is low level (weak pull down). Oscillation stops

Pin Map	
Pin	**Connection**
1	VIN
2	NC/OE/$\overline{ST}$
3	GND
4	CLK
5	NC
6	Vdd

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

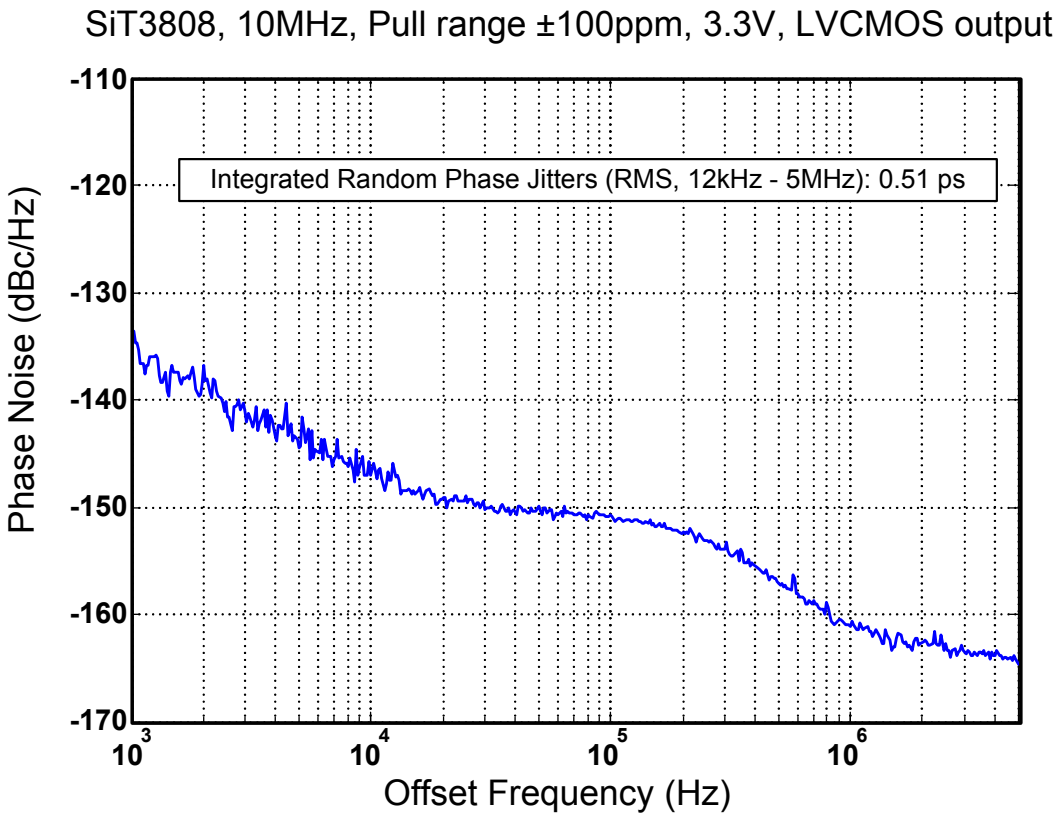
Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
Vdd	-0.5	4	V
Electrostatic Discharge	–	6000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125°C, Process, Vdd (0 to 3.65 V)	1,000+	–	years

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002; 50kG
Mechanical Vibration	MIL-STD-883F, Method 2007; 70G
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensibility Level	MSL1 @ 260°C

Notes:
3. In 1.8V mode, a resistor of <10 kΩ between OE pin and Vdd is required. SiTime recommends using pull-up resistors for other Vdd(s).

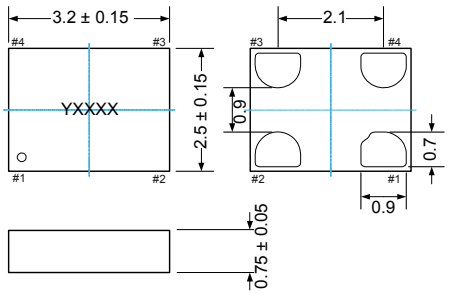
Phase Noise Plot

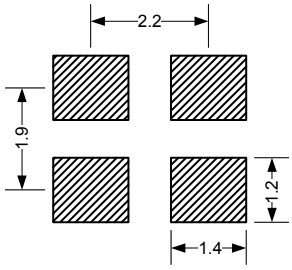


■ Dimensions and Land Patterns

Packages (4-pin device)

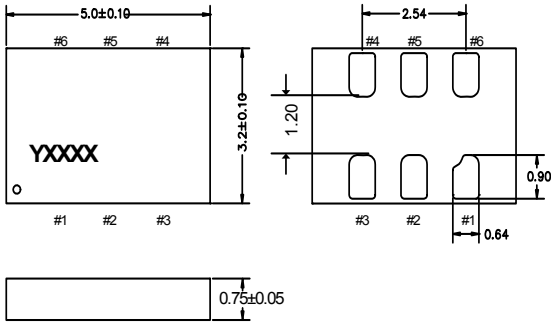
3.2 x 2.5 x 0.75 mm

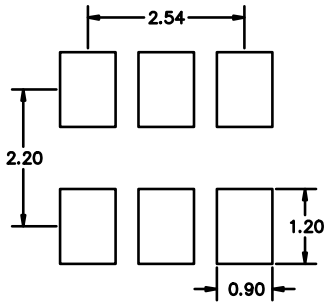


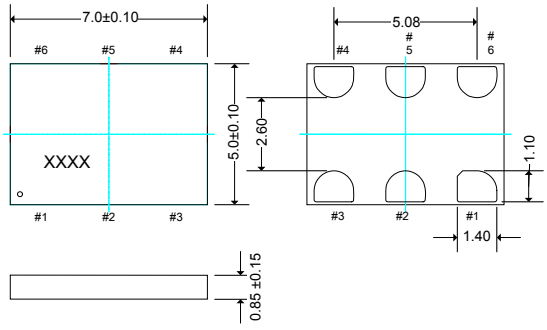


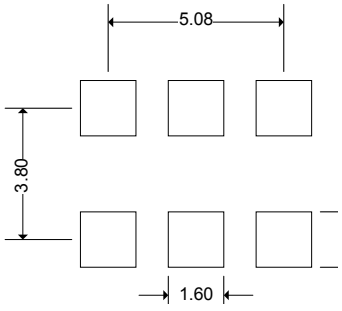
Packages (6-pin device)

Package Size – Dimensions (Unit: mm)[4]	Recommended Land Pattern (Unit: mm)[5]
5.0 x 3.2 x 0.75 mm	
7.0 x 5.0 x 0.90 mm	





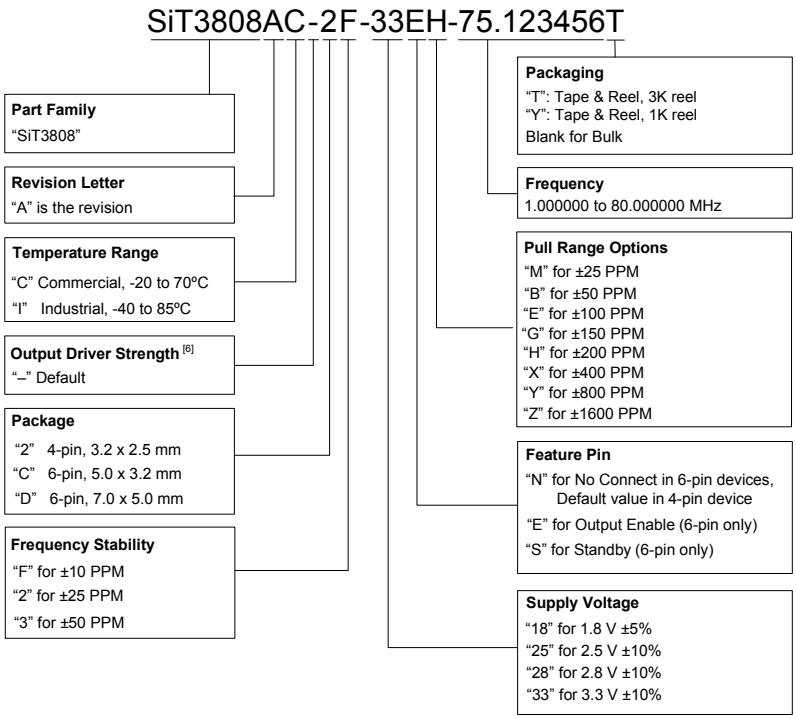




Notes:

4. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
5. A capacitor of value 0.1 µF between Vdd and GND is recommended.

Part No. Guide - How to Order



APR Definition

Absolute pull range (APR) = Norminal pull range (PR) - frequency stability (F_stab) - Aging (F_aging)

APR Table

Nominal Pull Range	Frequency Stability		
	± 10	± 25	±50
	APR (PPM)		
± 25	± 10	—	—
± 50	± 35	± 20	—
± 100	± 85	± 70	± 45
± 150	± 135	± 120	± 95
± 200	± 185	± 170	± 145
± 400	± 385	± 370	± 345
± 800	± 785	± 770	± 745
± 1600	± 1585	± 1570	± 1545

Note:
6. Contact SiTime for different drive strength options for driving higher loads or reducing EM