SiT9375

Ultra-Low Jitter Differential XO for Standard Frequencies

Description

The SiT9375 is a differential oscillator with an integrated MEMS resonator (such as ApexMEMS™), that is engineered for low-jitter applications requiring standard frequencies from 25 MHz to 644.53125 MHz.

In addition to standard differential signal types, a unique FlexSwing™ output-driver performs like LVPECL and provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9375 can be factory programmed for specific combinations of frequency, stability, output signaling, voltage, and output enable functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to Manufacturing Notes for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Standard frequencies from 25 MHz to 644.53125 MHz
- 150 fs RMS typical phase jitter, 12 kHz to 20 MHz
- 9 fs/mV typical PSNR
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ±20, ±25, ±30, and ±50 ppm frequency stabilities
- Wide temperature range (-40°C to 105°C)
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous power supply voltage range options
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package

Applications

- 100G/200G/400G/800G network equipment
- Optical modules
- Coherent optics
- Network switches, routers
- Industrial networking equipment
- Server and storage systems
- Test and measurement
- Broadcast video

Order samples

Block Diagram

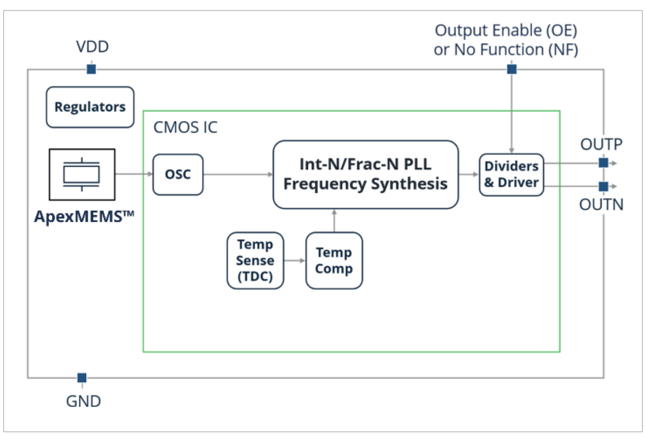

Figure 1. SiT9375 Block Diagram

Package Pinout

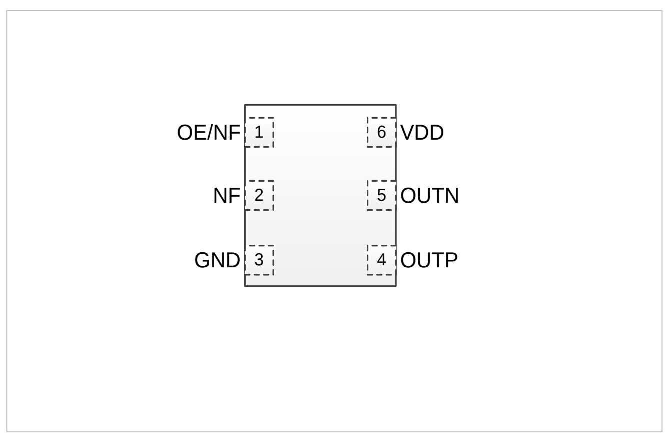

Figure 2. Pin Assignments (Top view)
(Refer to Table 16 for Pin Descriptions)

Ordering Information

SiT9375AC-01B2-3310-100.000000D

Part Family
"SiT9375"

Revision Letter
"A" is the revision of Silicon

Temperature Range
"C": Extended Commercial, -20 to 70°C
"I": Industrial, -40 to 85°C
"B": -40 to 95°C
"E": Extended Industrial, -40 to 105°C

Signaling Group
"-": LVPECL, LVDS, HCSL, Low-power HCSL
"1": FlexSwing referenced to voltage on VDD pin.
"0": FlexSwing referenced to voltage on GND pin.

Signaling Type
"01": LVPECL
"02": LVDS
"04": HCSL
"08": Low-power HCSL
2-digit order code: FlexSwing, see Table 17 and Table 18 for 2-digit order code specifying V_Swing, VHn and VLn.

Packaging
Refer to Table 1 for packing method
Leave blank for bulk (for sampling only)

Frequency
Refer to the frequencies in Table 2

Reserved
"0-": Default

Pin 1 Functionality
"0": NF (no function)
"1": OE active high
"2": OE active low

Supply Voltage
"18": 1.8 V ± 5%
"25": 2.5 V ±10%
"33": 3.3 V ±10%
"XX": 2.25 V to 3.63 V
"YY": 1.71 V to 3.63 V

Frequency Stability
"1": ±20 ppm
"2": ±25 ppm
"8": ±30 ppm
"3": ±50 ppm

Package Size[1]
"P": 2.0 x 1.6 mm x mm
"A": 2.5 x 2.0 mm x mm
"B": 3.2 x 2.5 mm x mm

Note:
1. Contact SiTime for other package sizes.
2. Contact SiTime for Spread Spectrum option for EMI reduction.

Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

Table 2. Supported Frequencies

25.000000 MHz	30.720000 MHz	50.000000 MHz	53.125000 MHz	61.440000 MHz	62.500000 MHz	74.250000 MHz	75.000000 MHz
80.000000 MHz	98.304000 MHz	100.000000 MHz	106.250000 MHz	122.880000 MHz	125.000000 MHz	133.333333 MHz	148.500000 MHz
150.000000 MHz	153.600000 MHz	155.520000 MHz	156.250000 MHz	159.375000 MHz	160.000000 MHz	161.132813 MHz	166.666666 MHz
200.000000 MHz	212.500000 MHz	250.000000 MHz	300.000000 MHz	312.500000 MHz	322.265625 MHz	333.330000 MHz	425.000000 MHz
625.000000 MHz	644.531250 MHz						

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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage. See Test Circuit Diagrams for the test setups used with each signaling type.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information section
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 2 pF ± 10%, and 10 years aging at 85°C
		–	–	±25	ppm	
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±0.7	±2.3	ppm	Ambient temperature of 85°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code "YY"
		2.25	–	3.63	V	Voltage-supply order code "XX"
		1.71	1.80	1.89	V	Voltage-supply order code "18". Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code "25"
		2.97	3.30	3.63	V	Voltage-supply order code "33"
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Logic High function for Pin 1
Input Voltage Low	VIL	–	–	30%	Vdd	Logic High function for Pin 1
Input Pull-up/Pull-down Impedance	Z_in	112.9	120	133.4	kΩ	Pin 1 for OE function
Output Characteristics						
Duty Cycle	DC	48	–	52	%	See Figure 18 for waveform.
Startup, OE and SE Timing						
Startup Time	T_start	–	1.2	2	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time 1	T_oe	–	–	100+3 clock cycles	ns	For all signaling types except Low-Power HCSL. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 24 for waveform.
Output Enable Time 2	T_oe	–	–	500+3 clock cycles	ns	For Low-Power HCSL signaling type. Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of final swing. See Figure 24 for waveform.
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 25 for waveform.
Jitter and Phase Noise, measured at f = 156.25 MHz unless specified otherwise						
"4-16A" Phase Jitter[3]	T_416A	-	85	115	fs rms	Measuring with phase noise analyzer, extending (flat) phase noise to 3rd harmonic (e.g. 312.5 MHz offset), folding phase noise below the Nyquist frequency, filtering and integrating. Uses 4 MHz low pass and 16 MHz high pass filters, each with 20 dB/dec roll off. Includes spurs. See for "4-16A" Phase Jitter Methodology additional details.
Legacy RMS Phase Jitter (random)	T_phj	–	150	200	fs	12 kHz to 20 MHz offset frequency integration bandwidth Refer to SiT95 fi01 for <100 fs rms jitter.
Spurious Phase Noise	PN_spur_a	–	-110	–	dBc	12 kHz to 20 MHz offset frequency range
	PN_spur_b	–	-88	–	dBc	12 kHz to 20 MHz offset frequency range. Measured at f = 155.52 MHz
RMS Period Jitter[4]	T_jitt_per	–	0.5	0.6	ps	Measured based on 10K cycles
Peak Cycle-to-cycle Jitter[4]	T_jitt_cc	–	3.5	6.2	ps	Measured based on 1K cycles

Note:

3. Measured according to JESD65B using Keysight DSAX91604A Oscilloscope.
4. Applicable for SerDes applications. Label "4-16A" refers to filtering with 4 MHz receive CDR and 16 MHz transmit PLL bandwidths and accounting for aliased phase noise.

Table 4. Electrical Characteristics – LVPECL | Supply voltage (“order code”): 2.5 V ±10% (“25”), 3.3 V ±10% (“33”), 2.25 V to 3.63 V (“XX”). All typical specifications are measured at nominal supply voltage of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 7 and Figure 8 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	35.5	42.5	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	46	56	mA	Including load termination current as shown in Figure 29 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V and R3=220 Ohms
		–	46	52	mA	Including load termination current as shown in Figure 29 for Vdd=2.5 V ±10% and R3=220 Ohms
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	62	68	mA	Including load termination current. See Figure 30 for termination
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	53.5	65	mA	Including load termination current as shown in Figure 29 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	53.5	61	mA	Including load termination current as shown in Figure 29 for Vdd=2.5 V ±10% and R3=220 Ohms. Driver output is at logic-high voltage levels.
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	73.5	80	mA	Including load termination current. See Figure 30 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.075	Vdd-0.95	Vdd-0.86	V	See Figure 17 for waveform
Output Low Voltage	VOL	Vdd-1.84	Vdd-1.7	Vdd-1.62	V	See Figure 17 for waveform
Output Differential Voltage Swing	V_Swing		1.5	1.65	V	See Figure 18 for waveform
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	45	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±30	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 22 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	9	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 7
Power Supply-Induced Phase Noise	PSPN	–	-79	–	dBc	50 mV peak-peak ripple on VDD
		–	-92	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 7

Table 5. Electrical Characteristics – FlexSwing | Supply voltage ("order code") referred to VDD, only: 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See Figure 9 and Figure 10 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	36.5	45	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44	55	mA	Including load termination current, for FlexSwing order code "ER". See Figure 29 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms
		–	44	51	mA	Including load termination current, for FlexSwing order code "ER". See Figure 29 for Vdd=2.5 V ±10%, and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	49.5	60.5	mA	Including load termination current, for FlexSwing order code "ER". See Figure 29 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	49.5	57	mA	Including load termination current, for FlexSwing order code "ER". See Figure 29 for Vdd=2.5 V ±10%, and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn -0.13	VHn	VHn +0.1	V	See Figure 17 for waveform; Refer to Table 17 or Table 18 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn -0.13	VLn	VLn +0.12	V	See Figure 17 for waveform; Refer to Table 17 or Table 18 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 18 for waveform
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	55	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 22 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "ER"
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "ER". Using RC power supply filter as shown in Figure 9
Power Supply-Induced Phase Noise	PSPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "ER"
		–	-93	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "ER". Using RC power supply filter as shown in Figure 9

Table 6. Electrical Characteristics – FlexSwing | Supply voltage ("order code") referred to GND, only: 1.8 V ±5% ("18"), 1.71 V to 3.63 V ("YY"). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See Figure 9 and Figure 10 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	38	45	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	45.5	51	mA	Including load termination current, for FlexSwing order code "3E". See Figure 29 for Vdd=1.8 V ±5% and R3=220 Ohms
		–	45.5	52.5	mA	Including load termination current, for FlexSwing order code "3E". See Figure 29 for Vdd=1.71 V to 3.63 V and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	51.5	57.5	mA	Including load termination current, for FlexSwing order code "3E". See Figure 29 for Vdd=1.8 V ±5% and R3=220 Ohms. Driver output is at logic-high voltage levels.
		–	51.5	59	mA	Including load termination current, for FlexSwing order code "3E". See Figure 29 for Vdd=1.71 V to 3.63 V and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn – 0.1	VHn	VHn + 0.12	V	See Figure 17 for waveform; Refer to Table 17 or Table 18 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn – 0.1	VLn	VLn + 0.12	V	See Figure 17 for waveform; Refer to Table 17 or Table 18 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 18 for waveform
Rise/Fall Time	Tr, Tf	–	170	210	ps	20% to 80%. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 22 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	12	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "3E"
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "3E". Using RC power supply filter as shown in Figure 9
Power Supply-Induced Phase Noise	PSPN	–	-76	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "3E"
		–	-95	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "3E". Using RC power supply filter as shown in Figure 9

Table 7. Electrical Characteristics – FlexSwing | Supply voltage ("order code") referred to GND, only: 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal frequency of 156.25 MHz unless otherwise stated. See Figure 9 and Figure 10 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	37	43	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	44.5	51	mA	Including load termination current, for FlexSwing order code "VP". See Figure 29 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms
Current Consumption Output Disabled with Termination	Idd_od_wt	–	53	61	mA	Including load termination current, for FlexSwing order code "VP". See Figure 29 for Vdd=3.3 V ±10%, Vdd=2.25 V to 3.63 V, and R3=220 Ohms. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.11	VHn	VHn + 0.1	V	See Figure 17 for waveform; Refer to Table 17 or Table 18 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 17 for waveform; Refer to Table 17 or Table 18 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	-15%	2*(VHn-VLn)	+15%	V	See Figure 18 for waveform
Rise/Fall Time	Tr, Tf	–	170	200	ps	20% to 80%. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	60	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	12	–	%	Measured as percent of V_Swing. See Figure 22 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	14	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "VP"
		–	2	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. For FlexSwing order code "VP". Using RC power supply filter as shown in Figure 9
Power Supply-Induced Phase Noise	PSPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "VP"
		–	-93	–	dBc	50 mV peak-peak ripple on VDD. For FlexSwing order code "VP". Using RC power supply filter as shown in Figure 9

Table 8. Electrical Characteristics – LVDS | Supply voltage ("order code"): 2.5 V ±10% ("25"), 3.3 V ±10% ("33"), 2.25 V to 3.63 V ("XX"). All typical specifications are measured at nominal supply of 2.5 V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 11 and Figure 12 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32.5	39	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	36	42	mA	Including load termination current. See Figure 33 for termination
Current Consumption Output Disabled with Termination	Idd_od_wt	–	42	48	mA	Including load termination current. See Figure 33 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	360	450	mV	See Figure 19 for waveform
Delta VOD	ΔVOD	–	–	50	mV	See Figure 19 for waveform
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 19 for waveform
Delta VOS	ΔVOS	–	–	50	mV	See Figure 19 for waveform
Rise/Fall Time	Tr, Tf	–	290	330	ps	Measured 20% to 80% using Figure 33 for termination. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of VOD. See Figure 23 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	15	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 11
Power Supply-Induced Phase Noise	PSPN	–	-75	–	dBc	50 mV peak-peak ripple on VDD
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 11

Table 9. Electrical Characteristics – LVDS | Supply voltage (“order code”): 1.8 V ±5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 11 and Figure 12 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32.5	39	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	36	42	mA	Including load termination current. See Figure 33 for termination
Current Consumption Output Disabled with Termination	Idd_od_wt	–	42	48	mA	Including load termination current. See Figure 33 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	330	450	mV	See Figure 19 for waveform
Delta VOD	ΔVOD	–	–	50	mV	See Figure 19 for waveform
Offset Voltage	VOS	1.125	1.25	1.375	V	See Figure 19 for waveform
Delta VOS	ΔVOS	–	–	50	mV	See Figure 19 for waveform
Rise/Fall Time	Tr, Tf	–	290	330	ps	Measured 20% to 80% using Figure 33 for termination. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	25	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	8	–	%	Measured as percent of VOD. See Figure 23 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	17.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 11
Power Supply-Induced Phase Noise	PSPN	–	-73	–	dBc	50 mV peak-peak ripple on VDD
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 11

Table 10. Electrical Characteristics – HCSL | Supply voltage (“order code”): 2.5 V ±10% (“25”), 3.3 V ±10% (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V ±5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 13 and Figure 14 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32	38	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	46.5	52	mA	Including load termination current. See Figure 34 (a) and Figure 34 (b) for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	52.5	59	mA	Including load termination current. See Figure 34 (a) and Figure 34 (b) for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 17 for waveform
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 17 for waveform
Output Differential Voltage Swing	V_Swing	1.1	1.4	1.6	V	See Figure 18 for waveform
Rise/Fall Time	Tr, Tf	–	340	370	ps	Measured 20% to 80%. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	65	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±70	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	0	–	%	Measured as percent of V_Swing. See Figure 22 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	27	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	3.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 13
Power Supply-Induced Phase Noise	PSPN	–	-70	–	dBc	50 mV peak-peak ripple on VDD
		–	-88	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 13

Table 11. Electrical Characteristics – Low-Power HCSL | Supply voltage (“order code”): 2.5 V ±10% (“25”), 3.3 V ±10% (“33”), 2.25 V to 3.63 V (“XX”), 1.8 V ±5% (“18”), 1.71 V to 3.63 V (“YY”). All typical specifications are measured at nominal supply of 2.5V and nominal frequency of 156.25 MHz unless otherwise stated. See Figure 15 and Figure 16 for test setups.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, Frequency = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	33	38.5	mA	Excluding load termination current.
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	33.5	39	mA	Including load termination current. See Figure 35 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	35.5	42	mA	Including load termination current. See Figure 35 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 17 for waveform
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 17 for waveform
Output Differential Voltage Swing	V_Swing	1.6	1.83	2.0	V	See Figure 18 for waveform
Rise/Fall Time	Tr, Tf	–	330	380	ps	Measured 20% to 80%. See Figure 18 for waveform
Differential Asymmetry, peak-peak	V_da	–	55	–	mV	See Figure 20 for waveform
Differential Skew, peak	V_ds	–	±30	–	ps	See Figure 21 for waveform
Overshoot Voltage, peak	V_ov	–	1	–	%	Measured as percent of V_Swing. See Figure 22 for waveform
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity	PSJS	–	18	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz
		–	6.5	–	fs/mV	Power supply ripple from 10 kHz to 20 MHz. Using RC power supply filter as shown in Figure 15
Power Supply-Induced Phase Noise	PSPN	–	-73	–	dBc	50 mV peak-peak ripple on VDD
		–	-82	–	dBc	50 mV peak-peak ripple on VDD. Using RC power supply filter as shown in Figure 15

Table 12. Absolute Maximum Ratings

Operation outside the absolute maximum ratings may cause permanent damage to the part.
Performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	135	°C

Table 13. Thermal Considerations[5]

Package	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	θ_{JB} (°C/W)	$\theta_{JC,Top}$ (°C/W)
3225, 6-pin	101	4.7	23	86
2520, 6-pin	111	3.7	24	116
2016, 6-pin	134	3.4	24	147

Notes:

5. θ_{JA}, Ψ_{JT}, θ_{JB} and θ_{JC} are provided according to JEDEC standards 51-2A, 51-7, 51-8, and 51-12.01 with a 25C ambient and 250 mW power consumption (typical of 1 GHz f_{out}). The conduction thermal resistances θ_{JB} and θ_{JC} are obtained with the assumption that all heat flows from the junction to a heat sink through either the solder pads (θ_{JB}) or the top of the package ($\theta_{JC,Top}$). These may be used in a two-resistor compact model. The values of θ_{JA} and Ψ_{JT} are strongly application dependent, and we report values based on the JEDEC thermal environment. θ_{JA} is the thermal resistance to ambient on a JEDEC PCB - it is a highly conservative estimate, since the JEDEC board does not have vias to PCB planes in the vicinity of the package. Ψ_{JT} can be used to estimate the junction temperature from measurements of the temperature at the top of the package, if the thermal environment is similar to the JEDEC environment.

Table 14. Maximum Operating Junction Temperature[6]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	85°C
85°C	100°C
95°C	110°C
105°C	120°C

Notes:

6. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 15. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)[7]	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Notes:

7. Please refer to SiTime Manufacturing Notes.

Pin Description

Table 16. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H[8]: Specified frequency output L[9]: OUT: Logic HIGH,
		No Function (NF)	Open, 120 kΩ internal pull-down resistor to GND
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions.[10]
3	GND	Power	Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[11]

Top View

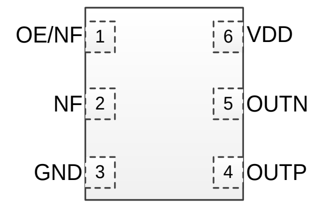


Figure 3. Pin Assignments

Notes:

8. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, the OE pin is recommended to include an external 10 kΩ resistor (Use 10kΩ pull-up if active high OE; use 10kΩ pull-down if active low OE) when the pin is not externally driven.
9. Differential Logic high means OUTP=VOH, OUTN=VOL.
10. Can be left open. SiTime recommends grounding it for better thermal performance.
11. A capacitor of value 0.1 µF or higher between VDD and GND pins is required.

"4-16A" Phase Jitter Methodology

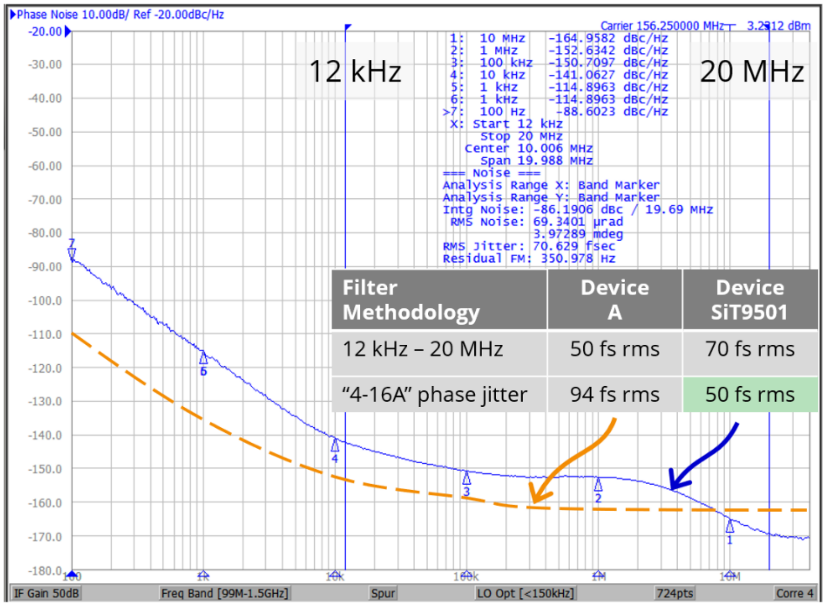


Figure 4:Two products analyzed with 2 different methodologies lead to opposite conclusions. The "4-16A" phase jitter methodology more accurately models modern SerDes applications.

Proper evaluation of reference clock (refclk) jitter is critical to optimize system performance in high-speed serial links. Fig. 1 shows how the traditional 12 kHz to 20 MHz analysis of filtering refclk jitter can mislead designers to select components that degrade rather than improve link performance. Using a more accurate filter analysis shows a roughly 50% reduction (50 vs 94 fs rms) in system jitter. Therefore, this datasheet replaces the legacy 12 kHz to 20 MHz filter analysis with a more accurate and established methodology adopted by several industry standards (e.g. PCI Express, CXL, UCIe) and referred to here as "4-16A" phase jitter. A brief overview follows.

Established in 1991 for SONET OC-48 line rates, the traditional 12 kHz to 20 MHz jitter filter served as a golden reference to evaluate refclk jitter for over 30 years. The filter is used is nearly all clock and timing datasheets today. However, the results it provides no longer correlate with system performance and can create suboptimum link performance. Sources of filter error include incorrect corner frequencies, unrealistic brick-wall roll offs and a lack of accounting for aliased phase noise. Errors of tens of femtoseconds are significant today and will become more significant as data rates increase. For these reasons, we recommend customers adopt the more accurate "4-16A" phase jitter methodology for SerDes applications.

The conventional refclk jitter analysis uses a band-pass filter, as shown in Fig. 2, to extract the refclk contribution to jitter observed at the receiver. Historically the refclk jitter filter was arbitrarily applied to phase noise up to an offset equal to the refclk Nyquist frequency. However, this ignores higher-offset phase noise that aliases when the refclk is sampled by a PLL's phase detector. Studies have shown that extending the phase noise data flat to the third harmonic (or, twice the fundamental frequency in the offset-frequency axis) derives an accurate estimate of worst-case phase jitter [1]. Above the third harmonic, phase noise rolls off quickly and can be ignored.

[1] "How to evaluation reference-clock phase noise in high-speed serial links", Signal Integrity Journal, https://www.signalintegrityjournal.com/articles/1216-methodology-for-analyzing-reference-clock-phase-noise-in-high-speed-serial-links

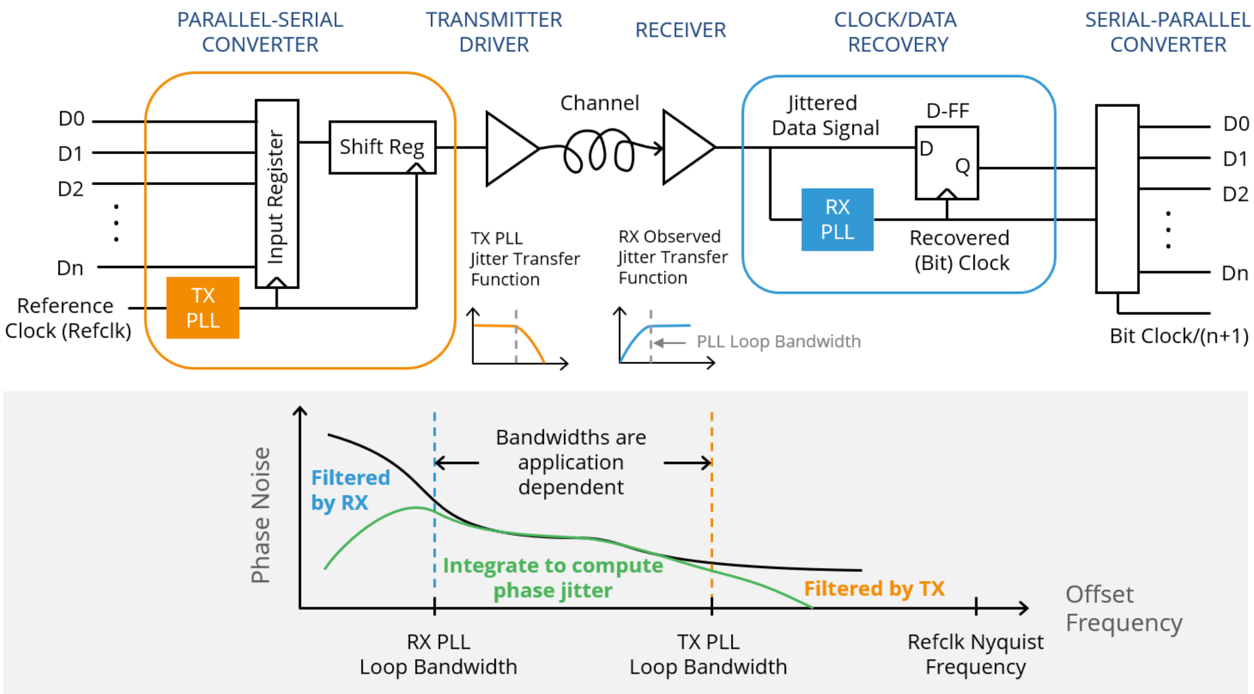


Figure 5:A generic serial link (top) uses a transmit PLL and receive CDR to low and high pass filter, respectively, refclk phase noise. This forms a band-pass system filter (bottom) for computing phase jitter.

The left Fig. 3 chart illustrates this methodology of filtering aliased phase noise for a 156.25 MHz clock. Phase noise analyzers include an anti-aliasing filter. Thus, to account for aliasing, the phase noise is extended flat to the 3rd harmonic (468.75 MHz in the signal spectrum, which is 312.5 MHz in offset frequency) and the jitter filter is mirrored across Nyquist-zone boundaries (at 156.25/2, 156.25 and 156.25×3/2 MHz). Then the phase noise data is filtered and integrated to derive phase jitter. The right Fig. 3 chart illustrates a mathematically equivalent process that aliases the extended phase noise below an offset equal to the Nyquist frequency before filtering. [1]

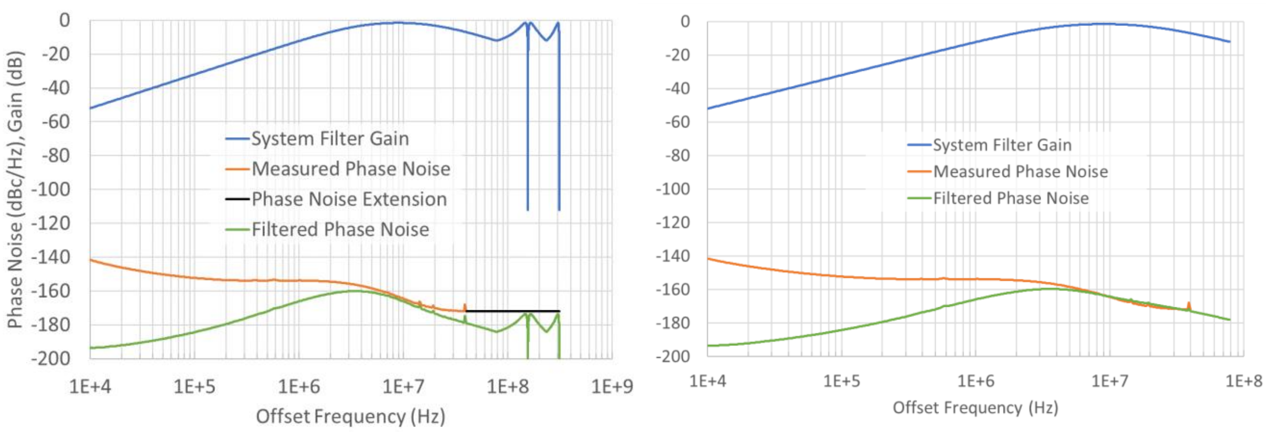


Figure 6:Illustration of two equivalent processes to filter aliased phase noise. The left chart extends (black) the measured phase noise (orange) to the 3rd harmonic, mirrors the filter (blue) across higher Nyquist zones before deriving the filtered phase noise (green). Alternatively, the right chart aliases the extended phase noise (not shown) below Nyquist before filtering (green). Integrating either green curve yields the same value of phase jitter.

A shorthand label for this methodology is “#-#A” phase jitter where the first and second numbers “#” are replaced with RX CDR and TX PLL bandwidths, respectively, with 20 dB/dec roll offs. The “A” indicates that aliasing is included. For example, “4-16A” phase jitter uses 4 MHz RX and 16 MHz TX bandwidths. Here, 4 MHz represents the most common serial standard, Ethernet, which typically specifies a CDR bandwidth of 4 MHz for 10 Gbps and higher link rates, and 16 MHz represents a worst-case estimate for TX PLL bandwidth. Adopting such a terminology makes it easy to describe variations. For example, “2-10A” phase jitter describes the same methodology but for 2 MHz RX CDR and 10 MHz TX PLL bandwidths. The actual bandwidths are application dependent, and “4-16A” is simply chosen here to represent the most common application (Ethernet).

FlexSwing Configurations

A FlexSwing output-driver performs like LVPECL and additionally provides independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDD or GND pins.

Table 17. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on VDD pin

Order Code V_Swing (V) — VHn (VLn + V_Swing / 2) ↓ / VLn →	A Vdd-2.31V	B Vdd-2.26V	C Vdd-2.21V	D Vdd-2.16V	E Vdd-2.11V	F Vdd-2.06V	G Vdd-2.01V	H Vdd-1.96V	J Vdd-1.91V	K Vdd-1.86V	L Vdd-1.82V	M Vdd-1.77V	N Vdd-1.72V	P Vdd-1.67V	Q Vdd-1.62V	R Vdd-1.57V	S Vdd-1.52V	T Vdd-1.47V	U Vdd-1.42V	V Vdd-1.37V	W Vdd-1.32V	X Vdd-1.28V
A									AJ 1.94	AK 1.86	AL 1.77	AM 1.69	AN 1.61	AP 1.52	AQ 1.44	AR 1.35	AS 1.27	AT 1.18	AU 1.10	AV 1.01	AW 0.93	AX 0.85
B								1.94	BJ 1.86	BK 1.77	BL 1.69	BM 1.61	BN 1.52	BP 1.44	BQ 1.35	BR 1.27	BS 1.18	BT 1.10	BU 1.01	BV 0.93	BW 0.85	BX 0.76
C							1.94	1.86	CJ 1.77	CK 1.69	CL 1.61	CM 1.52	CN 1.44	CP 1.35	CQ 1.27	CR 1.18	CS 1.10	CT 1.01	CU 0.93	CV 0.85	CW 0.76	CX 0.68
D						1.94	1.86	1.77	DJ 1.69	DK 1.61	DL 1.52	DM 1.44	DN 1.35	DP 1.27	DQ 1.18	DR 1.10	DS 1.01	DT 0.93	DU 0.85	DV 0.76	DW 0.68	DX 0.59
E					1.94	1.86	1.77	1.69	EJ 1.61	EK 1.52	EL 1.44	EM 1.35	EN 1.27	EP 1.18	EQ 1.10	ER 1.014	ES 0.93	ET 0.85	EU 0.76	EV 0.68	EW 0.59	EX 0.51
F				1.94	1.86	1.77	1.69	1.61	FJ 1.52	FK 1.44	FL 1.35	FM 1.27	FN 1.18	FP 1.10	FQ 1.01	FR 0.93	FS 0.85	FT 0.76	FU 0.676	FV 0.59	FW 0.51	0.42
G			1.94	1.86	1.77	1.69	1.61	GH 1.52	GJ 1.44	GK 1.35	GL 1.27	GM 1.18	GN 1.10	GP 1.01	GQ 0.93	GR 0.85	GS 0.76	GT 0.68	GU 0.59	GV 0.51	0.42	0.34
H		1.94	1.86	1.77	1.69	1.61	HG 1.52	HH 1.44	HJ 1.35	HK 1.27	HL 1.18	HM 1.10	HN 1.01	HP 0.93	HQ 0.85	HR 0.76	HS 0.68	HT 0.59	HU 0.51	0.42	0.34	0.25
J	1.94	1.86	1.77	1.69	1.61	JF 1.52	JG 1.44	JH 1.35	JJ 1.27	JK 1.18	JL 1.10	JM 1.01	JN 0.93	JP 0.85	JQ 0.76	JR 0.68	JS 0.59	JT 0.51	0.42	0.34	0.25	
K	1.86	1.77	1.69	1.61	KE 1.52	KF 1.44	KG 1.35	KH 1.27	KJ 1.18	KK 1.10	KL 1.01	KM 0.93	KN 0.85	KP 0.76	KQ 0.68	KR 0.59	KS 0.51	0.42	0.34	0.25		
L	1.77	1.69	1.61	LD 1.52	LE 1.44	LF 1.35	LG 1.27	LH 1.18	LJ 1.10	LK 1.01	LL 0.93	LM 0.85	LN 0.76	LP 0.68	LQ 0.59	LR 0.51	0.42	0.34	0.25			
M	1.69	1.61	MC 1.52	MD 1.44	ME 1.35	MF 1.27	MG 1.18	MH 1.10	MJ 1.01	MK 0.93	ML 0.85	MM 0.76	MN 0.68	MP 0.59	MQ 0.51	0.42	0.34	0.25				
N	1.61	NB 1.52	NC 1.44	ND 1.35	NE 1.27	NF 1.18	NG 1.10	NH 1.01	NJ 0.93	NK 0.85	NL 0.76	NM 0.68	NN 0.59	NP 0.51	0.42	0.34	0.25					
P	PA 1.52	PB 1.44	PC 1.35	PD 1.27	PE 1.18	PF 1.10	PG 1.01	PH 0.93	PJ 0.85	PK 0.76	PL 0.68	PM 0.59	PN 0.51	0.42	0.34	0.25						
Q	QA 1.44	QB 1.35	QC 1.27	QD 1.18	QE 1.10	QF 1.01	QG 0.93	QH 0.85	QJ 0.76	QK 0.68	QL 0.59	QM 0.51	0.42	0.34	0.25							
R	RA 1.35	RB 1.27	RC 1.18	RD 1.10	RE 1.01	RF 0.93	RG 0.85	RH 0.76	RJ 0.68	RK 0.59	RL 0.51	0.42	0.34	0.25								
S	SA 1.27	SB 1.18	SC 1.10	SD 1.01	SE 0.93	SF 0.85	SG 0.76	SH 0.68	SJ 0.59	SK 0.51	0.42	0.34	0.25									
T	TA 1.18	TB 1.10	TC 1.01	TD 0.93	TE 0.85	TF 0.76	TG 0.68	TH 0.59	TJ 0.51	0.42	0.34	0.25										
U	UA 1.10	UB 1.01	UC 0.93	UD 0.85	UE 0.76	UF 0.68	UG 0.59	UH 0.51	0.42	0.34	0.25											
V	VA 1.01	VB 0.93	VC 0.85	VD 0.76	VE 0.68	VF 0.59	VG 0.51	0.42	0.34	0.25												
W	WA 0.93	WB 0.85	WC 0.76	WD 0.68	WE 0.59	WF 0.51	0.42	0.34	0.25													

Supply Voltage	Available Colors	
1.8V±5%	Not Supported	
1.71V to 3.63V	Not Supported	
2.5V±10%	Blue	
3.3V±10%	Blue	Red
2.25V to 3.63V	Blue	
Note 12	Gray	

Note:

12. Please contact SiTime.

The above table identifies supported combinations of nominal VOH (i.e. VHn) and nominal VOL (i.e. VLn) in colored boxes. The two-character code in each box corresponds to the VHn and VLn codes specified in the 2nd column and 2nd row in the table, respectively. The number in each box indicates the nominal differential swing (i.e. 2x VHn – VLn).

For example, order code "FS" selects VHn code "F" (i.e. Vdd-1.095 V) and VLn code "S" (i.e. Vdd-1.520 V) corresponding to a V_Swing of 0.85 V peak-peak, which may be used for supply voltages of 2.5 V ±10%, 3.3 V ±10% or (2.25 V to 3.63 V). Alternatively, an order code of "GS" corresponds to a VHn code "G" (i.e. Vdd-1.14 V) and a VLn order code "S" (e.g. Vdd-1.520 V) corresponding to a V_Swing of 0.760 V peak-peak, which may be used for a supply voltage of 3.3 V ±10%.

Table 18. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on GND pin

Supply Voltage	Available Colors			
1.8V±5%	Orange	Green		
1.71V to 3.63V	Green			
2.5V±10%	Orange	Green	Blue	Purple
3.3V±10%	Green	Blue	Red	
2.25V to 3.63V	Green	Blue		
Note 13	Gray			

Order Code V_Swing (V) → VHn ↓ / VLn + V_Swing / 2	C 0.45V	D 0.49V	E 0.54V	F 0.59V	G 0.64V	H 0.69V	J 0.74V	K 0.79V	L 0.84V	M 0.89V	N 0.94V	P 0.99V	Q 1.03V	R 1.08V	S 1.16V	T 1.23V	U 1.3V	V 1.38V	W 1.45V	X 1.53V	Y 1.6V
A																		AV 1.94	AW 1.86	AX 1.69	AY 1.61
B																		BV 1.86	BW 1.77	BX 1.61	BY 1.52
C																	CU 1.94	CV 1.77	CW 1.69	CX 1.52	CY 1.44
D																DT 1.94	DU 1.86	DV 1.69	DW 1.61	DX 1.44	DY 1.35
E																ET 1.86	EU 1.77	EV 1.61	EW 1.52	EX 1.35	EY 1.27
F															FS 1.94	FT 1.77	FU 1.69	FV 1.52	FW 1.44	FX 1.27	FY 1.18
G														1.94	GS 1.86	GT 1.69	GU 1.61	GV 1.44	GW 1.35	GX 1.18	GY 1.10
H													1.94	1.86	HS 1.77	HT 1.61	HU 1.52	HV 1.35	HW 1.27	HX 1.10	HY 1.01
J												1.94	1.86	1.77	JS 1.69	JT 1.52	JU 1.44	JV 1.27	JW 1.18	JX 1.01	JY 0.93
K											1.94	1.86	1.77	1.69	KS 1.61	KT 1.44	KU 1.35	KV 1.18	KW 1.10	KX 0.93	KY 0.85
L										1.94	1.86	1.77	1.69	1.61	LS 1.52	LT 1.35	LU 1.27	LV 1.10	LW 1.01	LX 0.85	LY 0.76
M									1.94	1.86	1.77	1.69	1.61	MR 1.52	MS 1.44	MT 1.27	MU 1.18	MV 1.01	MW 0.93	MX 0.76	MY 0.68
N								1.94	1.86	1.77	1.69	1.61	NQ 1.52	NR 1.44	NS 1.35	NT 1.18	NU 1.10	NV 0.93	NW 0.85	NX 0.68	NY 0.59
P							1.94	1.86	1.77	1.69	1.61	PP 1.52	PQ 1.44	PR 1.35	PS 1.27	PT 1.10	PU 1.01	PV 0.85	PW 0.76	PX 0.59	PY 0.51
Q						1.94	1.86	1.77	1.69	1.61	QN 1.52	QP 1.44	QQ 1.35	QR 1.27	QS 1.18	QT 1.01	QU 0.93	QV 0.76	QW 0.68	QX 0.51	0.42
R					1.94	1.86	1.77	1.69	1.61	RM 1.52	RN 1.44	RP 1.35	RQ 1.27	RR 1.18	RS 1.10	RT 0.93	RU 0.85	RV 0.68	RW 0.59	0.42	0.34
S				1.94	1.86	1.77	1.69	1.61	SL 1.52	SM 1.44	SN 1.35	SP 1.27	SQ 1.18	SR 1.10	SS 1.01	ST 0.85	SU 0.76	SV 0.59	SW 0.51	0.34	0.25
T			1.94	1.86	1.77	1.69	1.61	TK 1.52	TL 1.44	TM 1.35	TN 1.27	TP 1.18	TQ 1.10	TR 1.01	TS 0.93	TT 0.76	TU 0.68	TV 0.51	0.42	0.25	
U		1.94	1.86	1.77	1.69	1.61	UJ 1.52	UK 1.44	UL 1.35	UM 1.27	UN 1.18	UP 1.10	UQ 1.01	UR 0.93	US 0.85	UT 0.68	UU 0.59	0.42	0.34		
V	1.94	1.86	1.77	1.69	1.61	VH 1.52	VJ 1.44	VK 1.35	VL 1.27	VM 1.18	VN 1.10	VP 1.01	VQ 0.93	VR 0.85	VS 0.76	VT 0.59	VU 0.51	0.34	0.25		
W	1.86	1.77	1.69	1.61	WG 1.52	WH 1.44	WJ 1.35	WK 1.27	WL 1.18	WM 1.10	WN 1.01	WP 0.93	WQ 0.85	WR 0.76	WS 0.68	WT 0.51	0.42	0.25			
X	1.77	1.69	1.61	XF 1.52	XG 1.44	XH 1.35	XJ 1.27	XK 1.18	XL 1.10	XM 1.01	XN 0.93	XP 0.85	XQ 0.76	XR 0.68	XS 0.59	0.42	0.34				
Y	1.69	1.61	YE 1.52	YF 1.44	YG 1.35	YH 1.27	YJ 1.18	YK 1.10	YL 1.01	YM 0.93	YN 0.85	YP 0.76	YQ 0.68	YR 0.59	YS 0.51	0.34	0.25				
Z	1.61	ZD 1.52	ZE 1.44	ZF 1.35	ZG 1.27	ZH 1.18	ZJ 1.10	ZK 1.01	ZL 0.93	ZM 0.85	ZN 0.76	ZP 0.68	ZQ 0.59	ZR 0.51	0.42	0.25					
1	1C 1.52	1D 1.44	1E 1.35	1F 1.27	1G 1.18	1H 1.10	1J 1.01	1K 0.93	1L 0.85	1M 0.76	1N 0.68	1P 0.59	1Q 0.51	0.42	0.34						
2	2C 1.44	2D 1.35	2E 1.27	2F 1.18	2G 1.10	2H 1.01	2J 0.93	2K 0.85	2L 0.76	2M 0.68	2N 0.59	2P 0.51	0.42	0.34	0.25						
3	3C 1.35	3D 1.27	3E 1.18	3F 1.10	3G 1.01	3H 0.93	3J 0.85	3K 0.76	3L 0.68	3M 0.59	3N 0.51	0.42	0.34	0.25							

Note:

13. Please contact SiTime.

Test Circuit Diagrams

A 1.5 pF capacitive load is used at each differential output. Because of the additive input capacitance of the active probe used with the oscilloscope, the output characteristics for all signal types are measured with a total of 2 pF capacitive load.

Test Setups for LVPECL Measurements

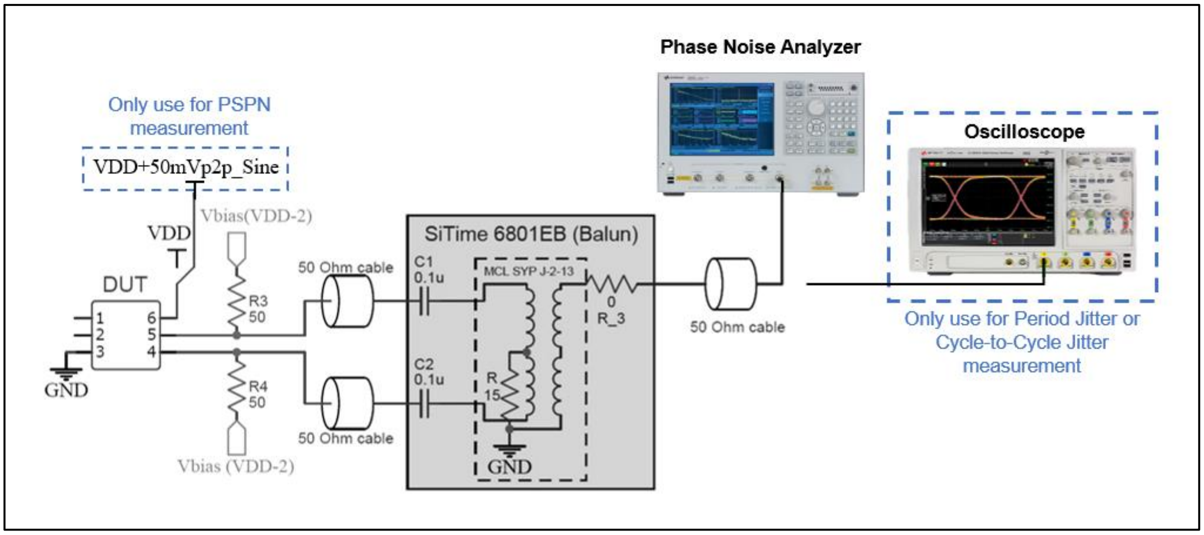


Figure 7. Test setup to measure LVPECL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) without filter added[14]

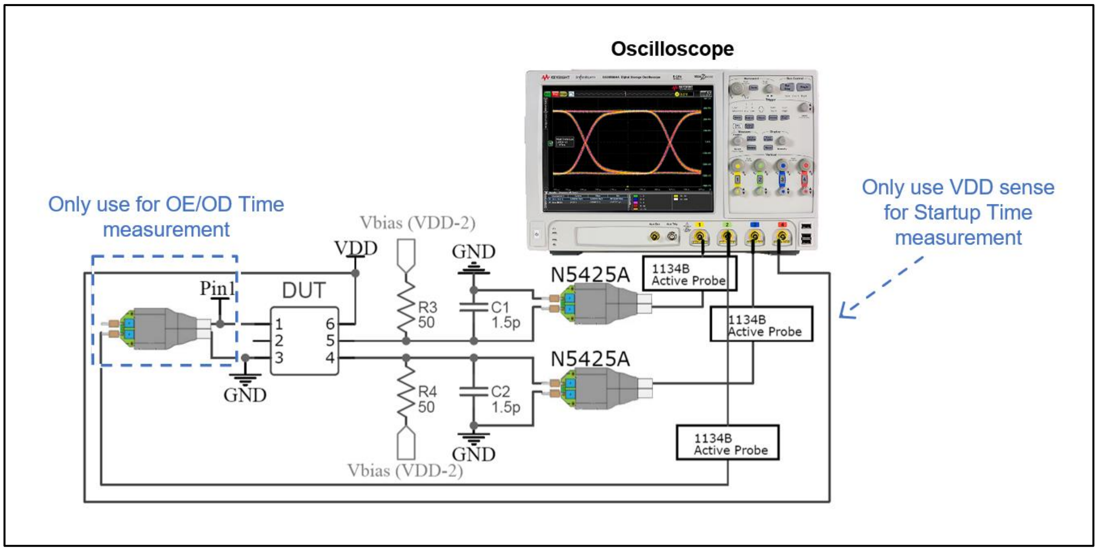


Figure 8. Test setup to measure LVPECL Waveform Characteristics, Current Consumption (with Termination 2)[15], Output Enable/Disable Time, and Startup Time

Notes:

14. See Figure 9 for the test setup to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
15. See Figure 10 for the test setup to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for FlexSwing Measurements[16]

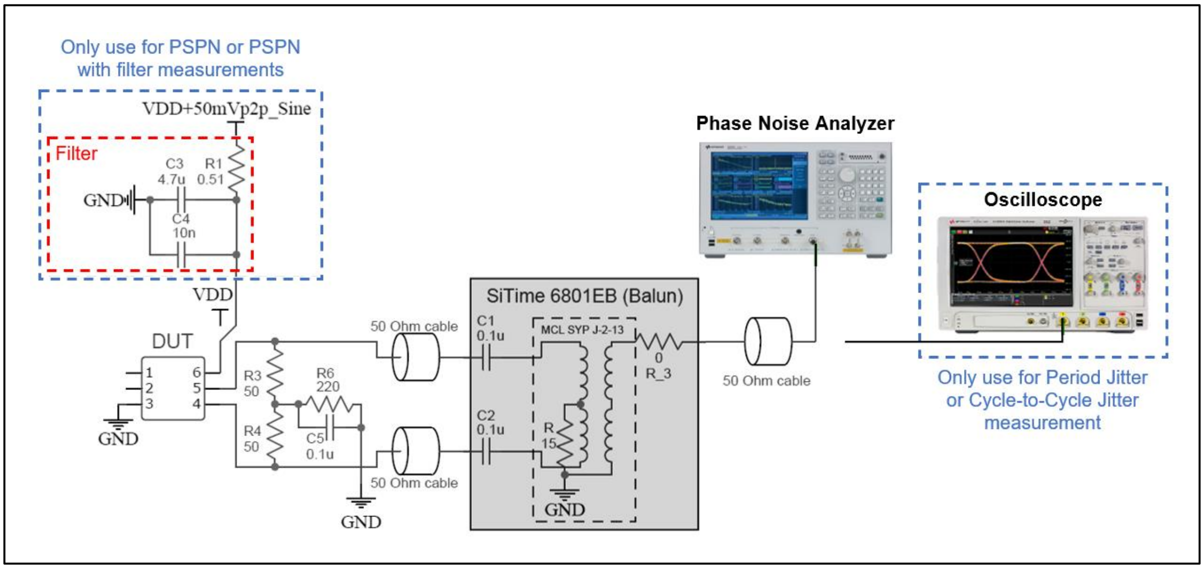


Figure 9. Test setup to measure FlexSwing Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added[17]

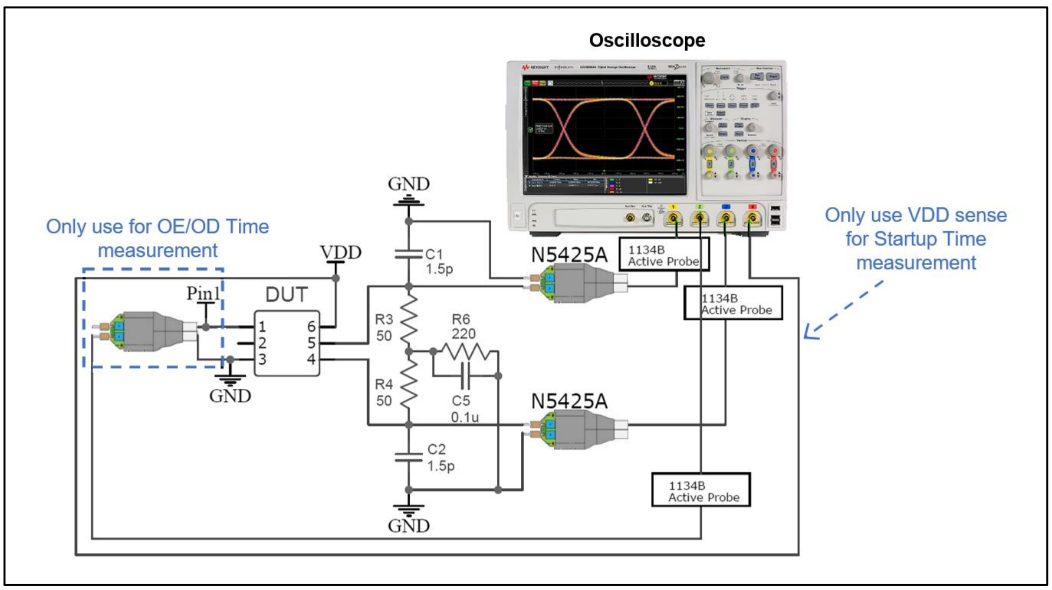


Figure 10. Test setup to measure FlexSwing Waveform Characteristics, Current Consumption[18], Output Enable/Disable Time, and Startup Time

Note:

16. The same test circuits are used for FlexSwing referenced to VDD and FlexSwing referenced to GND.
17. Test setup is also used to measure LVPECL Power Supply-Induced Phase Noise (PSPN) with filter added.
18. Test setup is also used to measure LVPECL Current Consumption with Termination 1 or without Termination.

Test Circuit Diagrams (continued)

Test Setups for LVDS Measurements

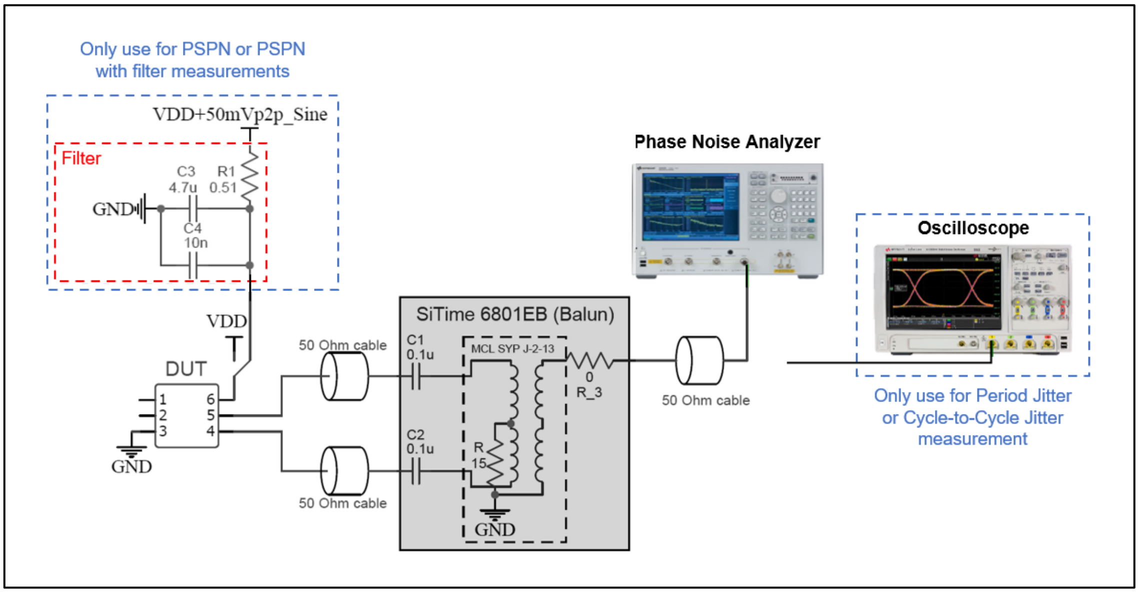


Figure 11. Test setup to measure LVDS Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

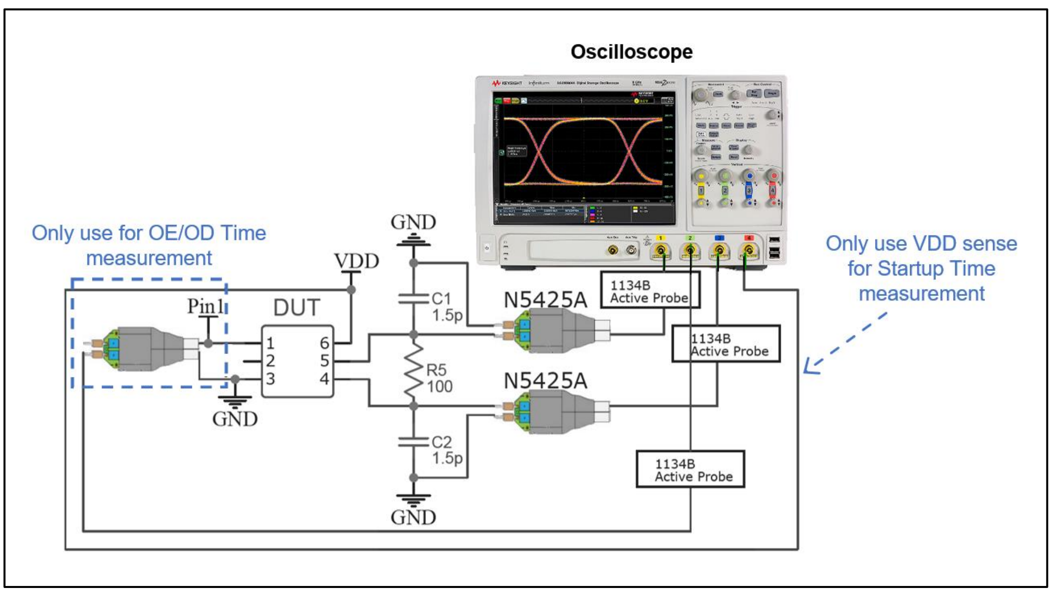


Figure 12. Test setup to measure LVDS Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for HCSL Measurements

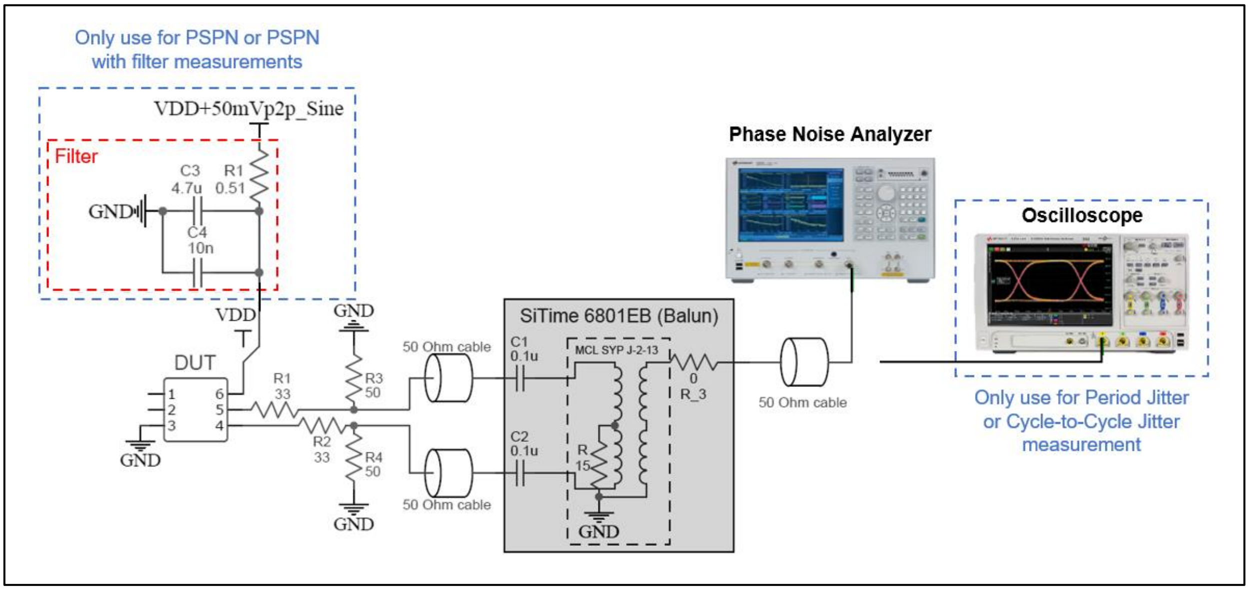


Figure 13. Test setup to measure HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

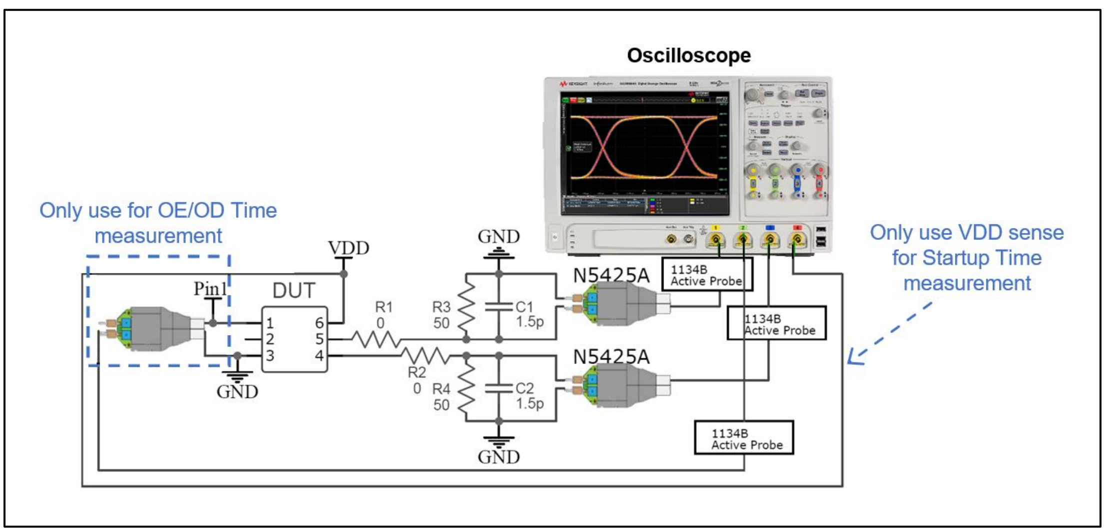


Figure 14. Test setup to measure HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Test Circuit Diagrams (continued)

Test Setups for Low-Power HCSL Measurements

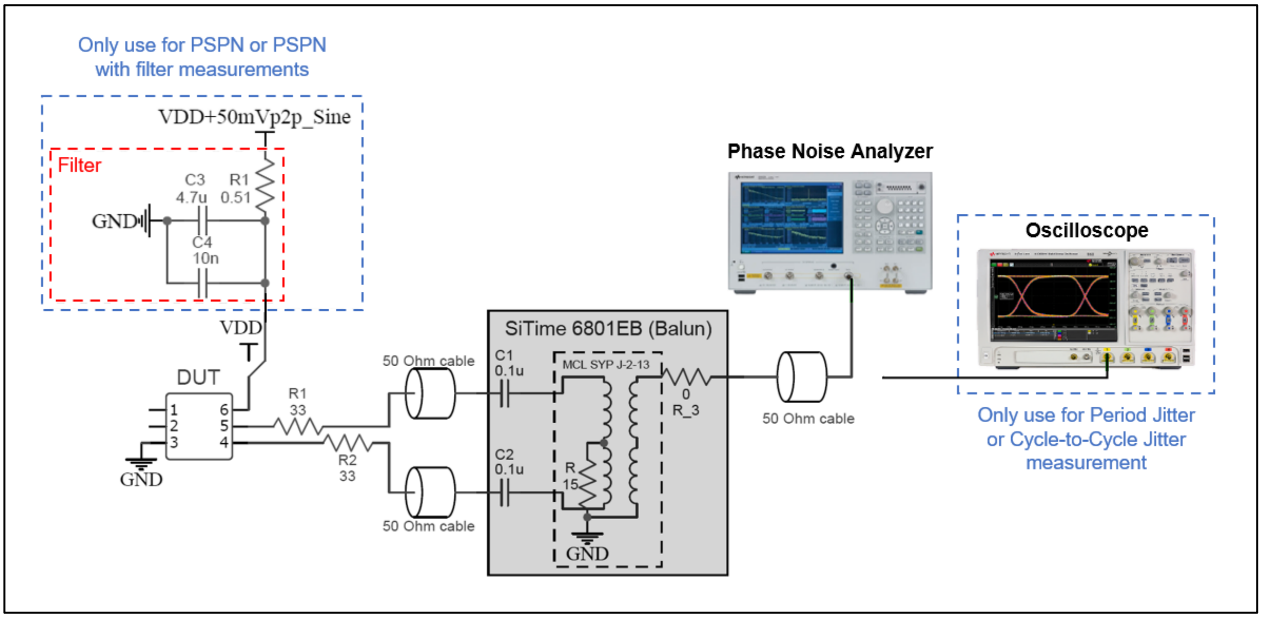


Figure 15. Test setup to measure Low-Power HCSL Phase Noise, Period Jitter, Cycle-to-Cycle Jitter, and Power Supply-Induced Phase Noise (PSPN) with and without filter added

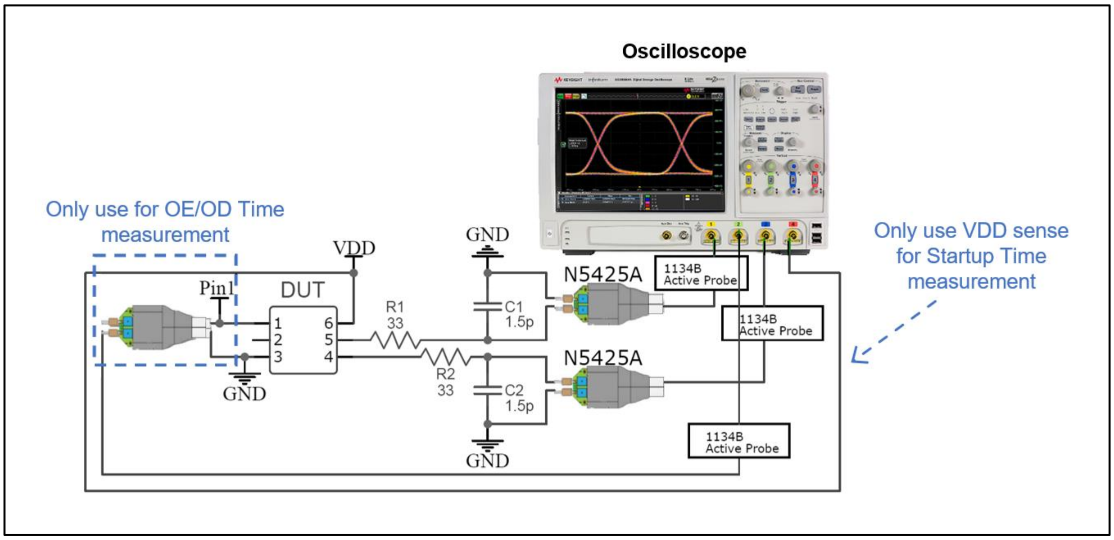


Figure 16. Test setup to measure Low-Power HCSL Waveform Characteristics, Current Consumption, Output Enable/Disable Time, and Startup Time

Waveform Diagrams

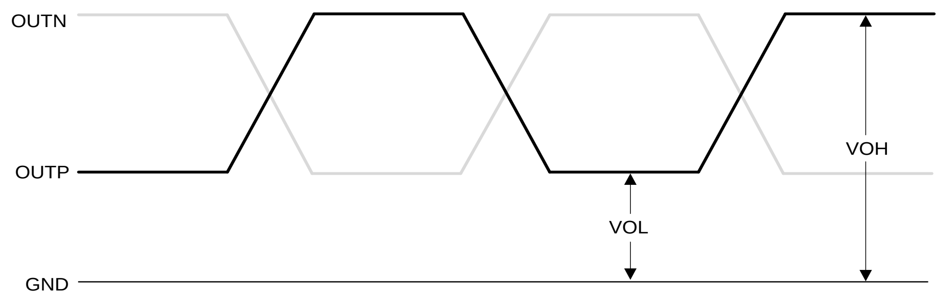


Figure 17. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

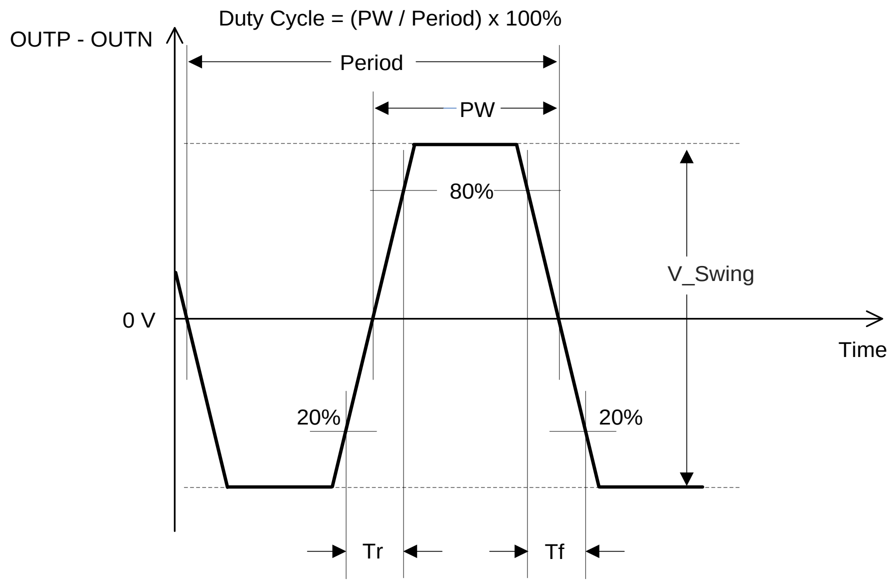


Figure 18. LVPECL, LVDS, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

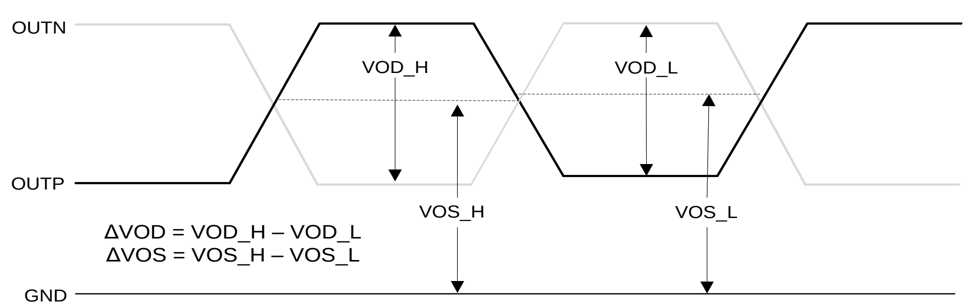


Figure 19. LVDS Voltage Levels per Differential Pin

Waveform Diagrams (continued)

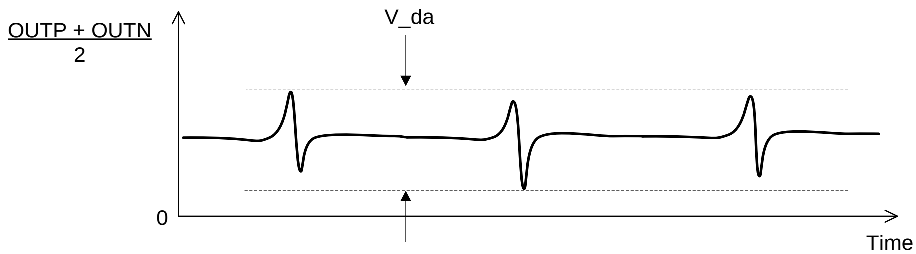


Figure 20. Differential Asymmetry (V_da)

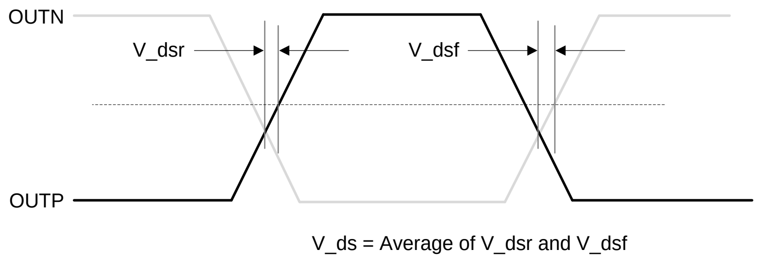


Figure 21. Differential Skew (V_ds) is measured as the Time between the Average Voltage Level and Crossing Voltage

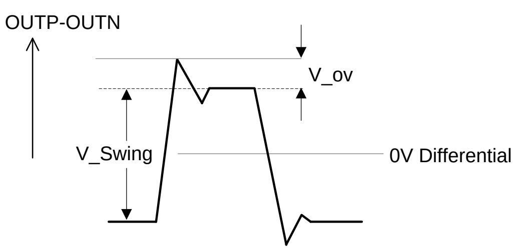


Figure 22. Overshoot Voltage (V_ov) for LVPECL, FlexSwing, HCSL, Low-power HCSL

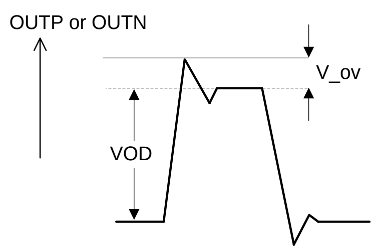


Figure 23. Overshoot Voltage (V_ov) for LVDS Output

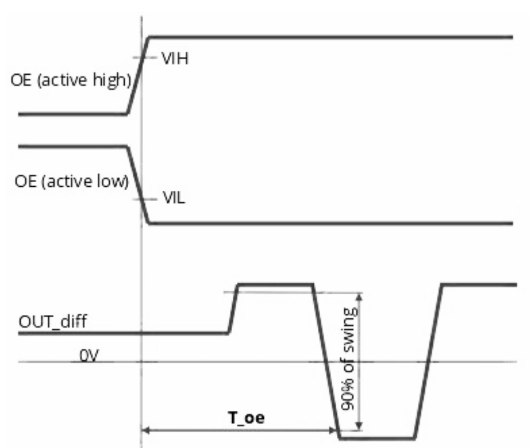


Figure 24. OE Pin Enable Timing (T_oe)

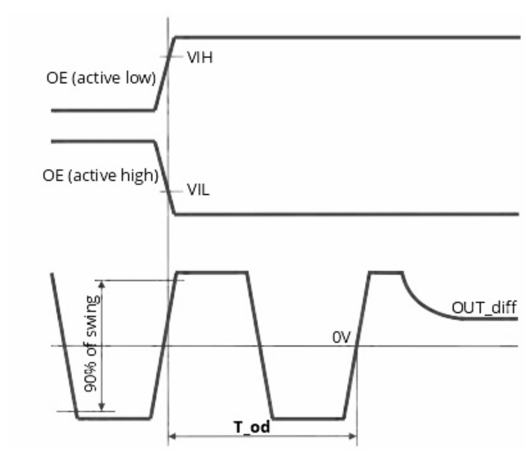


Figure 25. OE Pin Disable Timing (T_od)

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9375 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in Figure 27 and Figure 29, compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_load) into the load termination.

Table 19. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage Order Codes	Termination Options					
		Figure 26	Figure 27	Figure 28	Figure 29	Figure 30	Figure 31
LVPECL referenced to Vdd	"25", "33", "XX"	OK to use I_load = 40 mA with 100 Ω near-end bias resistor	**Do Not Use**	OK to use I_load = 28 mA	OK to use	OK to use I_load = 28 mA	**Do Not Use**
FlexSwing referenced to Vdd		OK to use[19]	OK to use (See Figure 27 for frequency ranges and voltage swings)	OK to use[20]	OK to use	OK to use	**Do Not Use**
FlexSwing referenced to Gnd	"25", "33", "XX", "YY"			**Do Not Use**	OK to use	**Do Not Use**	**Do Not Use**
	"18"			**Do Not Use**	OK to use	**Do Not Use**	OK to use

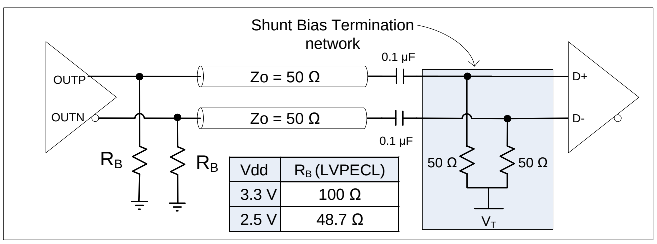


Figure 26. Recommended LVPECL and FlexSwing[19] Termination when AC-coupled

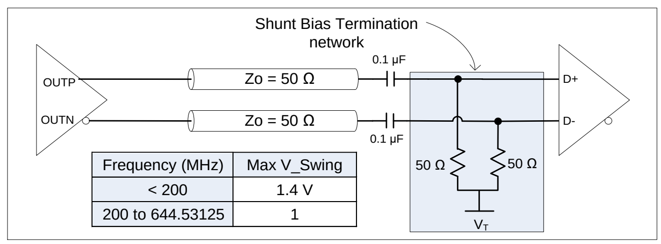


Figure 27. Recommended FlexSwing Termination when AC-coupled

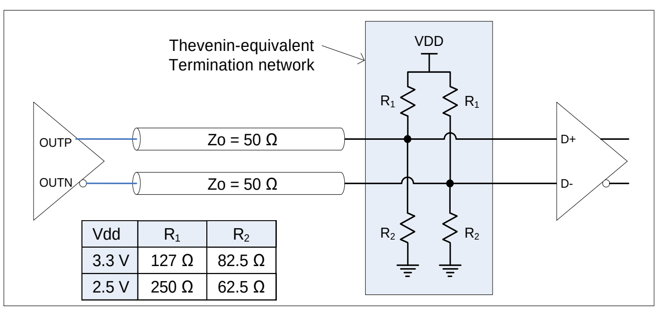


Figure 28. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network[20]

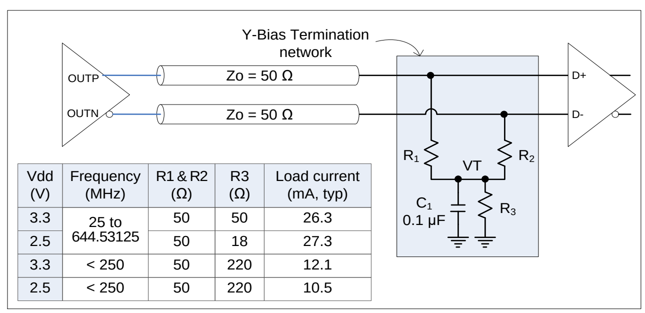


Figure 29. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

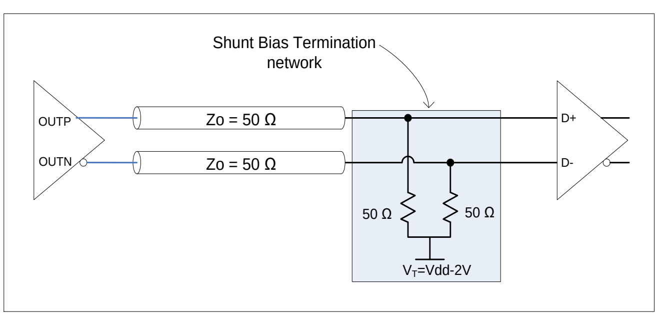


Figure 30. LVPECL and FlexSwing with Y-Bias Termination

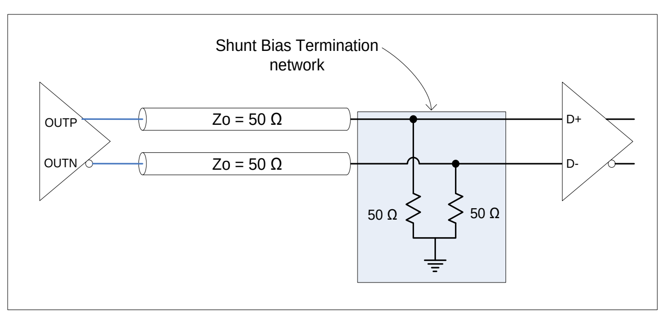


Figure 31. FlexSwing Termination – Only for use with Supply Voltage Order Code "18"

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

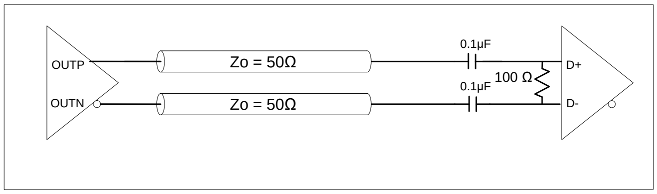


Figure 32. LVDS AC Termination

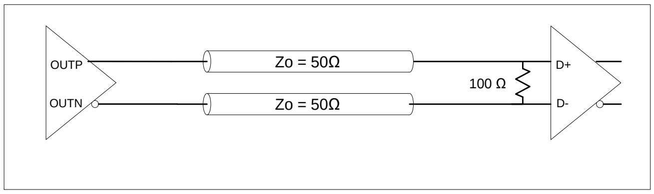
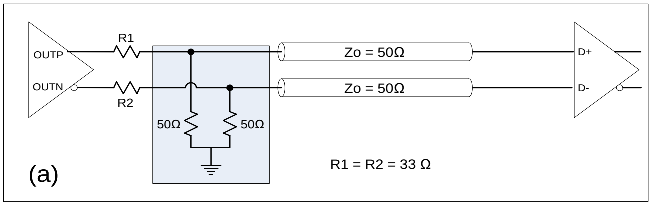


Figure 33. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V



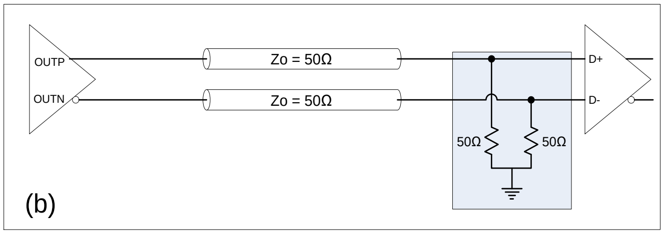


Figure 34. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

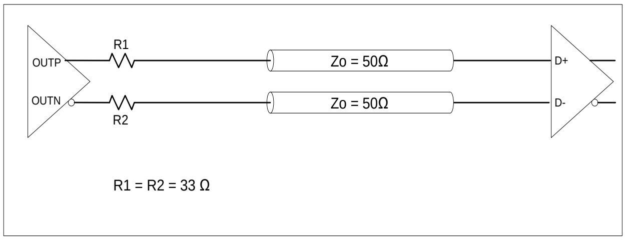


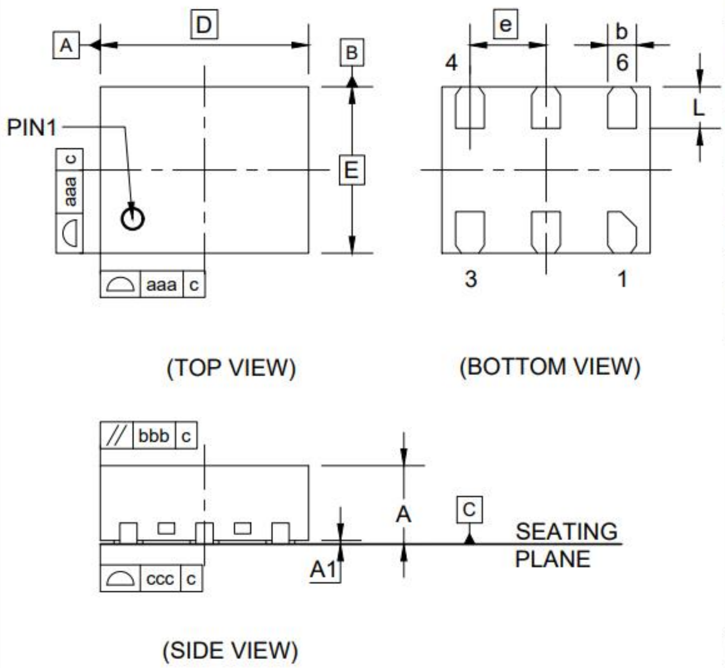
Figure 35. Low-power HCSL Termination

Notes:

19. Contact SiTime for optimum R_B values for FlexSwing options.
20. Contact SiTime for optimum R1 and R2 values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

Package Size – Dimensions (Unit: mm)[21]



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		2.000 BSC	
	Y	E		1.600 BSC	
LEAD WIDTH		b	0.225	0.275	0.325
LEAD LENGTH		L	0.300	0.400	0.500
LEAD PITCH		e		0.730 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

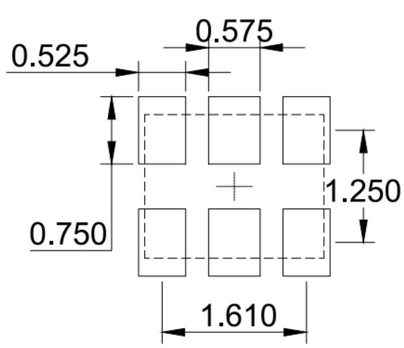
NOTE

1. ALL DIMENSION IN MM

SiTime

PKG INFO		DRAWING NO.	
6L PQFN 2.000x1.600x0.750 mm		POD-077-PQFN-006-C02016	
		REV	SHEET
DATE	12/6/2021	B02	01

Recommended Land Pattern (Unit: mm)[22]



Note : All units in mm.

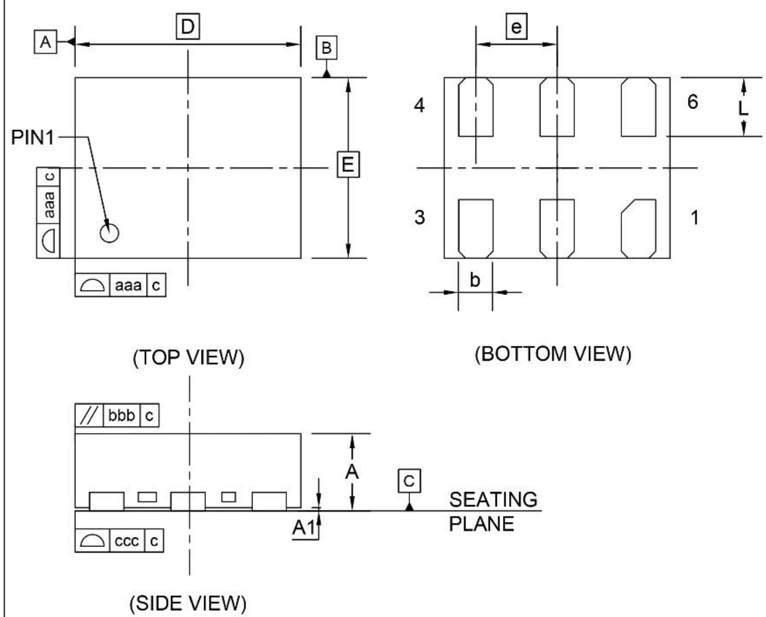
SiTime	PKG INFO	SPL DRAWING NO.	
	6L QFN 2.000x1.600 mm	SPL-077-QFN-006-C02016	
DATE		REV	SHEET
2020/04/20		B00	01

Notes:

21. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
22. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.

Dimensions and Patterns — 2.5 x 2.0 mm x mm

Package Size – Dimensions (Unit: mm)[21]



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		2.500 BSC	
	Y	E		2.000 BSC	
LEAD WIDTH		b	0.330	0.380	0.430
LEAD LENGTH		L	0.550	0.650	0.750
LEAD PITCH		e		0.900 BSC	
PACKAGE TOLERANCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

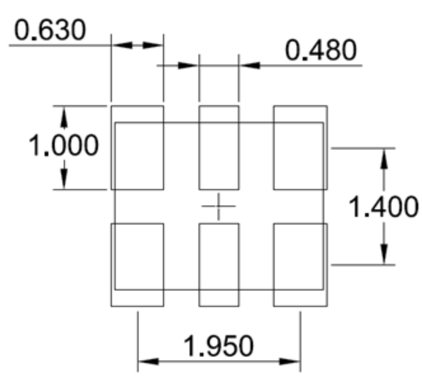
NOTE

1. ALL DIMENSION IN MM

SiTime

PKG INFO		DRAWING NO.	
6L PQFN 2.500x2.000x0.850 mm		POD-092-PQFN-006-C02520	
		REV	SHEET
DATE	2/28/2024	A01	01

Recommended Land Pattern (Unit: mm)[22]

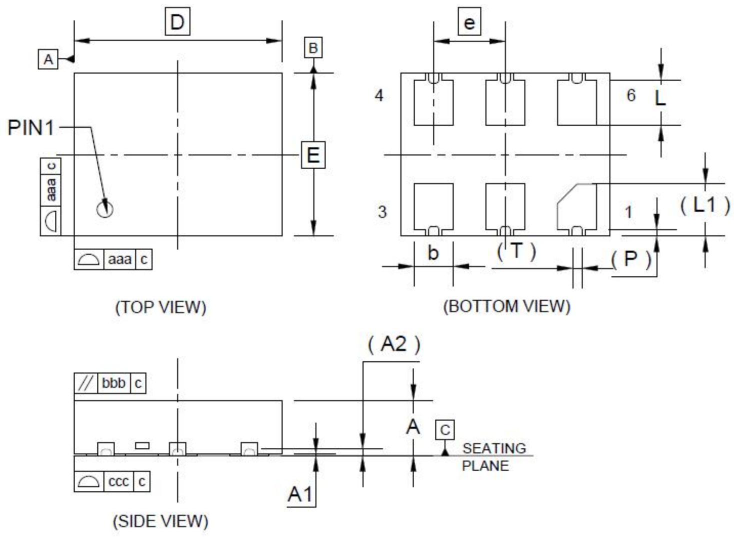


Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
		SPL-078-PQFW-006-C02520	
DATE	6L PQFW 2.500x2.000 mm	REV	SHEET
2020/04/20		A00	01

Dimensions and Patterns — 3.2 x 2.5 mm x mm

Package Size – Dimensions (Unit: mm)[21]



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D	3.200 BSC		
	Y	E	2.500 BSC		
LEAD WIDTH		b	0.550	0.600	0.650
LEAD LENGTH		L	0.650	0.700	0.750
		L1	0.800 REF		
LEAD PITCH		e	1.100 BSC		
PACKAGE TOLERANCE		aaa	0.100		
MOLD FLATNESS		bbb	0.100		
COPLANARITY		ccc	0.080		
DIMPLE WIDTH		T	0.150 REF		
DIMPLE LENGTH		P	0.150 REF		
DIMPLE DEPTH		A2	0.100 REF		

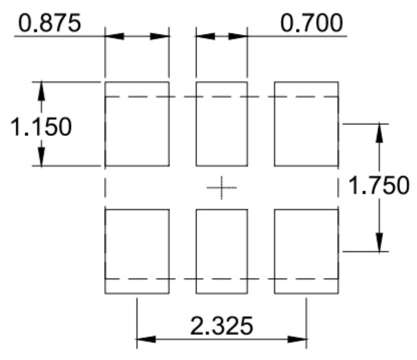
NOTE

1. ALL DIMENSION IN MM

SiTime

PKG INFO		DRAWING NO.	
6L PQFD 3.200x2.500x0.850 mm		POD-076-PQFD-006-C03225	
		REV	SHEET
DATE	10/11/2022	B01	01

Recommended Land Pattern (Unit: mm)[22]



Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	6L QFN 3.200x2.500 mm	SPL-076-QFN-006-C03225	
DATE		REV	SHEET
2020/04/20		B00	01

Additional Information

Table 20. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	https://www.sitime.com/support/resource-library/user-manuals/sit6760eb-evaluation-board-user-manual

Revision History

Table 21. Revision History

Revision	Release Date	Change Summary
0.5	22-May-2020	Advanced datasheet
0.51	1-Jun-2020	Formatting changes Updated package drawings
0.52	28-Jul-2020	Extended frequency to 644.53125 MHz
0.53	2-Aug-2020	Modified Termination Diagrams section
0.54	23-Sep-2020	Modified LVPECL, FlexSwing, LVDS current consumption specifications Modified phase jitter specification Added FlexSwing order codes Added 250u T&R order code Changed rev table date format
0.55	23-Oct-2020	Trademarks update Updated HCSL and low-power HCSL rise/fall time specs
0.56	15-Dec-2020	Updated current consumption
0.57	5-Jan-2021	Updated FlexSwing Electrical Characteristics tables and description Formatting updates
0.58	23-Mar-2021	Updated option to Contact SiTime for <100 fs rms jitter, Provide Flexswing use case example Updated hyperlinks; Changed date format; Formatting issues
0.59	29-Mar-2021	Updated Table 2. Supported Frequencies with 333.33 MHz
0.6	12-May-2022	Updated FlexSwing tables
0.9	29-Jul-2022	Added Test Diagrams section Updated Electrical Characteristics tables and descriptions
0.91	1-Aug-2022	Preliminary datasheet
0.92	12-Aug-2022	Updated Test Diagrams and formatting
0.93	15-Aug-2022	Added additional jitter integration bandwidths Updated Disclaimer
0.94	13-Oct-2022	Updated Dimensions & Patterns diagrams
0.95	24 Apr 2023	Added most commonly used Flexswing Level
0.96	20-June-2023	Added "**4-16A" Phase Jitter** specification and how to measure section.
1.0	28-Feb-2024	Updated 2520 package Dimensions drawing Rev 1.0 Production release

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