

Description

The [SiT9375](#) is a differential MEMS oscillator that is engineered for low-jitter applications requiring standard frequencies from 25 MHz to 644.53125 MHz.

A unique FlexSwing™ output-driver performs like LVPECL but provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9375 can be factory programmed for specific combinations of frequency, stability, voltage, output signaling, and pin 1 functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to [Manufacturing Notes](#) for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- Standard frequencies from 25 MHz to 644.53125 MHz
- 200 fs RMS typical phase jitter, 12 kHz to 20 MHz
- Excellent power-supply noise rejection
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ± 20 , ± 25 , ± 30 , and ± 50 ppm frequency stabilities
- Wide temperature support up to -40°C to 105°C
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous range power supply voltage
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package ([Contact SiTime](#) for 7 x 5, and 5 x 3.2 mm x mm packages)

Applications

- 100G/200G/400G network equipment
- Optical modules
- Coherent optics
- Network switches, routers
- Industrial networking equipment
- Server and storage systems
- Industrial networks
- Test and measurement
- Broadcast video

Block Diagram

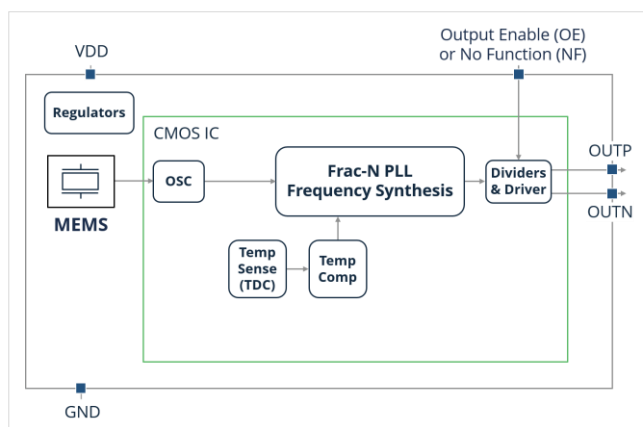


Figure 1. SiT9375 Block Diagram

Package Pinout

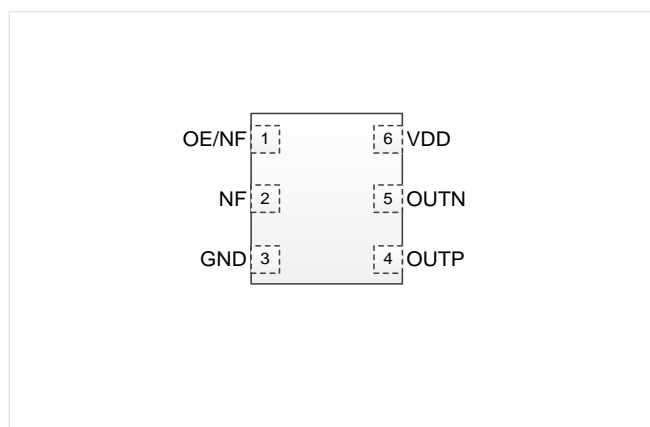


Figure 2. Pin Assignments (Top view)
(Refer to [Table 18](#) for Pin Descriptions)

Ordering Information

SiT9375AC-01B2-3310-125.000000T

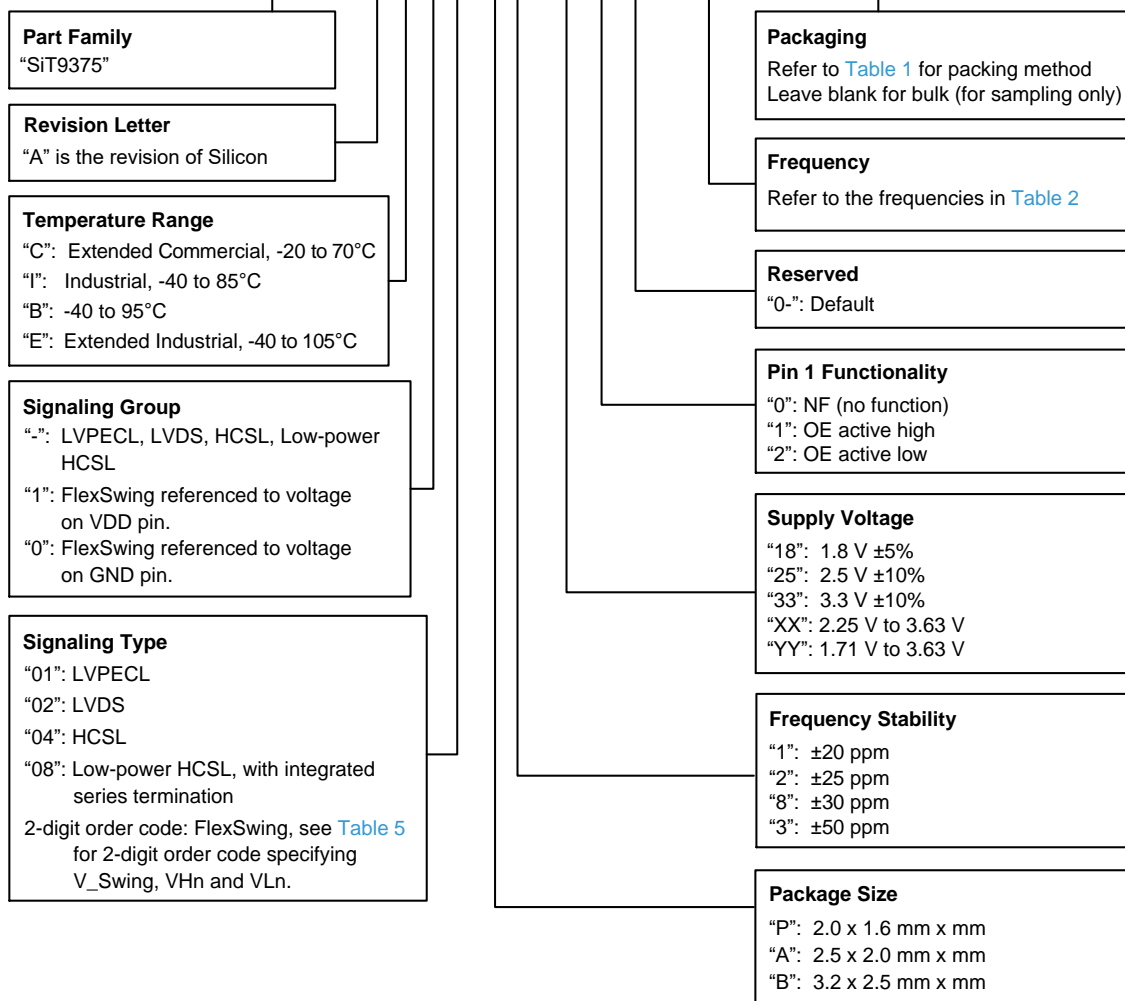


Table 1. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	8 mm T&R (250u)
2.0 x 1.6	D	E	G
2.5 x 2.0	D	E	G
3.2 x 2.5	D	E	G

Table 2. Supported Frequencies

25.000000 MHz	30.720000 MHz	50.000000 MHz	53.125000 MHz	61.440000 MHz	62.500000 MHz	74.250000 MHz	75.000000 MHz
98.304000 MHz	100.000000 MHz	106.250000 MHz	122.880000 MHz	125.000000 MHz	133.333333 MHz	148.500000 MHz	150.000000 MHz
153.600000 MHz	155.520000 MHz	156.250000 MHz	159.375000 MHz	160.000000 MHz	161.132813 MHz	166.666666 MHz	200.000000 MHz
212.500000 MHz	250.000000 MHz	300.000000 MHz	312.500000 MHz	322.265625 MHz	333.330000 MHz	625.000000 MHz	644.531250 MHz

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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information section.
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and 10 years aging at 25°C
		–	–	±25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and first year aging at 25°C
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±1	–	ppm	Ambient temperature of 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code “YY”
		2.25	–	3.63	V	Voltage-supply order code “XX”
		1.71	1.80	1.89	V	Voltage-supply order code “18”. Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code “25”
		2.97	3.30	3.63	V	Voltage-supply order code “33”
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Voltage Low	VIL	–	–	30%	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pins 1 and 2 for OE and SE, respectively
Output Characteristics						
Duty Cycle	DC	45	–	55	%	See Figure 5 and Figure 7
Startup, OE and SE Timing						
Startup Time	T_start	–	1	5	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time	T_oe	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of swing. See Figure 12
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 13
Jitter and Phase Noise						
RMS Phase Jitter (random) ^[1]	T_phj	–	170	–	fs	12 kHz to 20 MHz offset frequency integration bandwidth, 156.25 MHz
Spurious Phase Noise	PN_spur_a	–	-110	–	dBc	12 kHz to 20 MHz offset frequency range, 156.25 MHz
	PN_spur_b	–	-80	–	dBc	12 kHz to 20 MHz offset frequency range, 155.52 MHz
RMS Period Jitter ^[2]	T_jitt_per	–	1	–	ps	156.25 MHz
Peak Cycle-to-cycle Jitter ^[2]	T_jitt_cc	–	6	–	ps	156.25 MHz

Note:

1. [Contact SiTime](#) for <100 fs rms jitter.
2. Measured according to JESD65B.

Table 4. Electrical Characteristics – LVPECL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	56	–	mA	Including load termination current as shown in Figure 17 for Vdd = 3.3 V $\pm 10\%$, Vdd = 2.25 V to 3.63 V, and R3 = 220 Ohms.
		–	54.5	–	mA	Including load termination current as shown in Figure 17 for Vdd = 2.5 V $\pm 10\%$ and R3 = 220 Ohms.
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	71	–	mA	Including load termination current. See Figure 18 for termination
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	65	–	mA	Including load termination current as shown in Figure 17 for Vdd = 3.3 V $\pm 10\%$, Vdd = 2.25 V to 3.63 V, and R3 = 220 Ohms. Driver output is at logic-high voltage levels.
		–	63.5	–	mA	Including load termination current as shown in Figure 17 for Vdd = 2.5 V $\pm 10\%$ and R3 = 220 Ohms.
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	80	–	mA	Including load termination current. See Figure 18 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.025	Vdd-0.95	Vdd-0.88	V	See Figure 4
Output Low Voltage	VOL	Vdd-1.81	Vdd-1.7	Vdd-1.62	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1.2	1.5	1.9	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	± 40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 5. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to VDD, only: 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	50.5	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 17 for Vdd = 3.3 V ±10%, Vdd = 2.25 V to 3.63 V and R3 = 220 Ohms.
		–	49	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 17 for Vdd = 2.5 V ±10% and R3 = 220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	59.5	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 17 for Vdd = 3.3 V ±10%, Vdd = 2.25 V to 3.63 V and R3 = 220 Ohms.
		–	58	–	mA	Including load termination current, for FlexSwing order code “ER”. See Figure 17 for Vdd = 2.5 V ±10% and R3 = 220 Ohms.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 4 , Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values.
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 4 , Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 5
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 6. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	53	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 17 for Vdd = 1.8 V ±5% and R3 = 220 Ohms.
		–	53	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 17 for Vdd = 1.71 V to 3.63 V and R3 = 220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	62	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 17 for Vdd = 1.8 V ±5% and R3 = 220 Ohms.
		–	62	–	mA	Including load termination current, for FlexSwing order code “3E”. See Figure 17 for Vdd = 1.71 V to 3.63 V and R3 = 220 Ohms.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 4 , Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 4 , Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 5
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 7. Electrical Characteristics – FlexSwing | Supply voltage (“order code”) referred to GND, only: 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	43	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	53	–	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 17 for Vdd = 3.3 V \pm 10% and R3 = 220 Ohms.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	62	–	mA	Including load termination current, for FlexSwing order code “VP”. See Figure 17 for Vdd = 3.3 V \pm 10% and R3 = 220 Ohms.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 4 , Refer to Table 19 or Table 20 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 4 , Refer to Table 19 or Table 20 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 5
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 8. Electrical Characteristics – LVDS | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, $f = 156.25$ MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	45	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	49	–	mA	Including load termination current. See Figure 21 for termination.
Current Consumption Output Disabled with Termination	Idd_od_wt	–	58	–	mA	Including load termination current. See Figure 21 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 6
Delta VOD	ΔVOD	–	–	50	mV	See Figure 6
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 6
Delta VOS	ΔVOS	–	–	50	mV	See Figure 6
Rise/Fall Time	Tr, Tf	–	290	–	ps	Measured 20% to 80% using Figure 21 for termination. See Figure 7
Differential Asymmetry, peak-peak	V_da	–	50	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	± 40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of VOD; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 9. Electrical Characteristics – LVDS | Supply voltage (“order code”): 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, $f = 156.25$ MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	45	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	49	–	mA	Including load termination current. See Figure 21 for termination
Current Consumption Output Disabled with Termination	Idd_od_wt	–	58	–	mA	Including load termination current. See Figure 21 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 6
Delta VOD	ΔVOD	–	–	50	mV	See Figure 6
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 6
Delta VOS	ΔVOS	–	–	50	mV	See Figure 6
Rise/Fall Time	Tr, Tf	–	290	–	ps	Measured 20% to 80% using Figure 21 for termination. See Figure 7
Differential Asymmetry, peak-peak	V_da	–	50	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	± 40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of VOD; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 10. Electrical Characteristics – HCSL | Supply voltage (“order code”): 2.5 V \pm 10% (“25”), 3.3 V \pm 10% (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	41	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	56	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	64	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 4
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1	1.4	1.6	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	400	–	ps	Measured 20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 11. Electrical Characteristics – HCSL | Supply voltage (“order code”): 1.8 V \pm 5% (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	41	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	56	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	64	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 4
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1	1.4	1.6	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	400	–	ps	Measured 20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	\pm 40	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 12. Electrical Characteristics – Low Power HCSL | Supply voltage (“order code”): 2.5 V $\pm 10\%$ (“25”), 3.3 V $\pm 10\%$ (“33”), 2.25 V to 3.63 V (“XX”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, $f = 156.25$ MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	44	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	46	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 23 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	48	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 23 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 4
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1.55	1.65	1.9	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	520	–	ps	Measured 20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	550	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	± 30	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 13. Electrical Characteristics – Low Power HCSL | Supply voltage (“order code”): 1.8 V $\pm 5\%$ (“18”), 1.71 V to 3.63 V (“YY”)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, $f = 156.25$ MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	44	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	46	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 23 for termination
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	48	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 23 for termination. Driver output is at logic-high voltage levels.
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 4
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 4
Output Differential Voltage Swing	V_Swing	1.55	1.65	1.9	V	See Figure 5
Rise/Fall Time	Tr, Tf	–	520	–	ps	Measured 20% to 80%. See Figure 5
Differential Asymmetry, peak-peak	V_da	–	550	–	mV	See Figure 8
Differential Skew, peak	V_ds	–	± 30	–	ps	See Figure 9
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 10
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity ^[3]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Note:

3. Terminology chosen for clarity; referred to historically as power-supply noise rejection (PSNR).

Table 14. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		–	260	°C

Table 15. Thermal Considerations^[4]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	TBD	TBD

Notes:

4. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 16. Maximum Operating Junction Temperature^[5]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	TBD
85°C	TBD
95°C	TBD
105°C	TBD

Notes:

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 17. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	g
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Pin Description

Table 18. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H ^[6] Specified frequency output L: OUTP (OUTN) held at logic high (low)
		No Function (NF)	H or L or Open: No effect on output frequency or other device functions.
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions
3	GND	Power	VDD Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[7]

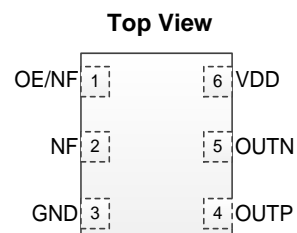


Figure 3. Pin Assignments

Notes:

6. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, OE pin that is active high or active low are recommended to include an external pull-up or pull-down resistor, respectively, of 10 kΩ when the pin is not externally driven.
7. A capacitor of value 0.1 μF or higher between VDD and GND pins is required.

FlexSwing Configurations

A FlexSwing output-driver performs like LVPECL but provides independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements

and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDD or GND pins.

Table 19. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on VDD pin

Order Code V_Swing (V)		VLn																																							
		A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X																		
		Vdd-2.31V	Vdd-2.26V	Vdd-2.21V	Vdd-2.16V	Vdd-2.11V	Vdd-2.06V	Vdd-2.01V	Vdd-1.96V	Vdd-1.91V	Vdd-1.86V	Vdd-1.82V	Vdd-1.77V	Vdd-1.72V	Vdd-1.67V	Vdd-1.62V	Vdd-1.57V	Vdd-1.52V	Vdd-1.47V	Vdd-1.42V	Vdd-1.37V	Vdd-1.32V	Vdd-1.28V																		
VHn	A								AJ	AK	AL	AM	AN	AP	AQ	AR	AS	AT	AU	AV	AW	AX																			
	B								1.94	1.86	1.77	1.69	1.61	BN	BP	BQ	BR	BS	BT	BU	BV	BW	BX																		
	C								1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76																		
	D								1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68																	
	E								1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59																
	F									1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51														
	G										1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51													
	H											1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51												
	J												1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51											
	K													1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51										
	L														1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51									
	M															1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51								
	N																1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51							
	P																	1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51						
	Q																		1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51					
	R																			1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51				
	S																				1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51			
	T																					1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51		
	U																						1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51	
	V																							1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59	0.51
	W																								1.94	1.86	1.77	1.69	1.61	1.52	1.44	1.35	1.27	1.18	1.10	1.01	0.93	0.85	0.76	0.68	0.59

Supply Voltage	Available Colors
1.8V±5%	Not Supported
1.71V to 3.63V	Not Supported
2.5V±10%	Blue
3.3V±10%	Blue Red
2.25V to 3.63V	Blue
Note A	Gray

Supply Voltage	Available Colors
1.8V±5%	Not Supported
1.71V to 3.63V	Not Supported
2.5V±10%	Blue
3.3V±10%	Blue Red
2.25V to 3.63V	Blue
Note A	Gray

The above table identifies supported combinations of nominal VOH (i.e. VHn) and nominal VOL (i.e. VLn) in colored boxes. The two-character code in each box corresponds to the VHn and VLn codes specified in the 2nd column and 2nd row in the table, respectively. The number in each box indicates the nominal differential swing or 2(VHn – VLn).

Example 1 – Suppose a design requires a differential swing (V_Swing) of 1 Vpp with a common-mode voltage of Vdd-1.3 V. If VDD is 2.5 V, and using Table 19, then VOL = Vdd – 1.3 V – (1 Vpp)/4 = 0.95 V. Solving for X in VLn = 2.5 V – X = 0.95 V, we obtain X = 1.55 V, whose closest match is 1.53 V, or column “S” in Table 19. The differential swing in Row D (i.e. 1.01 Vpp) is the closest match to V_Swing = 1 Vpp. Thus, the FlexSwing order code is “DS”. The value for VHn may be computed as VLn + V_Swing/2 = 0.95 V + (1.01 Vpp)/2 = 1.455 V. The common mode voltage is VLn + V_Swing/4 = 0.97 V + 1.01V/4 = 1.2225 V.

Table 20. FlexSwing 2-digit Order Codes specifying V_{Hn} and V_{Ln} referenced to voltage on GND pin

Order Code V _{Swing} (V)		C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y
		0.45V	0.49V	0.54V	0.59V	0.64V	0.69V	0.74V	0.79V	0.84V	0.89V	0.94V	0.99V	1.03V	1.08V	1.16V	1.23V	1.3V	1.38V	1.45V	1.53V	1.6V
V _{Hn}	A																		AV	AW	AX	AY
	B		Supply Voltage		Available Colors														BV	BW	BX	BY
	C		1.8V±5%		Orange		Green												CV	CW	CX	CY
	D		1.71V to 3.63V		Orange		Green		Blue		Purple								DU	DV	DX	DY
	E		2.5V±10%		Orange		Green		Blue		Red								EU	EV	EX	EY
	F		3.3V±10%		Green		Blue		Red										FS	FT	FX	FY
	G		2.25V to 3.63V		Green		Blue		Gray										GS	GT	GX	GY
	H		Note A		Gray														HS	HT	HW	HY
	J																		JS	JT	JX	JY
	K																		KS	KT	KX	KY
	L																		LS	LT	LX	LY
	M																		MS	MT	MX	MY
	N																		NQ	NR	NX	NY
	P																		PS	PT	PX	PY
	Q																		QS	QT	QX	QY
	R																		RS	RT	RX	RY
	S																		SU	SV	SY	SY
	T																		TU	TV	TX	TY
	U																		UU	UV	UX	UY
	V																		VU	VV	VX	VY
	W																		WU	WV	WX	WY
	X																		XU	XV	XY	XY
	Y																		YU	YV	YX	YY
	Z																		ZU	ZV	ZX	ZY
	1																		1U	1V	1X	1Y
	2																		2U	2V	2X	2Y
	3																		3U	3V	3X	3Y

Example 2 – Suppose a design requires a differential swing of 1 V_{pp} with a 1.2 V common mode voltage (similar to Example 1 but referenced to ground). Using Table 20, V_{Ln} = 1.2 V – (1 V_{pp})/4 = 0.95 V, whose closest match is column N. Scanning column N, row W has the closest V_{Swing} to

1 V_{pp}, so the FlexSwing order code is “WN”. Here, the resulting V_{Swing} is 1.01 V_{pp}, and the common mode voltage is V_{Ln} + V_{Swing}/4 = 0.94 + (1.01 V_{pp})/4 = 1.1925 V.

Waveform Diagrams

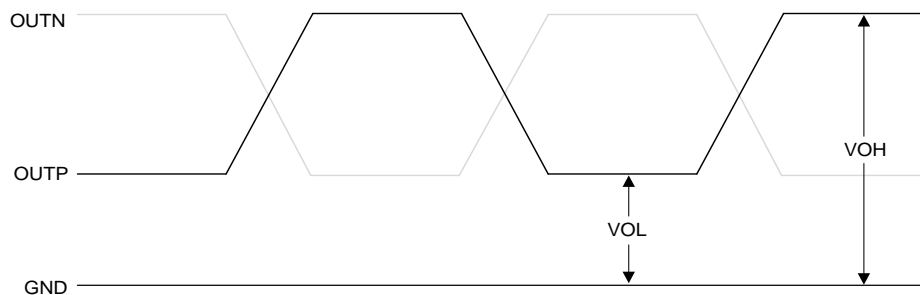


Figure 4. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

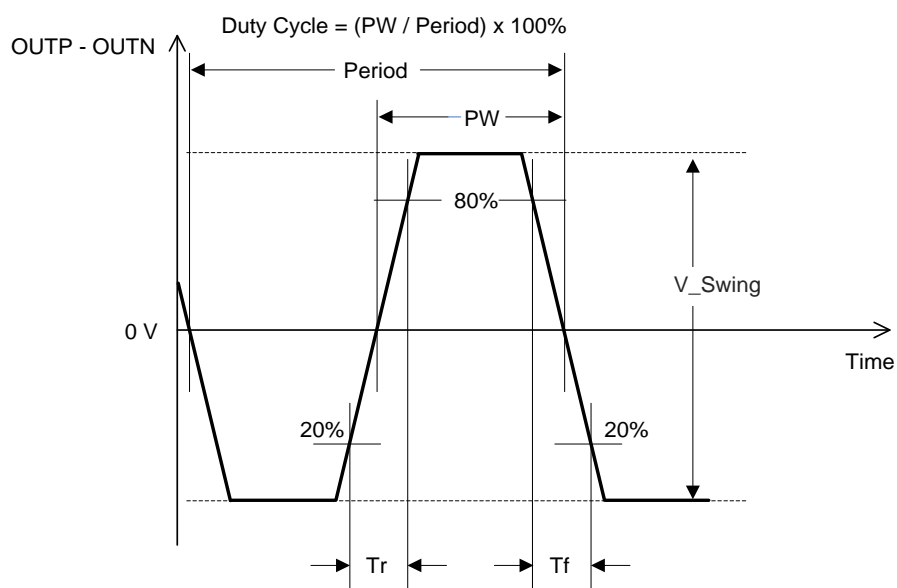


Figure 5. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

Waveform Diagrams (continued)

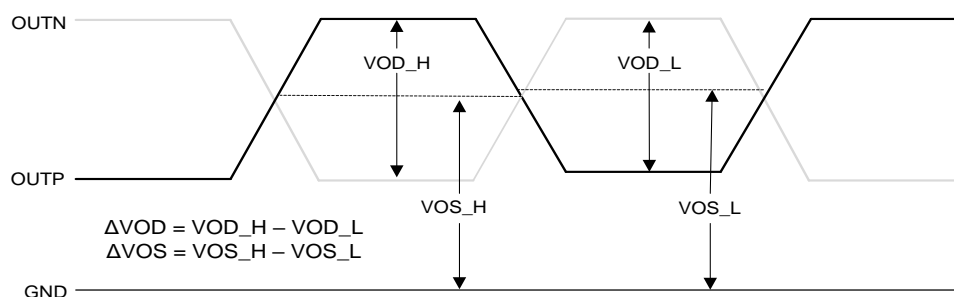


Figure 6. LVDS Voltage Levels per Differential Pin

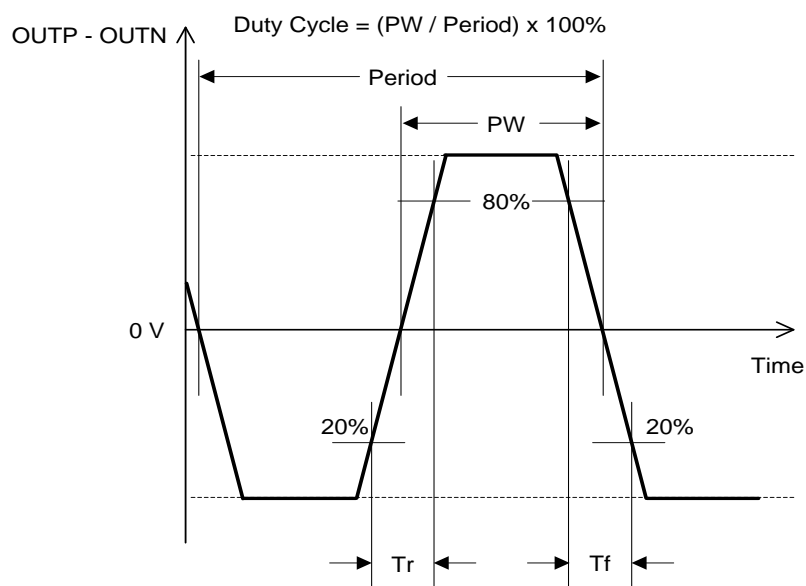


Figure 7. LVDS Differential Waveform

Waveform Diagrams (continued)

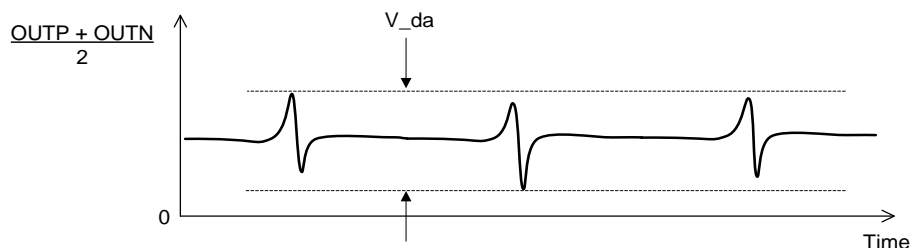


Figure 8. Differential Asymmetry (V_{da})

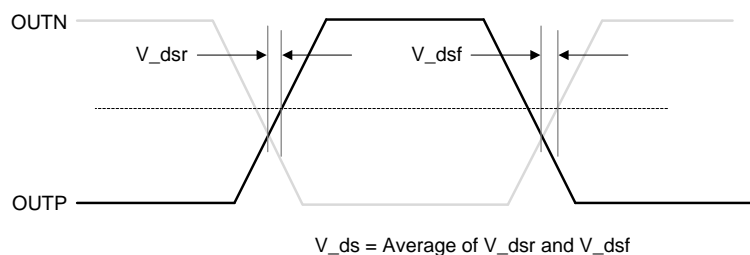


Figure 9. Differential Skew (V_{ds}) is measured as the Time between the Average Voltage Level and Crossing Voltage

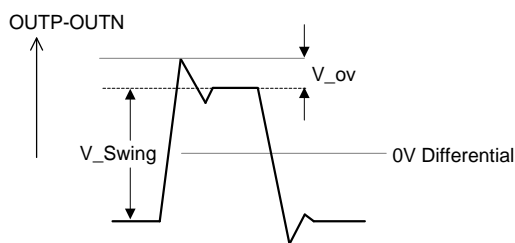


Figure 10. Overshoot Voltage (V_{ov}) for LVPECL, FlexSwing, HCSL, Low-power HCSL

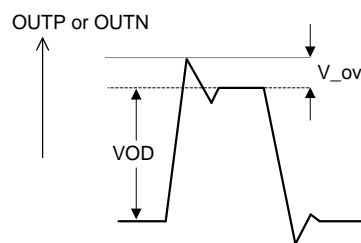


Figure 11. Overshoot Voltage (V_{ov}) for LVDS Output

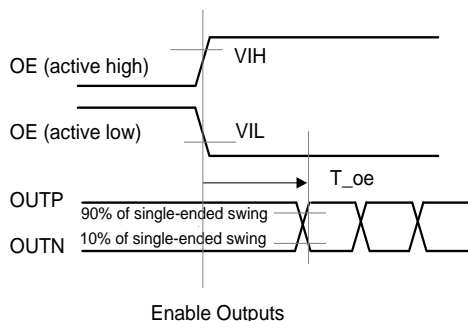


Figure 12. OE Pin Enable Timing (T_{oe})

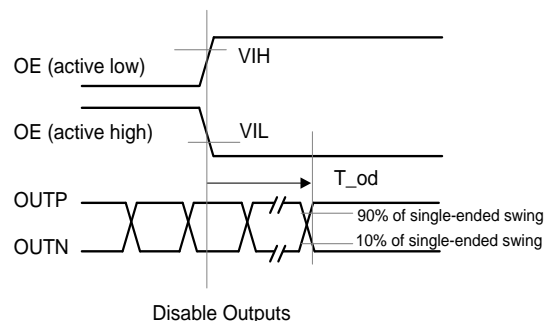


Figure 13. OE Pin Disable Timing (T_{od})

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9375 FlexSwing output drivers support low power without sacrificing signal integrity via simple terminations as shown in Figure 15 and Figure 17, compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are

voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_{load}) into the load termination.

Table 21. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage Order Codes	Termination Options					
		Figure 14	Figure 15	Figure 16	Figure 17	Figure 18	Figure 19
LVPECL referenced to Vdd	"25", "33", "XX"	OK to use $I_{load} = 40\text{ mA}$ with $100\text{ }\Omega$ near-end bias resistor	Do Not Use	OK to use $I_{load} = 28\text{ mA}$	OK to use	OK to use $I_{load} = 28\text{ mA}$	Do Not Use
FlexSwing referenced to Vdd			OK to use (See Figure 15 for frequency ranges and voltage swings)	OK to use ⁸	OK to use	OK to use	Do Not Use
FlexSwing referenced to Gnd	"25", "33", "XX", "YY"	OK to use ⁸		Do Not Use	OK to use	Do Not Use	Do Not Use
	"18"			Do Not Use	OK to use	Do Not Use	OK to use

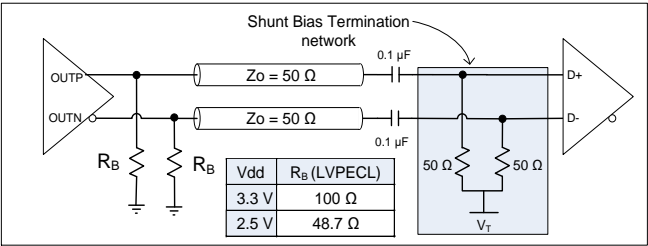


Figure 14. Recommended LVPECL and FlexSwing⁹ Termination when AC-coupled

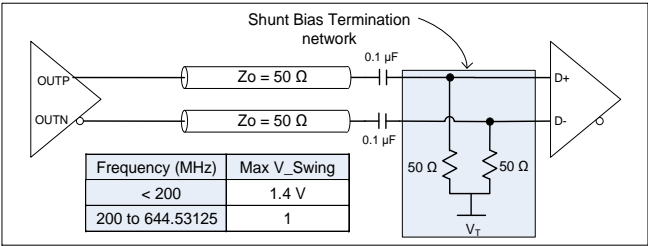


Figure 15. Recommended FlexSwing Termination when AC-coupled

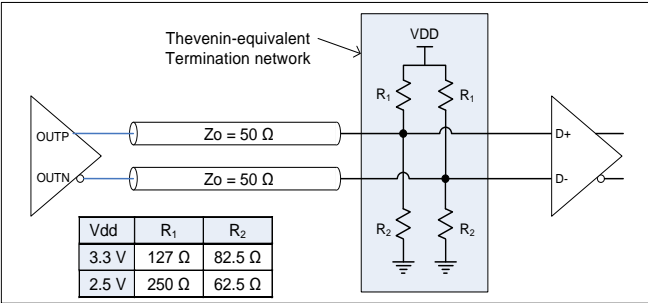


Figure 16. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network

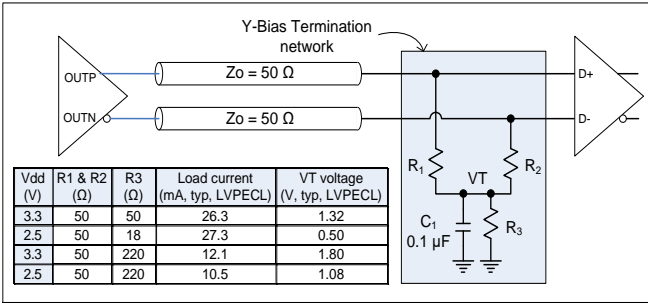


Figure 17. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

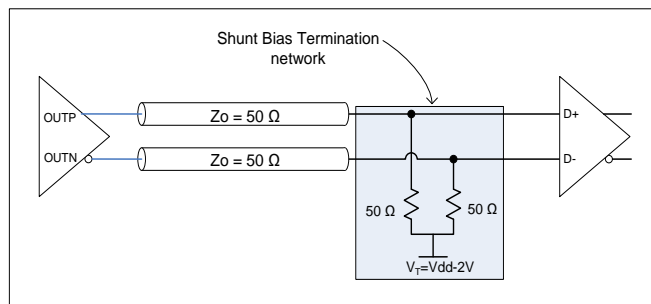


Figure 18. LVPECL and FlexSwing with Y-Bias Termination

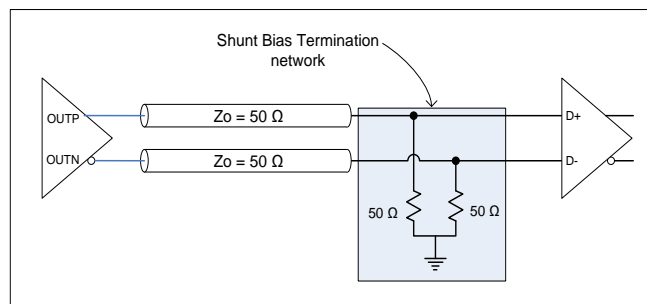


Figure 19. FlexSwing Termination – Only for use with Supply Voltage Order Code “18”

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

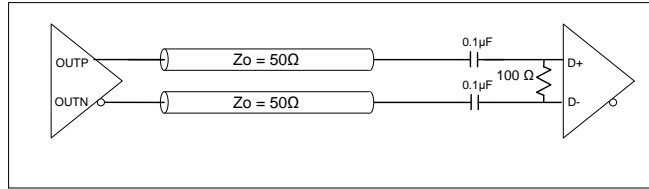


Figure 20. LVDS AC Termination

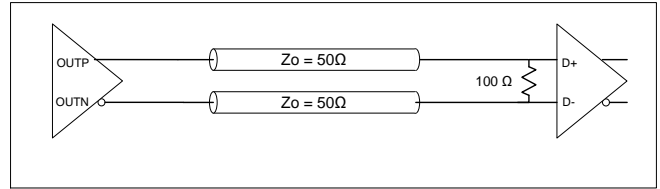


Figure 21. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

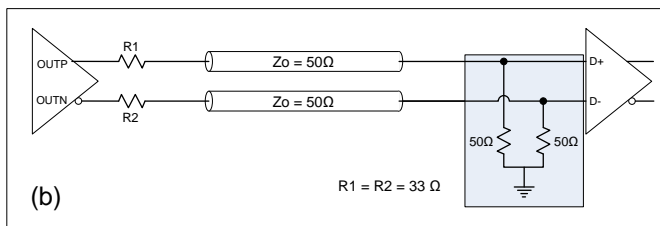
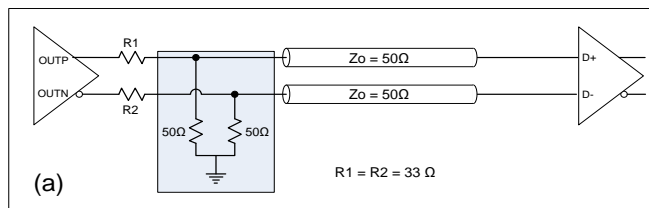


Figure 22. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V \pm 5%, 2.5 V \pm 10%, 3.3 V \pm 10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

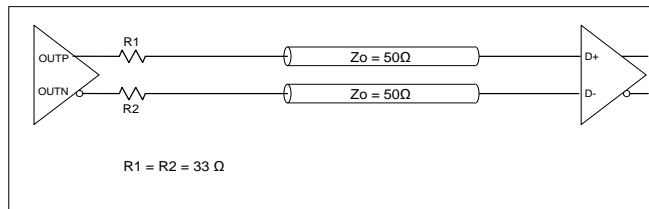
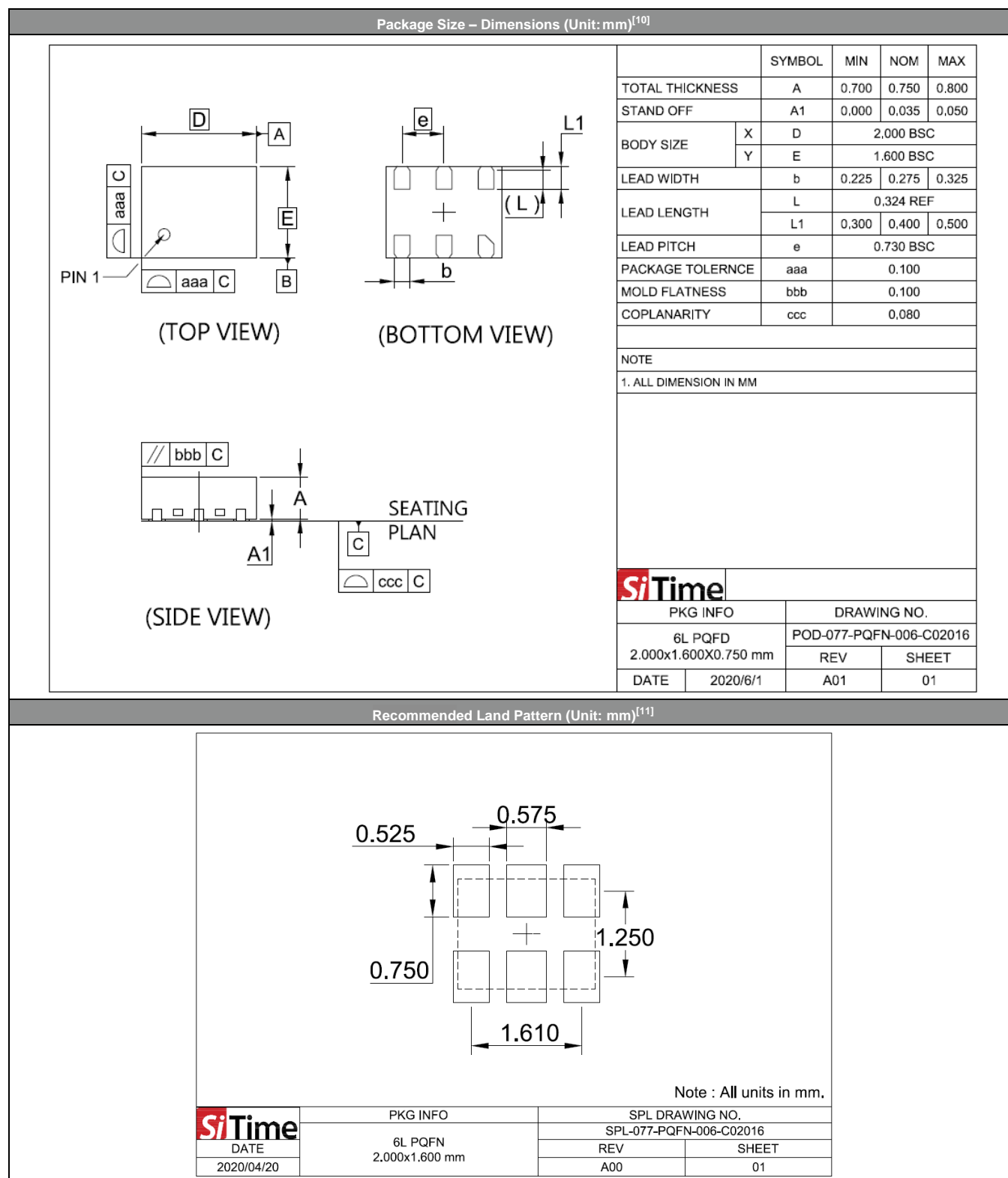


Figure 23. Low-power HCSL Termination

Notes:

8. [Contact SiTime](#) for optimum R1 and R2 values for FlexSwing options.
9. [Contact SiTime](#) for optimum Rs values for FlexSwing options.

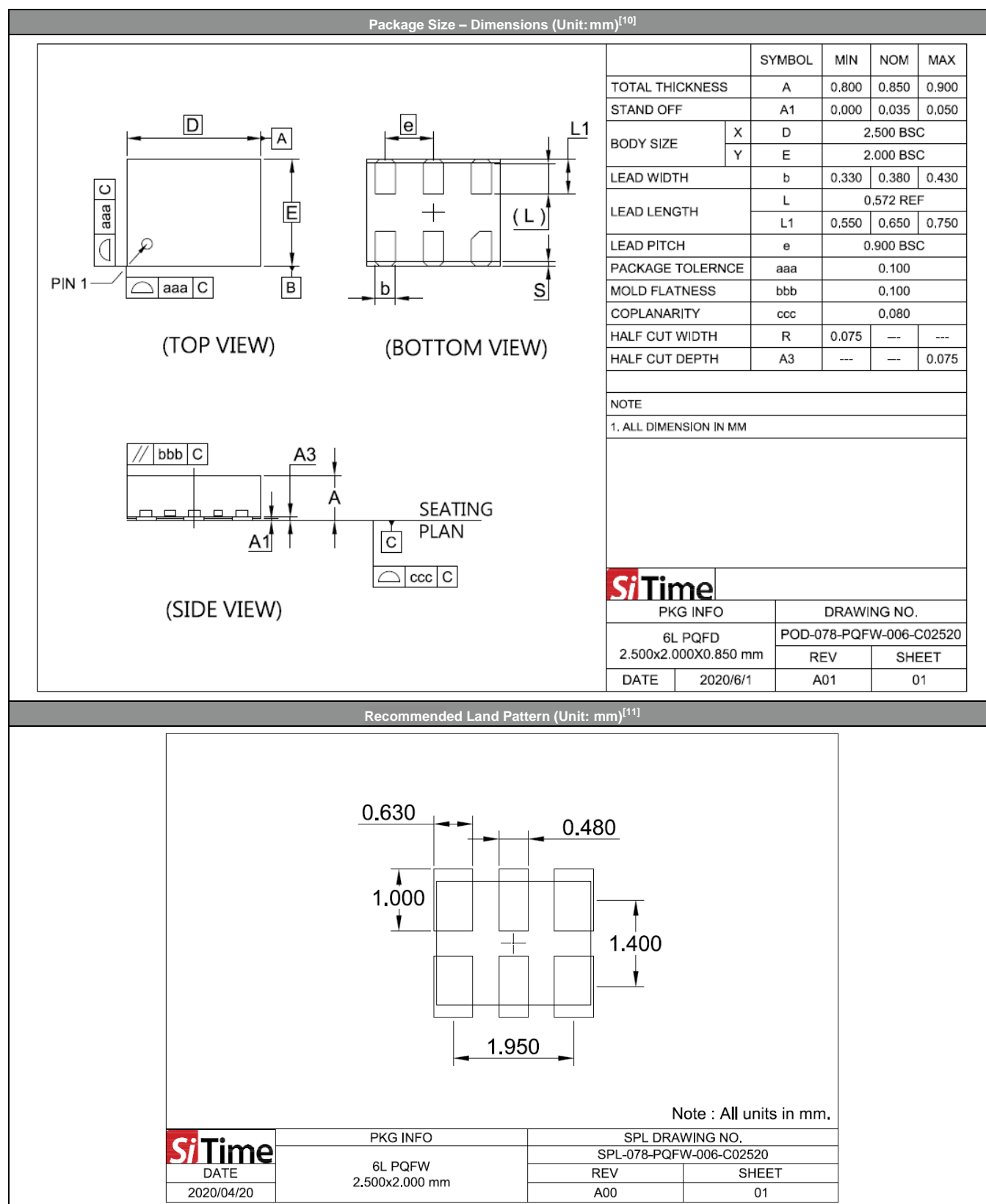
Dimensions and Patterns — 2.0 x 1.6 mm x mm



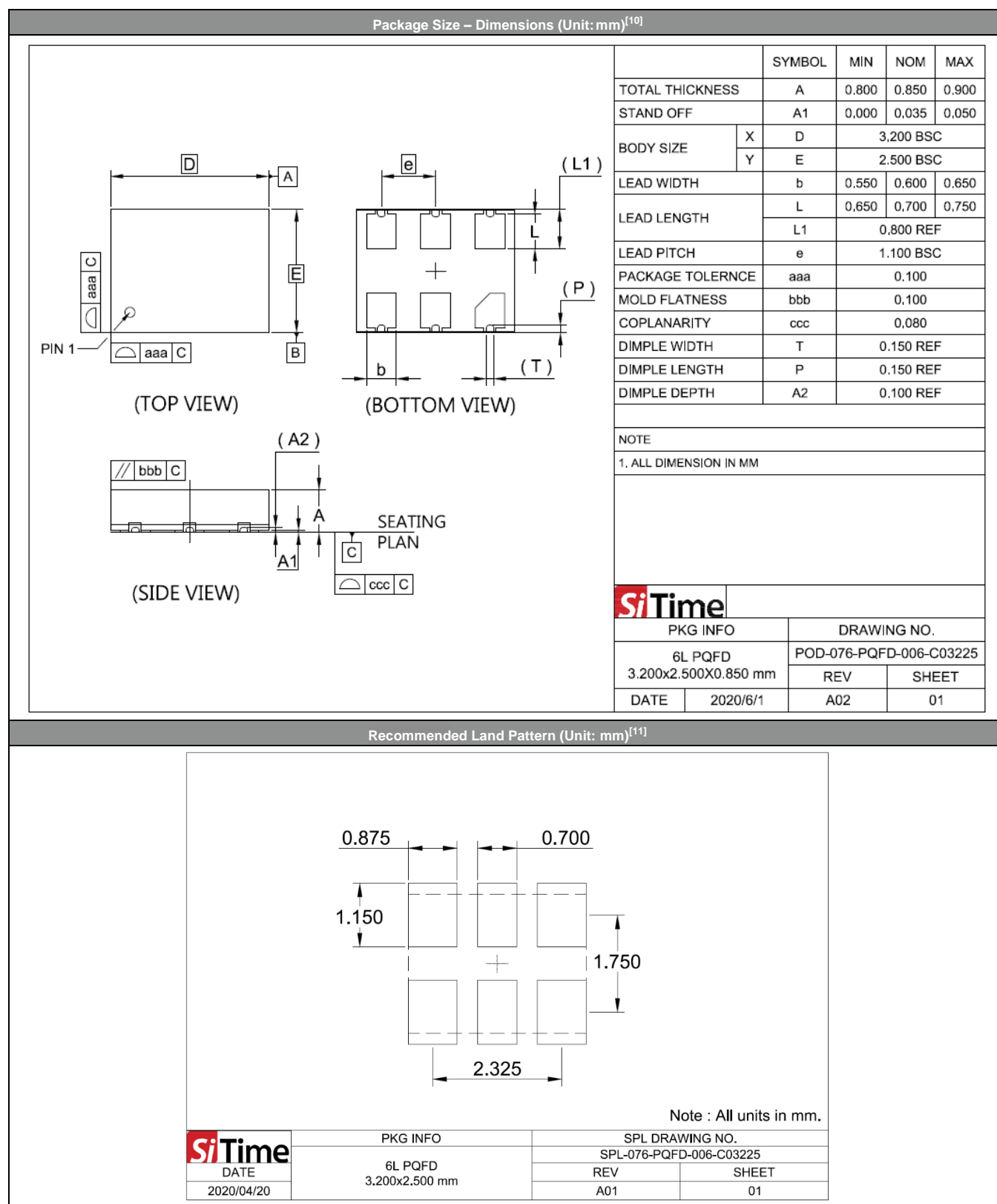
Notes:

- Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- A capacitor of value 0.1 μ F or higher between VDD and GND is required.

Dimensions and Patterns — 2.5 x 2.0 mm x mm



Dimensions and Patterns — 3.2 x 2.5 mm x mm



Additional Information

Table 22. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	TBD

Revision History

Table 23. Revision History

Revision	Release Date	Change Summary
0.5	22-May-2020	Advanced datasheet
0.51	1-Jun-2020	Formatting changes Updated package drawings
0.52	28-Jul-2020	Extended frequency to 644.53125 MHz
0.53	2-Aug-2020	Modified Termination Diagrams section
0.54	23-Sep-2020	Modified LVPECL, FlexSwing, LVDS current consumption specifications Modified phase jitter specification Added FlexSwing order codes Added 250u T&R order code Changed rev table date format
0.55	23-Oct-2020	Trademarks update Updated HCSL and low-power HCSL rise/fall time specs
0.56	15-Dec-2020	Updated current consumption
0.57	5-Jan-2021	Updated FlexSwing Electrical Characteristics tables and description Formatting updates
0.58	23-Mar-2021	Updated option to Contact SiTime for <100 fs rms jitter, Provide Flexswing use case example Updated hyperlinks; Changed date format; Formatting issues
0.59	29-Mar-2021	Updated Table 2. Supported Frequencies with 333.33 MHz
0.6	12-May-2022	Updated FlexSwing tables

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