SILICON LABORATORIES

Si552

PRELIMINARY DATA SHEET

DUAL FREQUENCY VCXO (10 MHZ TO 1.4 GHZ)

Features

- Available with any-rate output frequencies from 10–945 MHz and select frequencies to 1.4 GHz
- Two selectable output frequencies
- 3rd generation DSPLL® with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS & CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

Ordering Information:

See page 8.

Applications

- SONET/SDH
- xDSL
- 10 GbE LAN / WAN
- Low-jitter clock generation
- Optical Modules
- Clock and data recovery

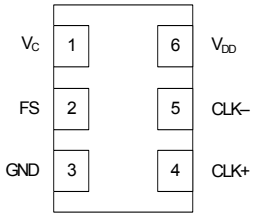
Description

The Si552 dual frequency VCXO utilizes Silicon Laboratories advanced DSPLL® circuitry to provide a very low jitter clock for all output frequencies. The Si552 is available with any-rate output frequency from 10 to 945 MHz and select frequencies to 1400 MHz. Unlike traditional VCXO's where a different crystal is required for each output frequency, the Si552 uses one fixed crystal frequency to provide a wide range of output frequencies. This IC based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si552 IC based VCXO is factory configurable for a wide variety of user specifications including frequency, supply voltage, output format, tuning slope, and temperature stability. Specific configurations are factory programmed at time of shipment, thereby eliminating long lead times associated with custom oscillators.

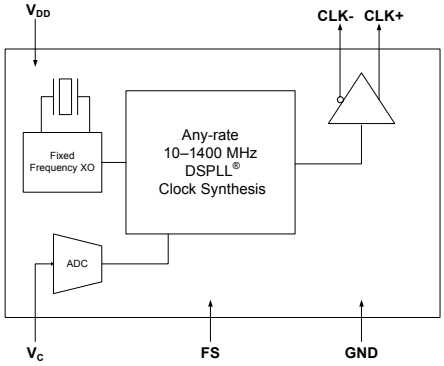
Pin Assignments:

See page 7.

(Top View)



Functional Block Diagram



1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I_{DD}	Output enabled	—	90	—	mA
		TriState mode	—	60	—	
Output Enable (OE)[2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	
Operating Temperature Range	T_A		–40	—	85	ºC

Notes:
1. Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 8 for further details.
2. OE pin includes a 17 kΩ pullup resistor to VDD. Pulling OE to ground causes outputs to tristate.

Table 2. V_C Control Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope[1,2,3]	K_V	10 to 90% of V_{DD}	—	45 90 135 180	—	ppm/V
Control Voltage Linearity[4]	L_{VC}	BSL	–5	±1	+5	%
		Incremental	–10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	kΩ
Nominal Control Voltage	V_{CNOM}	@ f_O	—	3/8 x V_{DD}	—	V
Control Voltage Tuning Range	V_C		0		V_{DD}	V

Notes:
1. Positive slope; selectable option by part number. See Section 3. "Ordering Information" on page 8.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. K_V variation is ±28% of typical values.
4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency[1,2,3]	f_O	LVDS/CML/LVPECL	10	—	945	MHz
		CMOS	10	—	160	
Temperature Stability[1,4]	$\Delta f/f_O$	T_A = –40 to +85 ºC	–20 –50 –100	— — —	+20 +50 +100	ppm
Absolute Pull Range[1,4]	APR		±25	—	±150	ppm
Aging		Frequency drift over 15 year life.	—	—	±10	ppm
Power up Time[5]	t_{OSC}		—	—	10	ms
Settling Time After FS Change	t_{FRQ}		—	—	10	ms

Notes:
1. See Section 3. "Ordering Information" on page 8 for further details.
2. Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
3. Nominal output frequency set by V_{CNOM} = 3/8 x V_{DD}.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f_O (to within ±1 ppm of f_O).

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.5	—	0.93	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.32	0.40	0.50	V_{PP}
CML Output Option[2]	V_O	mid-level	—	V_{DD} – 0.75	—	V
	V_{OD}	swing (diff)	0.70	0.95	1.20	V_{PP}
CMOS Output Option[3]	V_{OH}	I_{OH} = 32 mA	0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}	I_{OL} = 32 mA	—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with CL = 15 pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V_{DD}/2	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF

Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2,3] for $F_{OUT} \geq$ 500 MHz	ϕ_J	Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.35 0.38	 — —	ps
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.43 0.41	 — —	
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.52 0.46	 — —	
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.64 0.52	 — —	
Phase Jitter (RMS)[1,2,3] for F_{OUT} of 125 to 500 MHz	ϕ_J	Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.42 0.58	 — —	ps
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.48 0.60	 — —	
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.57 0.64	 — —	
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	 — —	 0.67 0.68	 — —	

Notes:
1. Differential Modes: LVPECL/LVDS/CML. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCSO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter* for $F_{OUT} \leq$ 160 MHz	J_{PER}	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles.

Table 7. CLK± Output Phase Noise (Typical)

Configuration	f_C K_V Output	74.25 MHz 45 ppm/V CMOS	300 MHz 90 ppm/V LVPECL	622.08 MHz 45 ppm/V LVPECL	Units
Offest Frequency (f)	$\mathcal{L}$ (f)				
100 Hz		–94	–74	–77	dBc/Hz
1 kHz		–117	–98	–101	
10 kHz		–128	–112	–114	
100 kHz		–135	–122	–118	
1 MHz		–138	–134	–128	
10 MHz		–143	–144	–144	
100 MHz		n/a	–147	–147	

Table 8. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	–0.5 to +3.8	Volts
Input Voltage (any input pin)	V_I	–0.5 to V_{DD} + 0.3	Volts
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	>2500	Volts
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	ºC
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	10	seconds

Notes:
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions.
2. Refer to Si5xx Packaging FAQ available for download from www.silabs.com/VCXO for further information, including soldering profiles.

Table 9. Environmental Compliance

The Si552 meets the following qualification test requirements.

Parameter	Conditions/ Test Method
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016

2. Pin Descriptions

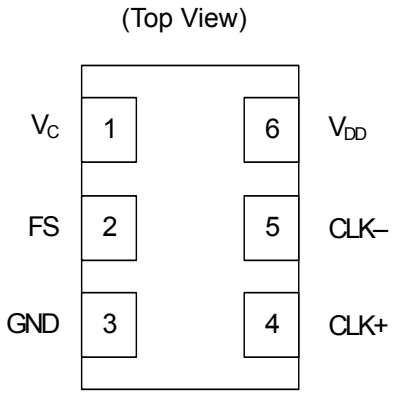
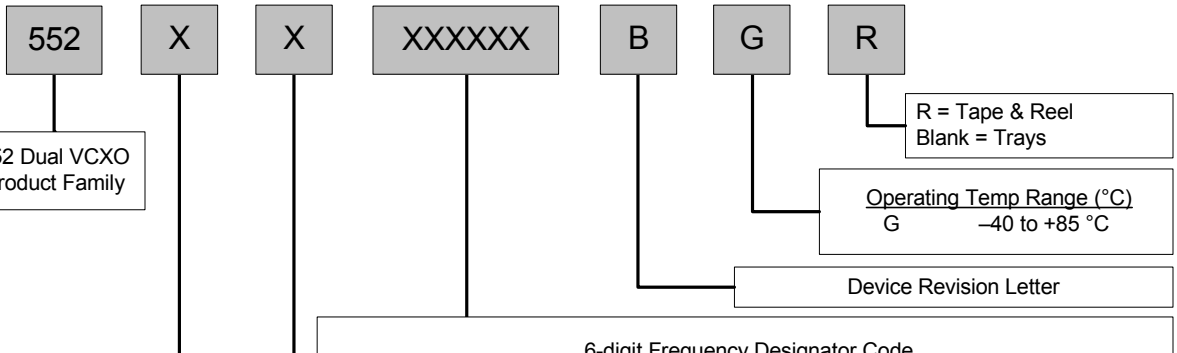


Table 10. Si552 Pin Descriptions

Pin	Name	Type	Function
1	V_C	Analog Input	Control Voltage
2	FS*	Input	Frequency Select: 0 = first frequency selected 1 = second frequency selected
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK– (N/A for CMOS)	Output	Complementary Output (N/C for CMOS)
6	V_{DD}	Power	Power Supply Voltage
***Note:** FS includes a 17 kΩ pullup resistor to V_{DD}. Consult 3.“Ordering Information” for details on frequency value ordering.			

3. Ordering Information

The Si552 was designed to support a variety of options including frequency, temperature stability, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si552 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to www.silabs.com/VCXOPartNumber to access this tool and for further ordering instructions. The Si552 VCXO series is supplied in an industry-standard, RoHS compliant, lead-free, 6-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.



6-digit Frequency Designator Code

Two unique frequencies can be specified within the following bands of frequencies: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz. A six digit code will be assigned for the specified combination of frequencies. Codes > 000100 refer to dual XOs programmed with the lower frequency value selected when FS = 0, and the higher value when FS = 1. Six digit codes < 000100 refer to dual XOs programmed with the higher frequency value selected when FS = 0, and the lower value when FS = 1.

1st Option Code

Code	VDD	Output Format
A	3.3	LVPECL
B	3.3	LVDS
C	3.3	CMOS
D	3.3	CML
E	2.5	LVPECL
F	2.5	LVDS
G	2.5	CMOS
H	2.5	CML
J	1.8	CMOS
K	1.8	CML

Notes:
CMOS available to 160 MHz.

2nd Option Code

Code	Temperature Stability ± ppm (max)	Tuning Slope Kv ppm/V (typ)	Minimum APR (±ppm) @ 3.3 V	@ 2.5 V	@ 1.8 V
A	100	180	100	75	25
B	100	90	30	Note 6	Note 6
C	50	180	150	125	75
D	50	90	80	30	25
E	20	45	25	Note 6	Note 6
F	50	135	100	75	50

Notes:
1. For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher higher Kv values to account for their higher temperature dependence, the Si55x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs. See AN255 and AN266 for more information.
2. APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±25 ppm is able to lock to a clock with a ±25 ppm stability, over 15 years.
3. Nominal Pull range (±) = 0.5 x V_{DD} x tuning slope.
4. Nominal Absolute Pull Range (±APR) = Pull range – stability – lifetime aging
   =0.5 x V_{DD} x tuning slope – stability – 10 ppm
5. Minimum APR values noted above include worst case values for all parameters.
6. Combination not available.

Example Part Number: 552AF000108BGR is a 5x7mm Dual VCXO in a 6 pad package. Since the six digit code (000108) is > 000100, f0 is 644.53125 MHz (lower frequency) and f1 is 693.48299 (higher frequency), with a 3.3V supply and LVPECL output. Temperature stability is specified as ± 50 ppm and the tuning slope is 135 ppm/V. The part is specified for a -40 to +85 C° ambient temperature range operation and is shipped in tape and reel format.

4. Outline Diagram and Suggested Pad Layout

Figure 1 illustrates the package details for the Si552. Table 11 lists the values for the dimensions shown in the illustration.

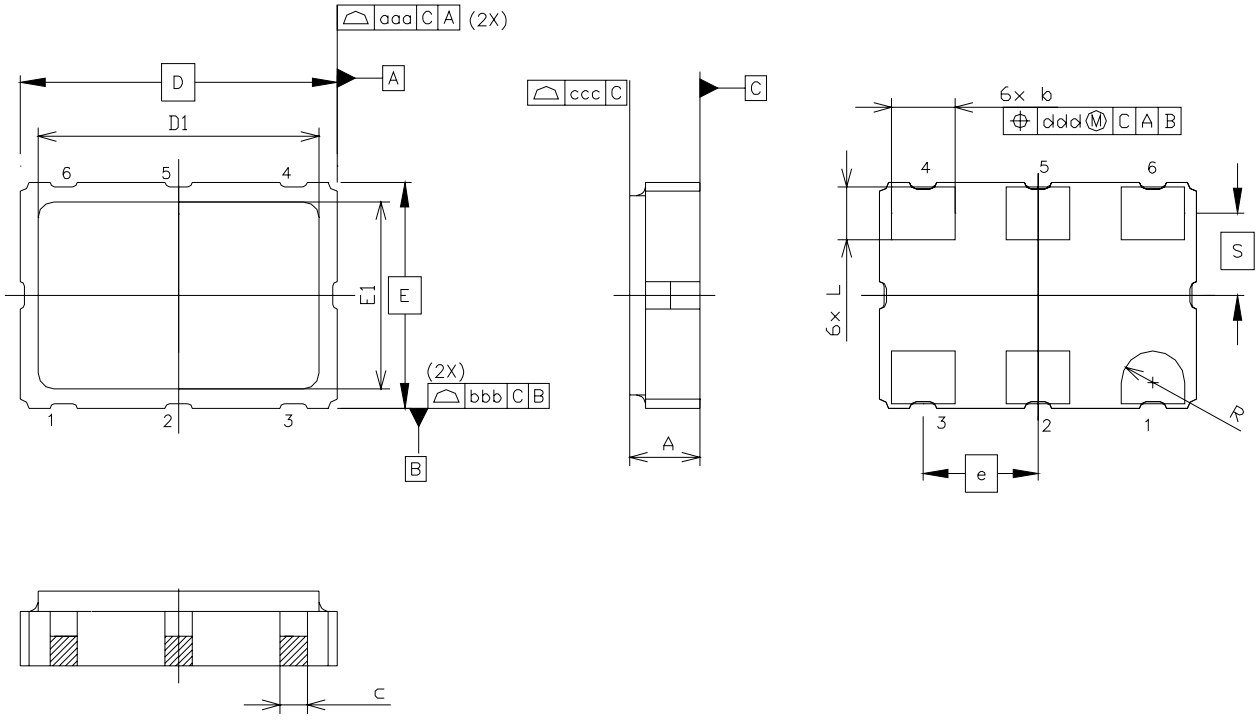


Figure 1. Si552 Outline Diagram

Table 11. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.45	1.65	1.85
b	1.2	1.4	1.6
c		0.60 TYP	
D		7.00 BSC	
D1	6.10	6.2	6.30
e		2.54 BSC	
E		5.00 BSC	
E1	4.30	4.40	4.50
L	1.07	1.27	1.47
S		1.815 BSC	
R		0.7 REF	
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10

5. 6-Pin PCB Land Pattern

Figure 2 illustrates the 6-pin PCB land pattern for the Si552. Table 12 lists the values for the dimensions shown in the illustration.

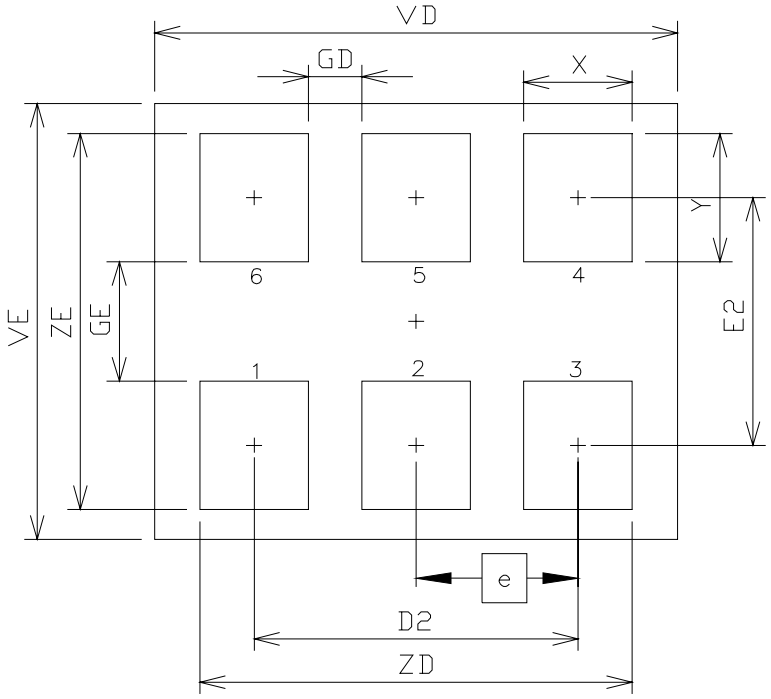


Figure 2. Si552 PCB Land Pattern

Table 12. PCB Land Pattern Dimensions (mm)

Dimension	Min	Max
D2	5.08 REF	
e	2.54 BSC	
E2	4.15 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X	1.70 TYP	
Y	2.15 REF	
ZD	—	6.78
ZE	—	6.30

Notes:
1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design based on IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

DOCUMENT CHANGE LIST

Revision 0.2 to Revision 0.3

- Updated 1. "Electrical Specifications" on page 2.
  - Updated ordering and format of Table 1 through Table 9.
  - Updated LVDS and CML in Table 4, “CLK± Output Levels and Symmetry,” on page 3.
  - Updated RMS jitter values in Table 5, “CLK± Output Phase Jitter,” on page 4.
  - Added Typical Phase Noise performance data in Table 5, “CLK± Output Phase Jitter,” on page 4.
  - Added Table 7, “CLK± Output Phase Noise (Typical),” on page 5.
- Updated 3. "Ordering Information" on page 8.
  - Removed ordering option E at V_{DD} = 2.5 V in table for the 2nd Option Code.
  - Typical APRs replaced with minimum APR values.
  - New 135 ppm/V K_V option included.
- Added specification for Settling Time After FS Change in Table 3, “CLK± Output Frequency Characteristics,” on page 3.

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