Signetics

74164, LS164
Shift Registers

8-Bit Serial-In Parallel-Out Shift Register
Product Specification

Logic Products

FEATURES
- **Gated serial Data inputs**
- **Typical shift frequency of 36MHz**
- **Asynchronous Master Reset**
- **Fully buffered Clock and Data inputs**

DESCRIPTION
The '164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one set-up time before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74164	36MHz	37mA
74LS164	36MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%; T_A = 0°C to +70°C
Plastic DIP	N74164N, N74LS164N
Plastic SO	N74LS164D

NOTE:
For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74LS
All	Inputs	1ul	1LSul
All	Outputs	5ul	10LSul

NOTE:
Where a 74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

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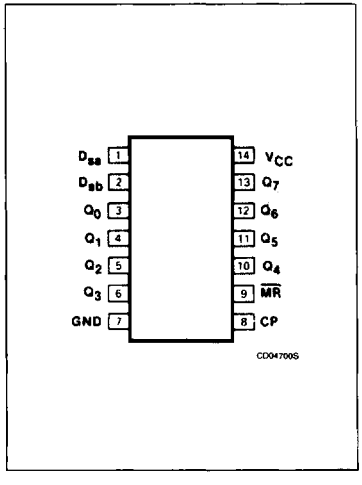
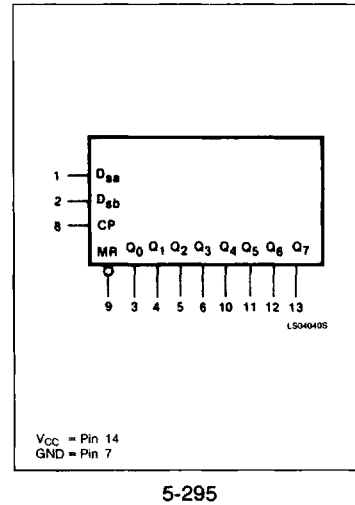
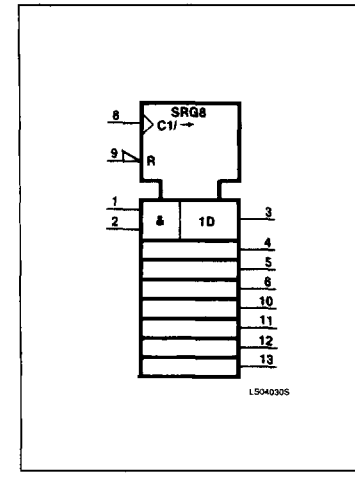
PIN CONFIGURATION



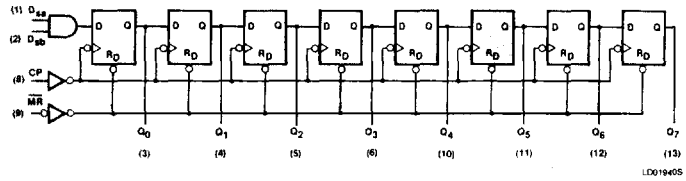
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1 — Q_7
Reset (clear)	L	X	X	X	L	L — L
Shift	H	↑	l	l	L	q_0 — q_6
	H	↑	l	h	L	q_0 — q_6
	H	↑	h	l	L	q_0 — q_6
	H	↑	h	h	H	q_0 — q_6

H = HIGH voltage level.
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one set-up time prior to the LOW-to-HIGH Clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8	V
I_{IK}	Input clamp current			−12			−18	mA
I_{OH}	HIGH-level output current			−400			−400	μA
I_{OL}	LOW-level output current			8			8	mA
T_A	Operating free-air temperature	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74164			74LS164			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX I_{OH} = MAX		2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA (74LS)					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V			40				μA
			V_I = 2.7V						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		9		−27.5	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			37	54		16	27	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

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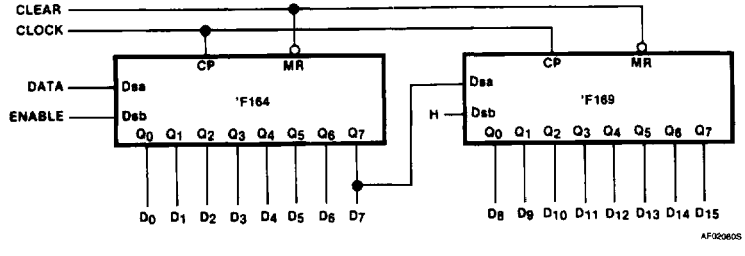
APPLICATION DIAGRAM



The '164 can be cascaded to form synchronous shift registers of longer length. Here, two devices are combined to form a 16-bit shift register.

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

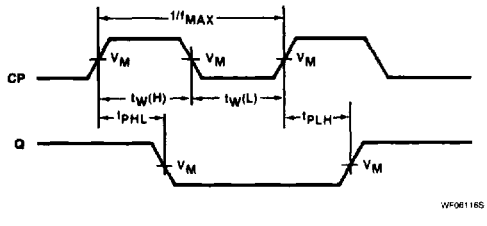
PARAMETER		TEST CONDITIONS		74 $C_L = 15pF$, $R_L = 800\Omega$		74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
				Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1		25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1			27 32		27 32	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2			36		36	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	$C_L = 50pF$ for these parameters	Waveform 1		30 37			ns
t_{PHL}	Propagation delay $\overline{MR}$ to output		Waveform 2		42			ns

NOTE:
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

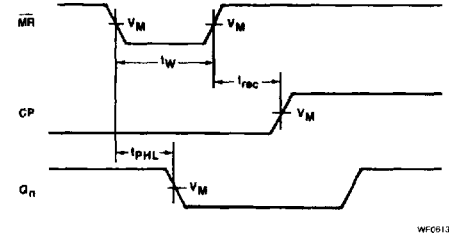
AC SET-UP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74		74LS		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		20		ns
t_s	Set-up time data to clock	Waveform 3	15		15		ns
t_h	Hold time data to clock	Waveform 3	5.0		5.0		ns
t_{rec}	$\overline{MR}$ to clock recovery time	Waveform 2	30		30		ns

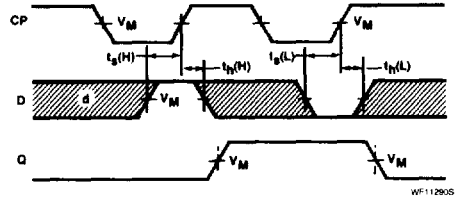
AC WAVEFORMS



Waveform 1. Clock To Output Delays And Clock Pulse Width



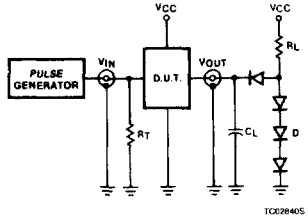
Waveform 2. Master Reset Pulse Width, Master Reset To Output Delay And Master Reset To Clock Recovery Time

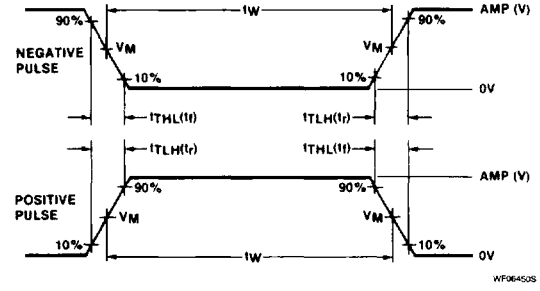


For all waveforms, $V_M = 1.5V$ for 74 and 74S; $V_M = 1.3V$ for 74LS. The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data Set-up And Hold Times

TEST CIRCUITS AND WAVEFORMS





V_M = 1.3V for 74LS; V_M = 1.5V for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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