Signetics

82LS135
2K-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82LS135 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82LS135 includes on-chip decoding and two chip enable inputs for ease of memory expansion, and features Three-state outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

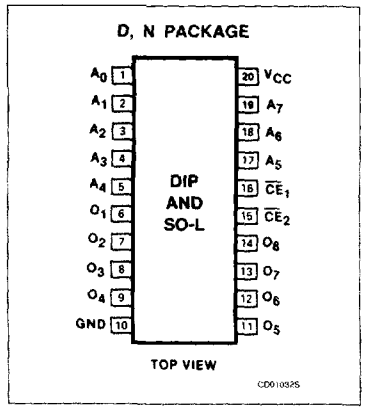
FEATURES

- **Address access time: 100ns max.**
- **Power dissipation: 200μW/bit typ**
- **Input loading: −100μA max**
- **Two chip enable inputs**
- **On chip address decoding**
- **No separate fusing pins**
- **Fully TTL compatible**
- **Unprogrammed outputs are at Low level**
- **Outputs: Three-state**

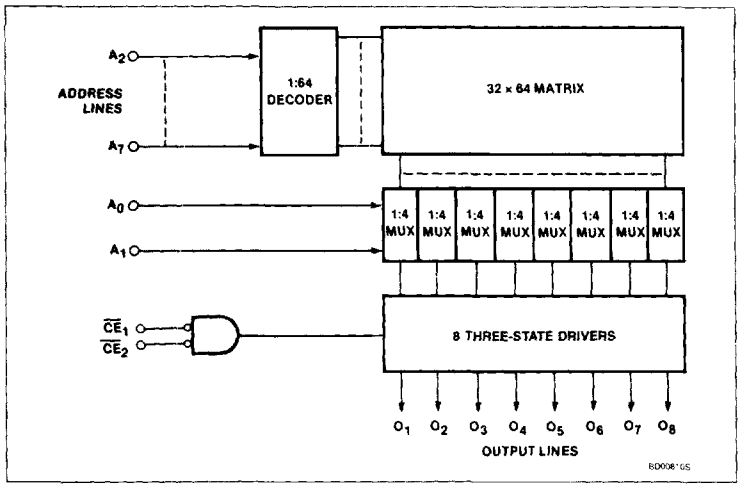
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (256 x 8) — 82LS135

ORDERING CODE

DESCRIPTION	ORDER CODE
Plastic Dual Inline 300mil wide 20-pin	N82LS135 N
Plastic Small Outline 300mil wide 20-pin	N82LS135 D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	V_{dc}
V_{IN}	Input voltage	+5.5	V_{dc}
V_O	Output voltage Off-state	+5.5	V_{dc}
	Temperature range		
T_A	Operating	0 to +75	°C
T_{STG}	Storage	−65 to +150	

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				.80	V
V_{IH}	High		2.0			
V_{IC}	Clamp	$I_{IN} = -12mA$			−1.2	
Output voltage						
V_{OL}	Low	$I_{OUT} = 16mA$			.50	V
V_{OH}	High	$I_{OUT} = -2mA$, High stored	2.4			
Input current						
I_{IL}	Low	$V_{IN} = 0.45V$			100	μA
I_{IH}	High	$V_{IH} = 5.5V$			40	
Output current						
I_{OZ}	Hi-Z State	$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 0.5V$			−40	μA
		$\overline{CE}_1$, $\overline{CE}_2$ = High, $V_{OUT} = 5.5V$			40	
I_{OS}	Short circuit[3]	$\overline{CE}_1$, $\overline{CE}_2$ = Low, $V_{OUT} = 0V$, One stored	−15		−75	ma
Supply current						
I_{CC}		$V_{CC} = 5.25V$		80	100	mA
Capacitance		$V_{CC} = 5.0V$ $\overline{CE}$ = High				
C_{IN}	Input	$V_{IN} = 2.0V$		5		pF
C_{OUT}	Output	$V_{OUT} = 2.0V$		8		

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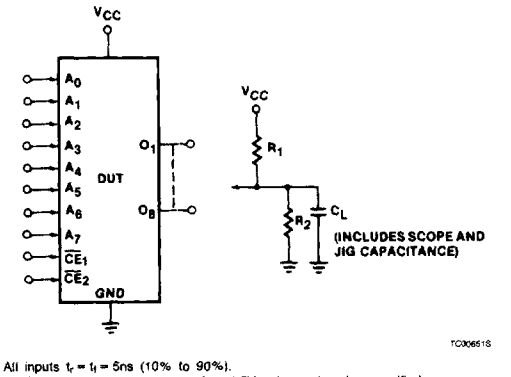
2K-Bit TTL Bipolar PROM (256 x 8) — 82LS135

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ[5]	Max	
Access time[4]						
T_{AA}	Output	Address		70	100	ns
T_{CE}	Output	Chip enable		30	50	
Disable time[6]						
T_{CD}	Output	Chip disable		30	60	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



All inputs $t_r = t_f = 5ns$ (10% to 90%).
All AC parameters are measured at 1.5V unless otherwise specified.

VOLTAGE WAVEFORM