SIEMENS

1 M × 9-Bit Dynamic RAM Module

HYM 91000S/-60/-70/-80

Advanced Information

- 1 048 576 words by 9-bit organization
- Fast access and cycle time
  60 ns access time
  110 ns cycle time (-60 version)
  70 ns access time
  130 ns cycle time (-70 version)
  80 ns access time
  150 ns cycle time (-80 version)
- Fast page mode capability with
  40 ns cycle time (-60/-70 version)
  45 ns cycle time (-80 version)
- Single + 5 V (± 10 %) supply
- Low power dissipation
  max. 4455 mW active (-60 version)
  max. 4000 mW active (-70 version)
  max. 3500 mW active (-80 version)
  CMOS – 50 mW standby
  TTL – 100 mW standby
- Common $\overline{CAS}$ control for eight common data-in and data-out lines
- Separate $\overline{CAS}$ control for ninth bit
- $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only-refresh, Hidden refresh
- 9 decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single in-Line Memory Module with 20,32 mm height
- Pin configuration according to JEDEC standards
- Utilizes nine 1M × 1-DRAMs in 300 mil wide SOJ packages
- 512 refresh cycles / 8 ms

The HYM 91000S-60/-70/-80 is a 1 Mbyte RAM module organized as 1 048 576 words by 9-bit in a 30-pin single-in-line package comprising nine HYB 511000BJ 1 M × 1 DRAMs in 300 mil wide SOJ-packages mounted together with nine 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

Each HYB 511000BJ is described in the data sheet and is fully electrical tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

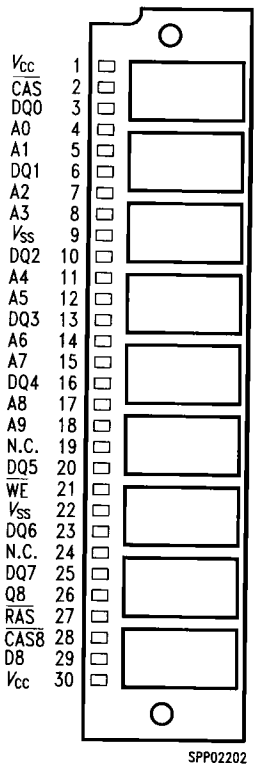
A common CAS controls for eight common data-in and data-out lines.

Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{CAS8}$.

The common I/O feature on the HYM 91000S-60/-70/-80 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYM 91000S-60	Q67100-Q470	L-SIM-30-3	DRAM Module (access time 60 ns)
HYM 91000S-70	Q67100-Q445	L-SIM-30-3	DRAM Module (access time 70 ns)
HYM 91000S-80	Q67100-Q396	L-SIM-30-3	DRAM Module (access time 80 ns)

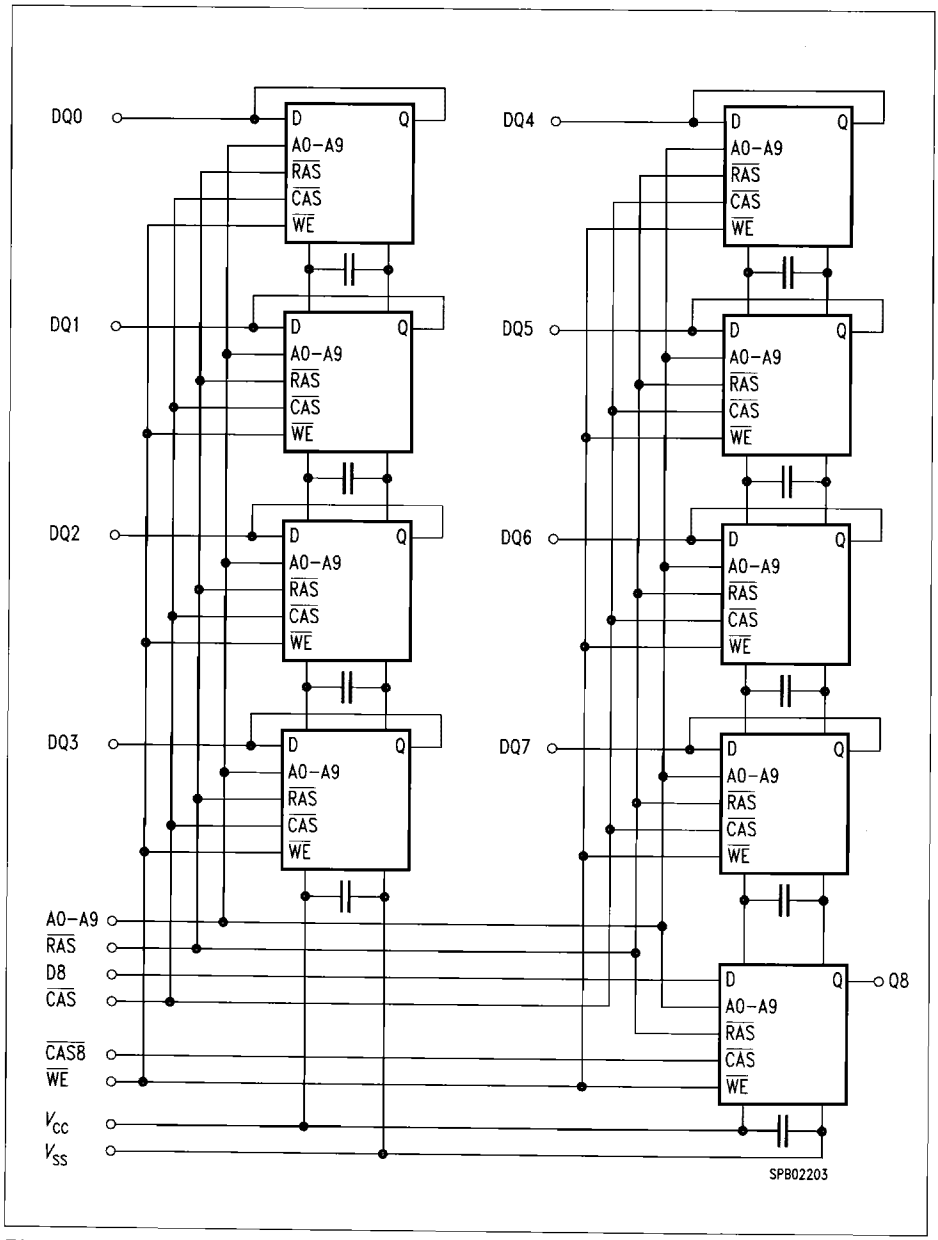


HYM 91000S
(Socket type)

Pin Names

A0-A9	Address Inputs
DQ0-DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{CAS8}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
Vcc	Power Supply (+ 5 V)
Vss	Ground (0V)
N.C.	No Connection

Pin Configuration



Block Diagram

Absolute Maximum Ratings

Operating temperature range ..... 0 to + 70 °C
Storage temperature range..... – 55 to + 125 °C
Soldering temperature ..... 260 °C
Soldering time..... 10 s
Input/output voltage ..... – 1 to + 7 V
Power supply voltage..... – 1 to + 7 V
Power dissipation..... 5.4 W
Data out current (short circuit) ..... 50 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics [1]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	–
Input low voltage	V_{IL}	– 1.0	0.8	V	–
Output high voltage (I_{OUT} = – 5 mA)	V_{OH}	2.4	–	V	–
Output low voltage (I_{OUT} = 4.2 mA)	V_{OL}	–	0.4	V	–
Input leakage current (0 V < V_{IN} < 6.5 V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	–
Output leakage current (DO is disabled, 0 V < V_{OUT} < 5.5 V)	$I_{O(L)}$	– 10	10	µA	–
Average V_{CC} supply current:	I_{CC1}				
HYM 91000S-60		–	810	mA	2), 3)
HYM 91000S-70		–	720	mA	
HYM 91000S-80		–	630	mA	
($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	18	mA	–
Average V_{CC} supply current during $\overline{RAS}$ only refresh cycles:	I_{CC3}				
HYM 91000S-60		–	810	mA	2)
HYM 91000S-70		–	720	mA	
HYM 91000S-80		–	630	mA	
($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					

Notes see page 339.

DC Characteristics (cont'd) [1]

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current during fast page mode: HYM 91000S-60	I_{CC4}	–	630	mA	2), 3)
HYM 91000S-70		–	540	mA	
HYM 91000S-80		–	450	mA	
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling: t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	9	mA	–
Average V_{CC} supply current during $\overline{CAS}$-before-$\overline{RAS}$ refresh mode:	I_{CC6}	–			2)
HYM 91000S-60		–	810	mA	
HYM 91000S-70		–	720	mA	
HYM 91000S-80			630	mA	
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					

Notes see page 339.

Capacitance

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9)	C_{I1}	–	60	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{I2}	–	60	pF
Input capacitance (D8, $\overline{CAS8}$)	C_{I3}		10	pF
I/O capacitance (DQ0 to DQ7)	C_{IO}	–	15	pF
Output capacitance (Q8)	C_O	–	10	pF

AC Characteristics [4) 5)]

T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	150	–	ns
Fast page mode cycle time	t_{PC}	40	–	40	–	45	–	ns
Access time from $\overline{RAS}$ [6) 11)]	t_{RAC}	–	60	–	70	–	80	ns
Access time from $\overline{CAS}$ [6) 11)]	t_{CAC}	–	20	–	20	–	20	ns
Access time from column address [6) 12)]	t_{AA}	–	30	–	35	–	40	ns
Access time from $\overline{CAS}$ precharge [6)]	t_{CPA}	–	30	–	35	–	40	ns
$\overline{CAS}$ to output in low-Z [6)]	t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay [7)]	t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall) [7)]	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	–	50	–	60	–	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100000	70	100000	80	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	20	–	ns
$\overline{CAS}$ hold time	t_{CSH}	60	–	70	–	80	–	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time [11)]	t_{RCD}	20	40	20	50	20	60	ns
$\overline{RAS}$ to column address delay time [12)]	t_{RAD}	15	30	15	35	15	40	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns

Notes see page 339.

AC Characteristics [4] [5] (cont'd)
T_A = 0 to 70 °C; V_{CC} = 5 V ± 10 %; t_T = 5 ns

Parameter	Symbol	Limit Values						Unit
		-60		-70		-80		
		min.	max.	min.	max.	min.	max.	
Column address hold time ref. to $\overline{RAS}$	t_{AR}	50	–	50	–	60	–	ns
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns
Read command hold time [8]	t_{RCH}	0	–	0	–	0	–	ns
Read command hold time ref. to $\overline{RAS}$ [8]	t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	15	–	15	–	15	–	ns
Write command hold time ref. to $\overline{RAS}$	t_{WCR}	50	–	55	–	60	–	ns
Write command pulse width	t_{WP}	15	–	15	–	15	–	ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time [9]	t_{DS}	0	–	0	–	0	–	ns
Data hold time [9]	t_{DH}	15	–	15	–	15	–	ns
Data hold time ref. to $\overline{RAS}$	t_{DHR}	50	–	55	–	60	–	ns
Refresh period	t_{REF}	–	8	–	8	–	8	ms
Write command setup time [10]	t_{WCS}	0	–	0	–	0	–	ns
$\overline{CAS}$ setup time (CBR cycle)	t_{CSR}	10	–	10	–	10	–	ns
$\overline{CAS}$ hold time (CBR cycle)	t_{CHR}	30	–	30	–	30	–	ns
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0	–	0	–	0	–	ns
$\overline{CAS}$-precharge time (CBR counter test cylce)	t_{CPT}	40	–	40	–	40	–	ns
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	10	–	ns

Notes see page 339.

Waveforms see page 391.

Notes for pages 335 to 338:

1) All voltages are referenced to V_{SS}.

2) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.

3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.

4) An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.

5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL}.

6) Measured with a load equivalent of 2 TTL loads and 100 pF.

7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit condition and is not referenced to output voltage levels.

8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{WRITE}}$ leading edge in read-write cycles.

10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min.), the cycles is an early write cycle and data out pin will remain open circuit (high impedance).

11) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

12) Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.