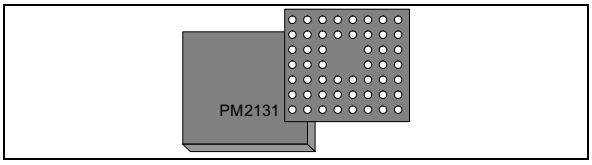
PM2131

4 A switching mode battery charger with power path

Datasheet - production data



Features

- 4 A DC/DC step-down battery charger
  - High efficiency up to 92%
  - Operation at 1.6 MHz with a 1 μH coil
  - Dual paths with 2.0 A integrated power field-effect transistor (FET)
  - Constant current constant voltage (CCCV) mode
  - Flexible charge parameter programming with predefined configurations
  - Compliant with multiple battery chemistry (LiCO2, LiFePO4, Ni-rich)
  - Output current regulation
  - High accuracy voltage regulation: <1%
  - Compliant with USB battery charging specification 1.2 and USB standard 2.0
  - External power source detections and charger priority control
- Battery charger safety and protection
  - 20 V absolute maximum input voltage ratings
  - Up to 16 V operating voltage
  - Input overvoltage and overcurrent protection
  - Safety timer with reset control
  - Reverse polarity and leakage protection
  - Down -2 V input voltage protection
  - Battery and die thermal protections
  - Current sensing and built-in current limiting
  - Battery overvoltage protection and anti-overshoot algorithm
  - Compliant with IEEE 1725-2006, JISC8714 (Japan), CTTL YDT1591 (China) standards
- Boost mode
  - For USB On-The-Go supply to provide 5 V and 1 A on VBUS when A device
  - Programmable boost voltage: 4.5 V, 5.0 V, 7.0 V and 11.0 V with 5 W max.
  - No external component needed
- Miscellaneous
  - Power-path mode with external FET and internal current source for empty battery case
  - I²C™ control
  - LED driver for charging indicator
  - Interrupt and wakeup signal
  - Autonomous charging algorithm or software control by system
  - External power source optimization loop

Description

The PM2131 is a fully integrated 4 A switching mode battery charger built upon a dual 2.0 A DC-DC down converter with integrated FET. This dual converter structure allows high efficiency at high current with small size external components. The two paths can remain separated when needed.

The battery CCCV charging mode is either fully autonomous when operating in standalone or software controlled by the host. Multiple charging parameters can be modified or monitored by I²C and through interrupt pin with several default settings. Also, the PM2131 permanently monitors several key parameters for charging algorithm and safety. The PM2131 features the power-path mode which allows the system to run in empty battery conditions and battery aging to be improved when the wall outlet adapter is plugged.

The PM2131 is ideal for tablets and smartphones. It fits perfectly portable/mobile devices and large battery capacity applications with parallel single cell Li-ion battery pack requiring fast charging.

Contents

List of figures

List of tables

1 Introduction

The PM2131 is a 3 A or 4 A switch mode battery charger based on a dual high efficiency DC-DC step-down battery charger. Each converter operates at 1.6 MHz with a 1 μH coil providing the best efficiency with a small PCB footprint.

DC-DC charging path is built according to the following loops:

- Input power loop: to optimize the power coming from the USB or an external power source.
- Input current limitation loop: to guarantee the input current for a USB adapter compatible with the USB specification and charger detection.
- Output current loop: to regulate the charging current.
- Output voltage loop: to regulate the battery charging voltage in case of charging mode.
- Output voltage loop: to regulate a VSYSTEM voltage for applications where power path mode is without charging.

The PM2131 also includes the power path feature with external FET. The power path feature allows the host and its environment in empty battery conditions to be run.

Furthermore, the die temperature monitoring is always active and gives an interrupt as soon as the die temperature reaches a given thermal warning threshold and stops the charging at a thermal shutdown threshold.

The PM2131 is compliant with the USB 2.0 standard and USB battery charger 1.2 standard.

For high charging current applications up to 4 A, on the application board, the two DC-DC step-down inputs, VPWR and VUSB must be externally shorted. For applications with two separated charging paths, each charging path can be enabled separately (for instance, one path dedicated to USB charging and the other one to wall adapter charging, alternatively the second path can be used as boost).

Battery charging safety is taken into account in charging algorithm and in DC-DC charging path design. Accurate battery temperature monitoring is performed using NTC=1% accuracy, (battery temperature thresholds are programmable). An innovative system minimizes the overshoots on battery line during CV mode operation and in presence of huge load transient (like GSM burst load transient).

The PM2131 embeds flexible programming capability thanks to the following:

- Multiple registers enabling on-the-fly tuning of all parameters through I²C interface.
- Multiple charging control strategies from autonomous hardware charging to fully software-controlled by the host.
- Several predefined default register configurations to fit different application needs, at power-up. Default register settings are recovered in the following cases:
  - The external power source is unplugged.
  - The host software is no more available.
  - The battery is disconnected.

2 Pin description

This section provides a description of the ball assignment. The ball description refers to the WLCSP package.

2.1 The PM2131 ball assignment (bottom view, ball side view)

Table 1. WLCSP 52 - ball assignment

	1	2	3	4	5	6	7	8
G	VPWR	VPWR	VPWR	LED	NC	VUSB	VUSB	VUSB
F	VPWR	VPWR	NC	NC	NC	NC	VUSB	VUSB
E	VLXPWR	VLXPWR	VLXPWR			VLXUSB	VLXUSB	VLXUSB
D	GNDPWR	GNDPWR	GNDPWR			GNDUSB	GNDUSB	GNDUSB
C	BSTRAPPWR	SENSEPWR	SENSE_ COMMON	NTC	ENN	IRQ	SENSEUSB	BSTRAPUSB
B	VSYSTEM	VSYSTEM	VBATSENSE	WAKEUP	GND	LPN/USBBC	SDA	SCL
A	VBAT	VBAT	VBAT	GPP	GND	CVIS	VREF	NC

2.2 Ball description

The PM2131 includes the following ball types:

VDDD / VDDA = digital and analog positive supply

GNDD / GNDA = digital and analog ground

DO / DI / DIO = digital output /input/input-output

AO / AI / AIO = analog output /input/input-output

Table 2. Ball description

I/O balls	Name	Type	Description
DC-DC battery charger path 1			
G1, G2, G3 F1, F2	VPWR	VDDA	Power supply input from PWR/wall adapter Shorted with VUSB for high charging current applications
E1, E2, E3	VLXPWR	AO	Coil connection for path VPWR
D1, D2, D3	GNDPWR	GNDA	Power ground for path VPWR
C1	BSTRAPPWR	AO	Bootstrap capacitor for high-side MOSFET gate driver VPWR DC/DC charger path 10 nF ceramic capacitor sets from BSTRAPPWR to VLXPWR

Table 2. Ball description (continued)

I/O balls	Name	Type	Description
C2	SENSEPWR	AI	Path VPWR sense for current measurement (sense resistor: 68 mΩ, 1% for 1.5 A) (sense resistor: 47 mΩ, 1% for 2.0 A)
DC-DC battery charger path 2			
G6, G7, G8 F7, F8	VUSB	VDDA	Power supply input from USB adapter Shorted with VPWR for high-current charging applications
E6, E7, E8	VLXUSB	AO	Coil connection for path USB
D6, D7, D8	GNDUSB	GNDA	Power ground for path USB
C8	BSTRAPUSB	AO	Bootstrap capacitor for high-side MOSFET gate driver VUSB path DC-DC charger path 10 nF ceramic capacitor sets from BSTRAPUSB to VLXUSB
C7	SENSEUSB	AI	Path USB sense for current measurement (sense resistor: 68 mΩ, 1%, for 1.5 A) (sense resistor: 47 mΩ, 1%, for 2.0 A)
Battery dedicated features			
C3	SENSE_ COMMON	AI	Common input for sense current measurement shared by VPWR and VUSB DC-DC charger paths
C4	NTC	AI	External NTC thermal resistor input
B3	VBATSENSE	AI	Accurate battery voltage monitoring input
A1, A2, A3	VBAT	AI	Battery voltage
Interface			
C5	ENN	DI	Battery charging enable. Active low
C6	IRQ	DO	Interrupt and charger status output (open drain) – active low
B4	WAKEUP	DO	Interrupt to wake up the system (open drain)
B7	SDA	DIO	I²C serial data
B8	SCL	DI	I²C serial clock (SCL) (always slave I²C)
B6	LPN/USBBC	DI	When the external power source is not connected: – Used to control the low power mode (active low) When external power source is connected: – Used to increase the input current limitation
LED indicator output			
G4	LED	AO	LED driver output current source
Other balls			
B1, B2	VSYSTEM	AIO	VSYSTEM voltage
A4	GPP	AO	External power path MOSFET gate driver

Table 2. Ball description (continued)

I/O balls	Name	Type	Description
A6	CVIS	AO	Internal regulated charger voltage
A7	VREF	AO	Internal reference voltage It cannot be loaded
B5, A5	GND	GNDA	Analog ground
G5 F3, F4, F5, F6, A8	NC	/	Not connected

3 Electrical characteristics

This section outlines the electrical characteristics of the PM2131.

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Parameter	Conditions	Min.	Typ.	Max.	Unit
VBAT maximum voltage		-0.3		4.8	V
VPWR maximum input voltage		-2		20	V
VUSB maximum input voltage		-2		20	V
Maximum voltage on analog I/O				4.8	V
Maximum voltage on digital I/O				4.8	V
Minimum/maximum ambient temperature		-40		85	°C
Minimum/maximum junction operating temperature		-40		125	°C
Minimum/maximum junction rating temperature		-40		150	°C
Electrostatic discharge (ESD)	Human body model (HBM) - JESD22-A114-B	+/- 1			kV
	Charged device model (CDM) - JESD22 – C101	+/- 500			V

3.2 Thermal information

Table 4. Thermal information

Package	R_{th} (°C/W)	TA = 25 °C Power rating [W]	TA = 65 °C Power rating [W]	Derating factor above TA = 25 °C (W/°C)
WLCSP 3.3x2.9	44	2.27	1.36	0.023

3.3 Electrical operating characteristics

All parameters are set for VPWR / VUSB = 5 V, VBAT = 3.6 V and ambient temperature is 25 °C. The device is measured on the board (as described in *Section 8*). Specific layout recommendations have to be respected in order to optimize thermal behavior of the application. Otherwise, specific parameters are indicated in the condition column.

Table 5. Electrical operating characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
Battery current consumption in power OFF mode	Battery charger OFF, no external power source connected, LPN ball at low level	-	70	-	µA
Battery current consumption in power ON mode	Battery charger OFF, no external power source connected, LPN ball at high level	-	180	-	µA

3.4 DC-DC charger electrical characteristics

Table 6. Electrical characteristics for DC-DC charger

Parameter	Conditions	Min.	Typ.	Max.	Unit
VUSB / VPWR / VBAT power up					
VPWR / VUSB operating voltage range		2.1		16.5	V
VPWR / VUSB detection positive threshold	Rising transition		3.8		V
VPWR / VUSB detection negative threshold	Falling transition	2.0	2.1		V
VPWR / VUSB overvoltage positive threshold	Programmable parameter(1) reg@11h(bit2-0) & reg@15h(bit2-0) <000> <001> <010> <011> or <111> <100> <101> <110>		 6.0 6.5 7.5 10.5 12.0 14.0 16.0		 V V V V V V V
VPWR / VUSB overvoltage negative threshold	Programmable parameter(1) reg@11h(bit2-0) & reg@15h(bit2-0) <000> <001> <010> <011> or <111> <100> <101> <110>		 5.83 6.14 7.08 10.0 11.0 12.9 15.00		 V V V V V V V
VPWR / VUSB detection VALID positive threshold		4.4	4.6	4.75	V
VPWR / VUSB detection VALID hysteresis		100		200	mV
VBAT / VSYSTEM power up for active I^2C	VBAT rising transition. No VUSB plug, no VPWR plug. Ball LPN/USBBC high	2.3			V

Table 6. Electrical characteristics for DC-DC charger (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
VBAT / VSYSTEM power OFF mode	VBAT falling transition. No VUSB plug, no VPWR plug. Ball LPN/USBBC high or low	2.1			V
Battery charger					
Charging float voltage regulation	Programmable parameter(1) (2)			3.5 to 4.5	V
Charging float voltage regulation level programming step			0.025		V
Charging float voltage regulation accuracy	Whole range			1	%
Charging float voltage regulation overshoot	Iload 2 A ->1 mA in 10 μs Cbat = 100 μF			20	mV
Internal charging (hardware charging mode)					
Charging current in pre-charge mode (trickle mode)			75		mA
Pre-charge voltage detection threshold			2.5		V
Pre-charge voltage detection hysteresis		100		250	mV
Reduced charge current	Programmable parameter Vprecharge < VBAT< (VSYSTEM - 0.3V) or (VSYSTEM-0.15V) according to reg@0Ah, bit4(3)			100 200 400	mA
Internal charge current	Programmable parameter step 100 mA(1)			100 to 1100	mA
Direct charging (software charging mode)					
Fast charge current	Programmable parameter step 145 mA(1) R1 = 47 mΩ (1%) R2 = 47 mΩ (1%)			145 to 4000	mA
Fast charge current accuracy with two paths selected in parallel (reg@01, bit0=0)	<0011> <0101> <1010> <1111> R1 = 47 mΩ (1%) R2 = 47 mΩ (1%)	0.77 1.30 2.61 3.90	0.86 1.44 2.9 4.34	0.95 1.58 3.19 4.77	A A A A

Table 6. Electrical characteristics for DC-DC charger (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
End-of-charge current level	Programmable(4) <00> <01> <10> <11> R1 = 47 mΩ (1%) R2 = 47 mΩ (1%)		 145 220 435 580		 mA mA mA mA
VBATLOW detection threshold: automatic transition from internal charging to external charging mode	Reg@22h=01h to enable feature reg@23h bit<4:0> programmable(4) VBAT rising transition		2.3 to 4.2		V
	PM2131UHT, PM2131AHT		3.9		V
DC-DC charger efficiency(5) – external charging mode	VPWR & VUSB= 5 V single path=0 L_ESR = 50 mΩ, L = 1 µH VBAT = 4.0 V				
	I_{BAT}=0.6 A		92.5		%
	I_{BAT}=1.6 A		92.1		%
	I_{BAT}=2.2 A		90.8		%
	I_{BAT}=3.0 A		88.9		%
	I_{BAT}=4.0 A		86.3		%
DC-DC charger efficiency – external charging mode	VPWR & VUSB= 12 V single path=0 L_ESR = 50 mΩ, L = 1 µH VBAT = 4.0 V				
	I_{BAT}=0.6 A		85.8		%
	I_{BAT}=1.6 A		87.4		%
	I_{BAT}=2.2 A		87.2		%
	I_{BAT}=3.0 A		86.3		%
	I_{BAT}=4.0 A		83.9		%
Power path feature					
Switching frequency		TBC	1.6	TBC	MHz

Table 6. Electrical characteristics for DC-DC charger (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
VSYSTEM power path mode output voltage regulation with reg@0Ah, bit4=1	reg@10h, bit[7,6] 00 with VBAT<2.35 V & USBBC=0 00 with VBAT<3.45 V & USBBC=1 01 with VBAT<3.45 V 10 with VBAT<3.75 V 11 with VBAT<4.15 V (1)	 2.3 3.4 3.4 3.7 4.1	 2.5 3.6 3.6 3.9 4.3		V
	When VBAT > VSYSTEM setting minus 150 mV (follower mode)		VBAT + 0.15 V		
	When VBAT > 4.35 V saturation mode		4.5		V
VSYSTEM power path mode output voltage with reg@0Ah, bit4=0	reg@10h, bit[7,6] 00 with VBAT<2.2 V & USBBC=0 00 with VBAT<3.3 V & USBBC=1 01 with VBAT<3.3 V 10 with VBAT<3.6 V 11 with VBAT<4.0 V(1)	 2.3 3.4 3.4 3.7 4.1	 2.5 3.6 3.6 3.9 4.3		V
	When VBAT is higher than target VSYSTEM setting minus 300 mV (follower mode)		VBAT + 0.3 V		
	When VBAT > 4.2 V (saturation mode)		4.5		V
VUSB input current limitation in hardware mode	VUSB = 5 V, L_ESR = 50 mΩ, L = 1 µH R2(USB) = 47 mΩ(1%)				
	PM2131AST				
	LPN/USBBC = low LPN/USBBC = high	390 1950		435 2170	mA mA
	PM2131UHT				
	LPN/USBBC = low LPN/USBBC = high	390 1950		435 2170	mA mA
	PM2131AHT				
	LPN/USBBC = low LPN/USBBC = high	130 1950		145 2170	mA mA

Table 6. Electrical characteristics for DC-DC charger (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
VUSB input current limitation after charger detection	Programmable reg@11h bit<6:3> R2(USB) = 47 mΩ(1%) <0000> <0001> <0110> <1010> <1111>	 65 130 650 1170 1950	 	 100 145 725 1300 2170	 mA mA mA mA mA
VUSB input current limitation programming step	reg@11h bit<6:3>		145		mV
VPWR input current limitation in hardware mode	VPWR = 5 V, L_ESR = 50 mΩ, L = 1 µH R1(VPWR) = 47 mΩ(1%)				
	PM2131AST, PM2131UHT				
		1950		2170	mA
	PM2131AHT				
	LPN/USBBC =low LPN/USBBC =high	130 1950		145 2170	 mA
VPWR input current limitation after charger detection	Programmable reg@15h bit<6:3> R2(USB) = 47 mΩ(1%) <0000> <0001> <0110> <1010> <1111>	 65 130 650 1170 1950	 	 100 145 725 1300 2170	 mA mA mA mA mA

1. Programmable parameter values are detailed in the register map. Programmable parameters can be modified through I^2C.
2. Drop ((VPWR/VUSB)-VBAT)>500 mV at max. charging current (4 A).
3. The reduced current charging can be disabled through I^2C in case of optimized power dissipation of global applications.
4. End-of-charge can be managed autonomously by the PM2131 with some specific ordering codes, but in that case, user needs to consider system current load value before selecting EOC threshold. We recommend end-of-charge to be managed by host with specific circuitry distinguishing between system load current and battery charging current (gas gauge approach).
5. See the DC-DC efficiency graphs (*Figure 1*, *Figure 2*, *Figure 3*).

Figure 1. Efficiency versus charging current for different coil references - case 1

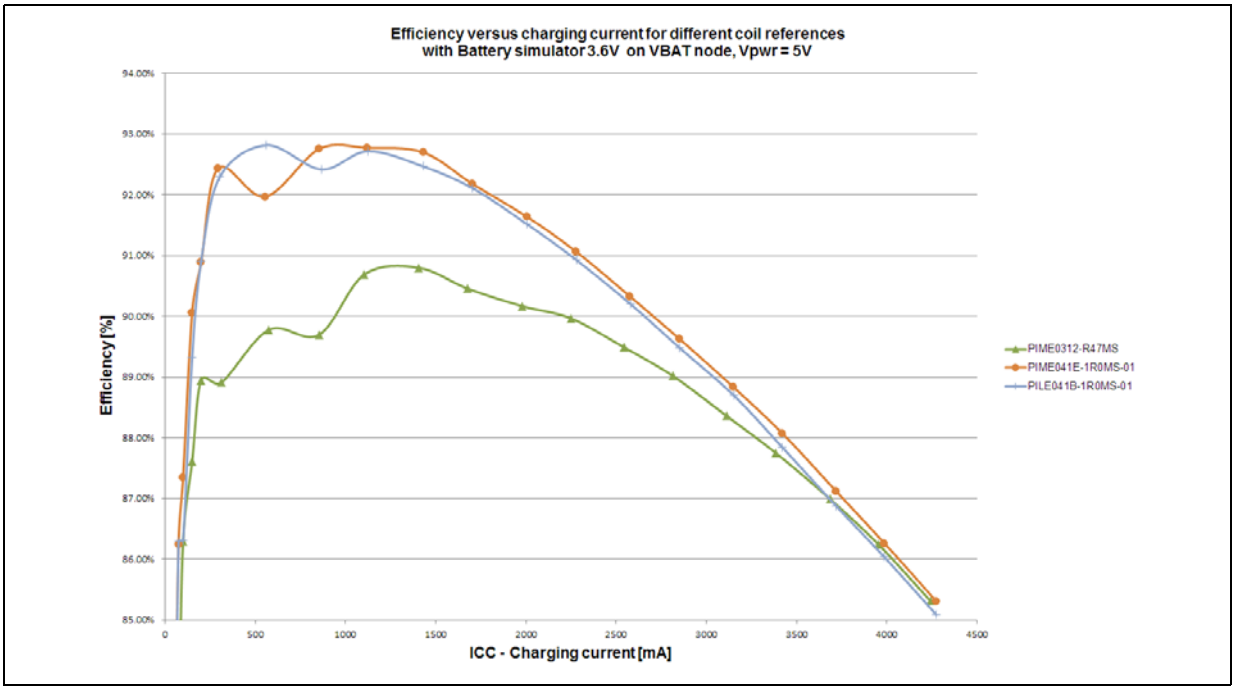


Figure 2. Efficiency versus charging current for different coil references - case 2

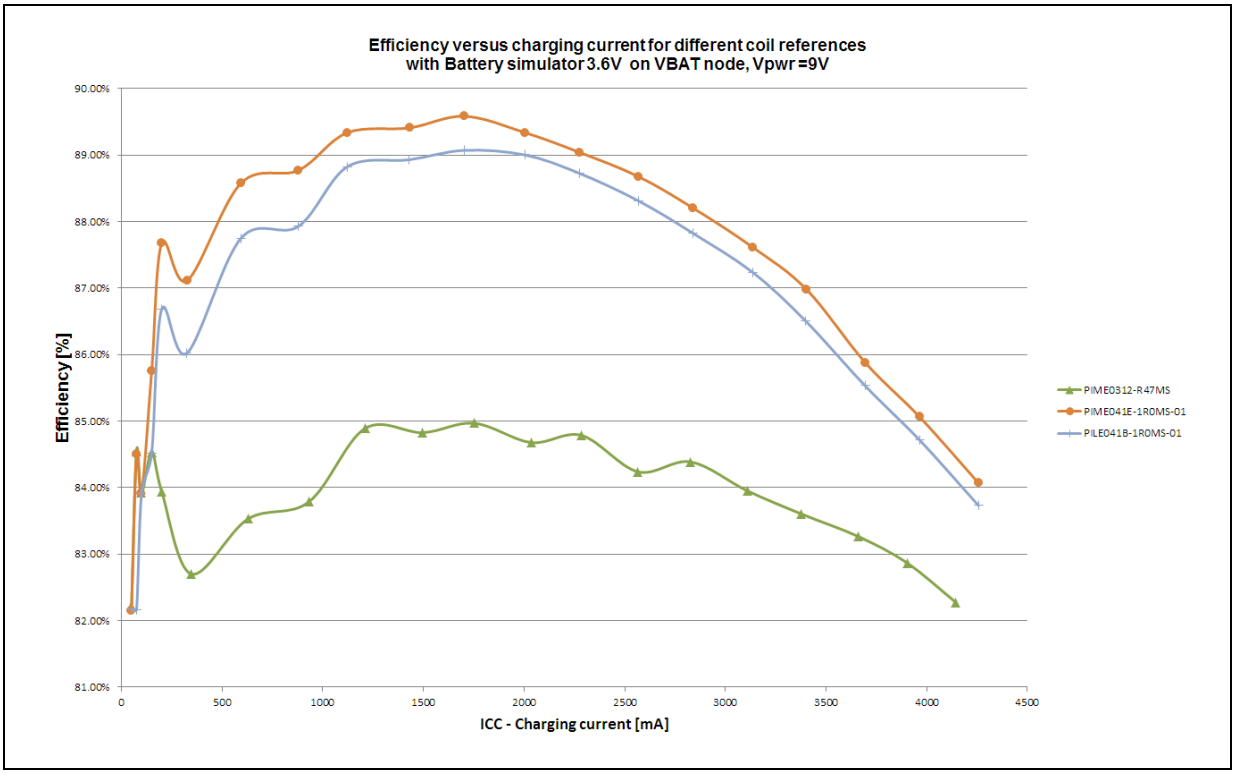
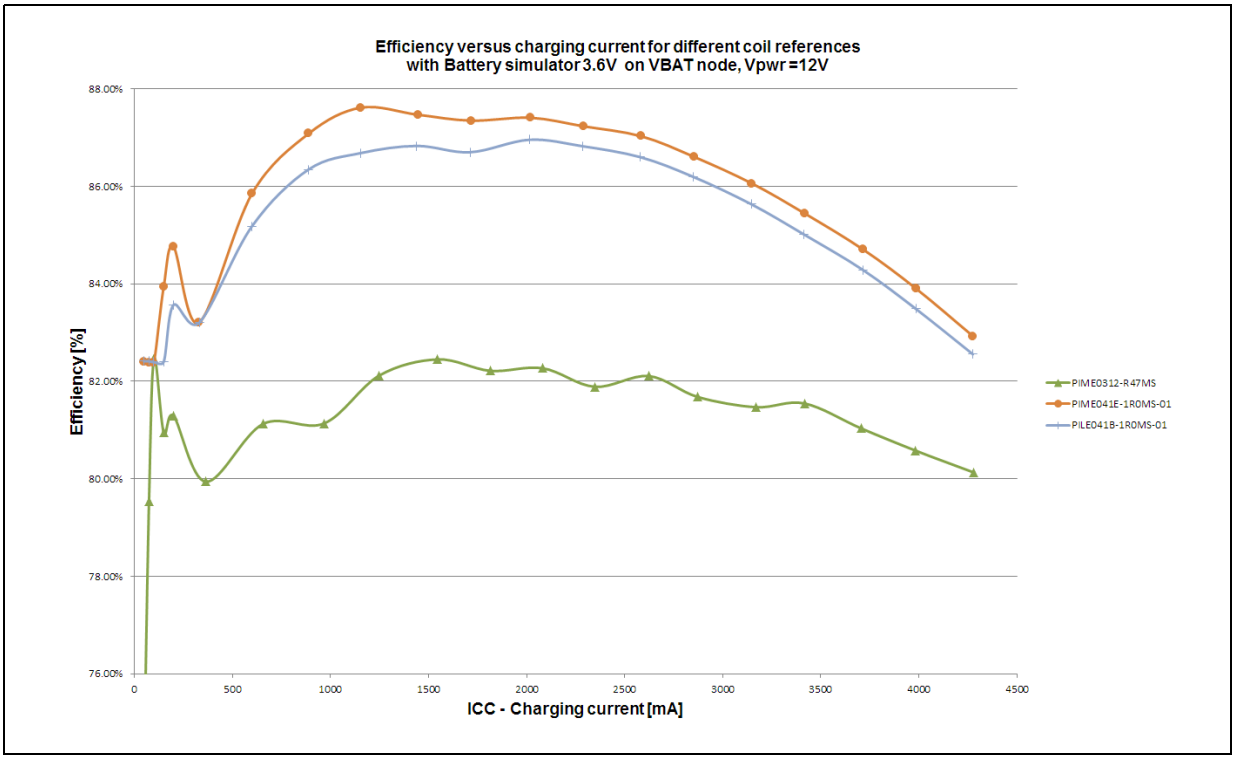


Figure 3. Efficiency versus charging current for different coil references - case 3



3.5 Boost mode

The boost mode works on both USB and VPWR paths.

All parameters are set for VBAT = 3.6 V and the ambient temperature is 25 °C.

Table 7. VPWR / VUSB BOOST mode parameter table

Parameter	Conditions	Min.	Typ.	Max.	Unit
VPWR / VUSB output voltage in boost mode	Programmable		4.5		V
	OTG output voltage	4.75	5.0	5.25	V
			7.0		V
			11.0		V
VPWR / VUSB boost mode output current	When V_{OUT} = 4.5 V	1000			mA
	When V_{OUT} = 5.0 V	1000			mA
	When V_{OUT} = 7.0 V	700			mA
	When V_{OUT} = 11.0 V	450			mA
IBAT quiescent current in boost mode	No load on VPWR or VUSB		TBD		µA
Start-up time				5	ms

Table 7. VPWR / VUSB BOOST mode parameter table (continued)

Parameter	Conditions	Min.	Typ.	Max.	Unit
5 V boost mode efficiency	VBAT = 3.0 V Iload = 200 mA Iload = 500 mA Iload=1A		 80 85 78		 % % %
	VBAT = 4.0 V Iload = 200 mA Iload = 500 mA Iload=1A		 78 88 88		 % % %
7 V boost mode efficiency	VBAT = 3.0 V Iload = 200 mA Iload = 500 mA Iload=700mA		 77 81 77		 % % %
	VBAT = 4.0 V Iload = 200 mA Iload = 500 mA Iload=700mA		 78 85 85		 % % %

3.6 Temperature monitoring

Table 8. Temperature monitoring

Parameter	Conditions	Min.	Typ.	Max.	Unit
Die thermal warning positive threshold	Programmable parameter(1)	110		140	°C
Die thermal warning hysteresis			20		°C
Die thermal shutdown positive threshold			150		°C
Die thermal shutdown hysteresis			20		°C
Battery charge minimum temperature range	Programmable parameter(1)	-5		10	°C
Battery charge maximum temperature range	Programmable parameter(1)	45		65	°C
Battery temperature accuracy	NTC is 1% accuracy	-3		+3	°C
NTC external resistance coefficient			3964		
NTC external resistance value	Programmable parameter (1) NTC is 1% accuracy		10 47 100		kΩ

1. Programmable parameter values are detailed in the register map. Programmable parameters can be modified through I^2C.

3.7 Digital interface I/O electrical parameters

Table 9. Input pin: ENN, LPN/USBBC

Parameter	Conditions	Min.	Typ.	Max.	Unit
Logic input pin (ENN, LPN/USBBC)					
Debouncing time ENN	Rising or falling transition		1		ms
Debouncing time LPN/USBBC rising high	With VPWR=VUSB=0		0		ms
	With VPWR or VUSB>VBAT		1		ms
Debouncing time LPN/USBBC falling low	With no charger plug With charger already plug		1 1		s ms
Input high threshold level	With VSYSTEM >2.3 V	1 V		VBAT / VSYSTEM	V
Input low threshold level		0.0		0.5	V
Logic output pin (IRQ, WAKEUPN)					
Output low threshold level	Open drain (active low) Sink current = 5 mA				V
I^2C interface pin (SDA, SCL)					
Input high threshold level	Compatible with 1.8 V or 3.3 V pull-up line	0.6		VBAT / VSYSTEM	V
Input low threshold level	Compatible with 1.8 V or 3.3 V pull-up line	0		TBC	V
f_{SCL} SCL clock frequency	Default hardware setting			400	kHz
I^2C communication active	VSYSTEM > 2.3V, no VUSB / no VPWR plug LPN/USBBC= high LPN/USBBC= low		 Yes No		
	VSYSTEM < 2.3 V, no VUSB / no VPWR plug LPN/USBBC= high LPN/USBBC= low		 No No		
	VUSB or VPWR > 3.8 V LPN/USBBC= high LPN/USBBC= low		 Yes Yes		

3.8 LED electrical characteristics

Table 10. LED electrical characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
LED current source	Programmable parameter[1]				mA
	<01>			1	
	<00>			2.5	
	<10>			5	
	<11>			10	

1. Programmable parameter values are detailed in the register map. Programmable parameters can be modified through I^2C.

4 DC-DC battery charger with power path

This section provides a description of the high efficiency DC-DC battery charger in power path configuration. The PM2131 is built with two DC-DC charger paths working:

- Sequentially, according to priority definition between the two external charger inputs for applications with separated input charger connectors. USB and VPWR are two different charging paths.
- In parallel, for high-current charging applications up to 4.0 A. USB and VPWR have to be shorted. The charging uses one path only, and then the host enables the second path after charger recognition.
- In parallel, for high-current charging applications up to 4.0 A. USB and VPWR have to be shorted. Both paths are enabled by startup, with high-current setting, not compliant with USB standard. A specific ordering code is needed.

Both DC-DC chargers are based on PWM topology with the chances of regulating the battery charging current and battery voltage during the charging operation. There is also the possibility to regulate the application supply VSYSTEM in power path mode.

4.1 The PM2131 description

The battery charging algorithm is CCCV (constant-current, constant-voltage) with overshoot prevention.

An external short-circuit must be designed on the PCB board to connect together the two paths (VPWR and VUSB) in case of high-current charging applications.

Because of the flexible programmability, classical and emerging battery technologies can be supported (LiCO2, LiFePO4, Ni-rich).

The PM2131 can operate in a fully standalone mode, hardware control mode charges the battery even if the system remains in power-down mode, for example when the battery voltage is too low. In the hardware control mode, predefined parameters are used to control the charging. (see *Section 10: Ordering information*).

The PM2131 can also operate under host controlled mode, so-called software control mode, where the PM2131 is aware that the software is still active through a watchdog which must be reset regularly. In case of the watchdog expires, the PM2131 stops charging, registers are reset to their predefined parameters (default value) and an interrupt is generated.

A valid external power source is automatically recognized by the PM2131 on VUSB balls and/or on VPWR balls. If a valid external power source is plugged, the PM2131 can wake up the system by driving the WAKEUP ball to low level and automatically starts the VSYSTEM voltage generation and the charging when enabled (if programmed through default parameter). If an invalid external power source is detected, the PM2131 doesn't start neither the VSYSTEM voltage generation nor charging and no information is provided on WAKEUP ball, which remains at high level.

In case of invalid external power sources connected on USB balls, voltage sources are higher than a programmable value PPUSBOVVlevel:

- The DC-DC circuitry is kept in OFF mode and VSYSTEM voltage is not generated
- The external MOSFET is kept closed, the battery supplies the application
- The battery charging operation doesn't start
- An interruption of overvoltage on input charger voltage is generated
- The information of charger plug is released on WAKEUP ball even if the charger is detected as invalid due to overvoltage

On VPWR path, an additional circuitry can be added to detect a sine wave AC adapter plugged (for specific ordering code only). This feature is not activated for application USB compliance with VUSB and VPWR balls shorted. In case of sine wave AC adapter plug or VPWR overvoltage:

- The DC-DC circuitry is kept in OFF mode and VSYSTEM voltage is not generated
- The external MOSFET is kept closed, the battery supplies the application
- The battery charging operation doesn't start
- An interruption of overvoltage on input charger voltage is generated
- The information of charger plug is released on WAKEUP ball even if the charger is detected as invalid due to overvoltage

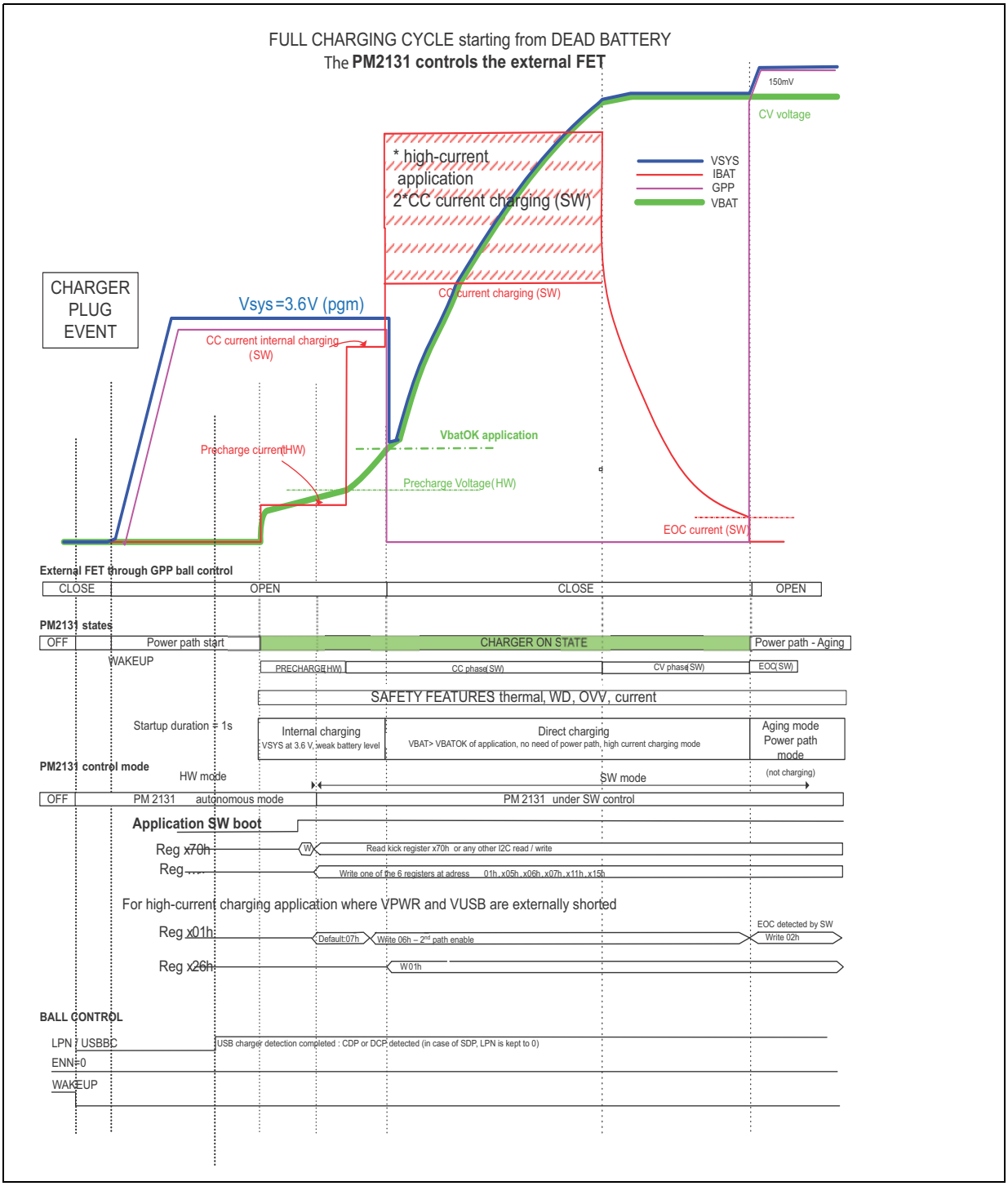
The DC-DC charger paths have an embedded reverse polarity protection such that when the external power source is not plugged or its voltage is below the battery voltage, no current flows from the battery to prevent battery discharging.

Moreover, the PM2131 embeds an input reverse polarity protection below -2 V. External protection is needed to protect the PM2131 input from full reverse polarity.

The PM2131 integrates an interrupt output named IRQ to inform the system when an event occurs. This ball is used to provide the charging status, the external power source and the global system information or to request specific actions from the system.

The PM2131 sends interruptions onto IRQ ball to inform the system about the external power source plug/unplug, battery charging phases, battery temperature monitoring, safety watchdogs and other safety features. An interrupt handler informs the system host about the source or nature of the interrupt through the I²C.

Figure 4. Full charging cycle starting from the dead battery



4.2 Power path mode description

In power path mode, the battery is connected to the system through an external FET driven by the PM2131 GPP ball. This allows the battery to be disconnected from the system in the following cases:

- To run the system when battery is empty (external FET is open)
- To disconnect the battery when the charging cycle is completed and external power source remains plugged

The PM2131 requires the following external EBOM (see *Figure 9*):

- An external MOSFET P1 (FDZ371PZ) with low $R_{DS(on)}$, the source of the external MOSFET is connected to VSYSTEM balls, and its drain is connected to VBAT balls. The ball GPP drives the gate of this MOSFET giving the chance of charging the battery through this external driving path.
- Few decoupling capacitors on the VSYSTEM and VBAT.

The external FET is used:

- In reverse ON mode to supply the application from the battery when no input charger is plugged in.
- In ON mode to charge the battery with high-current; when the battery voltage is high enough to supply the application.
- In OFF mode to disconnect VBAT and VSYSTEM nodes for power path setup (startup with dead battery, charging battery with internal current source, aging mode with full charge battery).

The external FET is controlled by the GPP ball. The PM2131 controls automatically the external FET as per two following conditions:

- When an external power source is not plugged, the FET is closed (forced in reverse ON mode).
- When VSYSTEM voltage drops below VBAT, the FET is closed. This may happen when the peak current from the system exceeds the capability from the external power source. FET automatic closure enables the battery to provide the required extra current.

When the voltage battery is high enough to supply the application and when a charger is connected, the software can close the external FET through I^2C to enable high charging mode or to open the external FET for the “aging mode” (when battery is fully charged).

4.2.1 VSYSTEM generation and host wakeup

After a charger plug on USB and/or VPWR balls, the PM2131 starts automatically to regulate a voltage on VSYSTEM node, opening the external FET. VSYSTEM is regulated as follows:

- A fixed programmable value (3.6 V or 3.9 V or 4.3 V or 2.5 V) (register address x10h, bit<7:6>), when VBAT is still 150 mV (300 mV) below this setting (PPVSYSTEMLevel_extpp).
- VBAT+150 mV (300 mV) in follower mode versus VBAT voltage, when VBAT has reached the fixed programmable setting minus 150 mV (300 mV).
- 4.5 V (saturation value), if VBAT>4.45 V (4.2 V).
- The voltage drop between VSYSTEM and VBAT in follower mode is defined in a register at address @0Ah, bit4. 2 settings are available 150 mV (default) or 300 mV.

The software wakes up even if the battery is fully discharged or no battery is connected. In case of overload on VSYSTEM node versus input current limitation of the charger input, the PM2131 automatically controls in reverse the external FET to allow reverse current and avoid the collapse of charger input voltage.

The VSYSTEM generation startup is compliant with USB charging specifications versus input current limitation.

4.2.2 Empty battery and charging cycle

When the external power source is plugged, the external FET opens (FET is OFF) and the VSYSTEM voltage is generated. This allows the host to be booted and the system with weak battery to be supplied.

By default configuration, the charging automatically starts 1 s after the VSYSTEM generation startup. In this manner, the platform wakes up the host and updates charging settings through I^2C if needed, before that charging cycle starts up.

Internal charging mode

The empty battery is charged by the internal current source, hardware charging settings are applied. As soon as the host runs thanks to power path mode, host can update charging parameters. In internal charging mode, the maximum charging current available is 1.1 A. The external FET is in OFF mode to allow the disconnection between VSYSTEM and VBAT node.

Direct charging mode

When VBAT reaches the minimum voltage requested by the system to run properly (minimum battery voltage to guarantee system operation), the host can close the external FET (FET in ON mode). Then the host can increase the programmable charging current up to 4 A. The charging path goes through the external FET to this phase.

The transition between internal charging to direct charging mode can be allowed by:

- Host decision, writing to the address register @26h, bit0>. In this case, the host also controls both the end-of-charge and the aging mode.
- Autonomous decision based on VBAT voltage detection (VBATlow threshold level); in this case the end-of-charge, during direct charging, can be also managed internally. However, the transition to aging mode after end-of-charge is only performed by the software action.

4.2.3 4 A charging/supply applications

The PM2131 allows 4 A charging / supply applications. The VUSB and VPWR must be shorted externally. Either adapter or USB plug, the circuit proceeds with charger detection giving priority to USB path. Then, the host allows the high-current capability by enabling in parallel the VPWR path through register at address @01h, bit0 (single path register bit).

The second path can be even enabled during the internal charging mode. In this case, the charging current remains limited to 1.1 A, but the system current capability increases up to 4 A.

In case of applications with short between VUSB and VPWR, a specific software control enables the boost mode feature. One path (for example VPWIN path) must be stopped,

before enabling the boost mode on the USB path, to avoid getting a wrong detection of charger plug on VPWIN path.

4.2.4 Power path regulation mode after end-of-charge

Once end-of-charge is reached, the host stops the charging through I^2C, the external FET is opened by the PM2131.The PM2131 continues regulating VSYSTEM 150 mV (300 mV) over VBAT as long as the power needed by the system remains below the power delivered by the external power source (power path configuration (Vsys = VBAT +150 mV (300 mV) or aging mode). In case the end-of-charge is managed directly by the device (PM2131UHT, PM2131AHT), once the end-of-charge is reached, the charging is stopped automatically by the IC, waiting for the software goes to power path mode, writing the register @01h, bit2 to 0. The transition to power path mode after the charging is managed by software action in reg@01h, bit2 only.

When the power needed by the system exceeds the external power source capability, VSYSTEM voltage drops. Once VSYSTEM reaches VBAT, the external FET is automatically closed by the PM2131 so that battery compensates the remaining need of power. The FET switches on fast enough to absorb application peak current from the battery. (Reverse mode VSYSTEM = VBAT).

4.2.5 External power source connected as suspend mode

If the external power source is not used by the host to supply VSYSTEM even if connected, the registers must be written to address x14h or/and x18h bit[0], to suspend the power path operation, stopping the DC-DC converter. The PM2131 switches on the external FET in reverse mode. The battery supplies the application until host's decision updates.

4.2.6 Charger plug without battery

By default configuration when the automatic charging is active, once the charger is plugged, the circuit detects that any battery is present. An interruption is generated to inform the software that the battery is disconnected. During 10 minutes, VBAT balls are regulated as per default charge voltage setting and the system is regulated either as per VSYSTEM regulation setting or in follower mode versus VBAT charge voltage. After 10 minutes, to verify whether the battery is connected or not, the NOBAT detection algorithm runs again.

If the host recognizes a missing battery, the application processor decides whether to disable or keep enable the charging action. The charging function can be disabled by I^2C register access (register reg@01h bit<2> = 0) or by GPIO control, driving high ENN ball. An additional feature is available to reset hardware setting registers related to battery charging.

4.2.7 Applications with different charger circuits

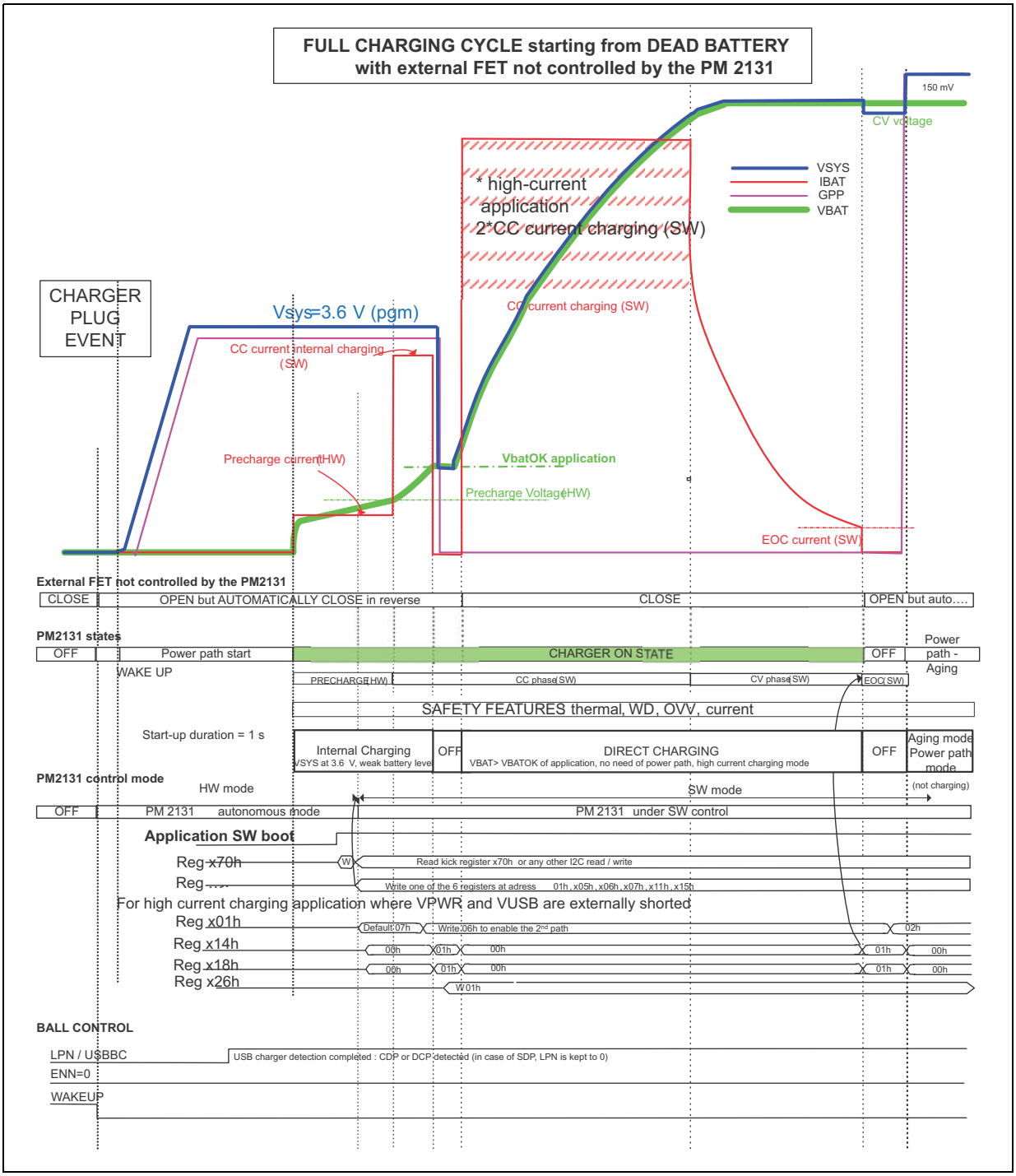
In case of applications with multiple charger circuits, the PM2131 is considered as an external charger versus analog base band charger. The analog base band must control the gate of the external FET. In this case the GPP ball must remain floating.

To avoid conflicts between I^2C command timing and external FET control, it is recommended the PM2131 to be suspended (register at address 14h and 18h) when:

- Switching from internal hardware charging mode to external FET charging mode
- Switching from external FET charging mode to aging mode

At system level, pay attention on battery or VSYSTEM overvoltage and battery overcurrent during transition phases.

Figure 5. Full charging cycle starting from dead battery



4.3 Hardware and software control

The PM2131 integrates a flexible control to meet different application requirements.

The PM2131 can operate in software control mode and control the charging parameters through I^2C.

The PM2131 can also operate in hardware control mode with predefined charging parameters and describe a full charging cycle without the software update. Aging mode transition after end-of-charge is however possible by software update only.

4.3.1 The PM2131 in hardware control mode

The PM2131 is in hardware control mode when the host (processor) does not control and defines the charging phase. This can happen in the following conditions:

- The host has not been booted yet
- The host does not start or stop I^2C access to the PM2131

In hardware control mode, when an external power source is plugged, battery charging starts with predefined battery charging settings.

The maximum duration of the hardware control mode is 20 minutes: if the host is not running within 20 minutes, the battery charging operation is stopped by the PM2131. If the software is running within 20 minutes, the PM2131 is in software controlled mode updated by specific I^2C register.

During the hardware control phase, the battery charging operation is performed by the CCCV algorithm, safety watchdogs for each active charging. If NTC is connected to the PM2131, the battery temperature can be also monitored during the hardware control mode and taken into account in the battery charging algorithm. During the hardware control mode the WAKEUP ball is at low level.

4.3.2 The PM2131 in software control mode

The PM2131 is in software control mode through I^2C access in one of the 6 register addresses: 01h, 05h, 06h, 07h, 11h, and 15h. The PM2131 charging parameters can be fixed by the host. The host manages the charging algorithm.

A security feature of software detection is available. It guarantees that host is still running and keeping the PM2131 under software control. To activate this kick watchdog feature, one I^2C write in reg@70h is mandatory, then any regular read or write I^2C access, in less than 32 s in any register, maintains the PM2131 under software control. If the host stops kicking the PM2131 or if the host collapses, while the feature of detection has been activated, the PM2131 goes back to hardware control mode, stops charging and resets most of its registers to hardware default values.

For safe software control, the detection feature must be activated before than any other register.

When the external power source is unplugged, the software is informed by interrupt or by the WAKEUP ball. If LPN ball is driven high, after the external power source is unplugged, the host must stop kicking regularly the PM2131 in order to correctly reset the charging registers. If LPN ball is driven low after the external power source is unplugged, the PM2131 automatically leaves the software control mode and switches back to hardware mode with default register settings.

5 Device interface

This section describes the PM2131 device interfaces.

5.1 Control pins

5.1.1 ENN input pin

The ENN pin enables the PM2131 battery charging operation. ENN is active at low level.

If ENN is driven to high level while the external FET is open (OFF mode), during VSYSTEM regulation mode, the battery charging operation through the internal current source is disabled.

When ENN is driven to high level and the external FET is closed (ON direct charging mode), the battery charging operation through the external MOSFET is disabled, the SMPS is disabled, equivalent to suspend mode.

When ENN is driven to high level, all the other functions (external power source detection, wake-up information, interrupt generation) are still active.

Another option to disable the charging feature is through I^2C register at address 01h bit2. Priority is always given to disabling action.

5.1.2 WAKEUP output pin

The WAKEUP output pin is open drain, active low. It informs the system that the PM2131 input is connected to a valid external power source.

An external power source is considered valid if its voltage is below a programmable OVV (overvoltage) threshold and on VPWR path when the charger plug is not a sine wave charger. WAKEUP information is valid even if battery charging operation is stopped.

For USB plug only: WAKEUP output is driven low level few μs after the plug, the generation of VSYSTEM voltage starts around 230 ms after the plug.

For VPWR plug only: WAKEUP output is forced low level around 120 ms after the plug, time corresponding to pirate charger detection, the generation of VSYSTEM voltage starts around 330 ms after the plug.

For applications with USB and VPWR balls shorted: WAKEUP output is driven low level few μs after the plug, the generation of VSYSTEM voltage starts around 230 ms after the plug.

5.1.3 IRQ output pin

The interrupt request (IRQ) ball pin informs the system when an event from the interrupt register list occurs. This pin is open drain, active low. All interrupt registers have interrupt register masks which can inactivate specific interrupt. The IRQ pin is reset when the interrupt flagged registers have been read.

5.1.4 LPN/USBBC pin

The LPN/USBBC pin driven to low level allows the PM2131 to be switched in low power mode after 1 s when the external power source is not connected. The current consumption

is optimized, the I²C communication with the PM2131 is no more accessible and all registers are reset to their default values.

As soon as an the external power source is connected, the PM2131 is active and I²C communication is alive. The LPN/USBBC pin controls the input current limitation. If a charger is plugged and the LPN/USBBC pin is at high level, the input current limitation is set to a higher current than the default one. There are four different predefined settings available for input current limitation set by LPN/USBBC high level: 650 mA, 725 mA, 1300 mA and 2170 mA. If the LPN/USBBC pin is at low level, the predefined value is used for the USB or VPWIN charger input current limitation as long as the register is updated by the software.

When the external power sources are unplugged, the host must put LPN pin high to communicate, through I^2C with the PM2131 and receive I^2C “acknowledge” from the PM2131. If LPN is kept low, 1 s after the charger unplug, the PM2131 goes to low power mode.

5.2 I²C interface information

The PM2131 can be controlled by I²C communication. The I²C interface offers flexibility to the battery charging operation, enabling/disabling/programming most functions and registers. I²C is also used to read the interrupt registers. The I²C interface is alive when an external power source is connected or when the PM2131 is not in low power mode (this means that LPN pin is driven to high level while no external power source is plugged).

The I²C bus ™ is configured as a slave serial interface compatible with the I²C register, built with a data line (SDA) and a clock line (SCL):

SCL: input clock used to shift the data

SDA: input/output bidirectional data transfer line

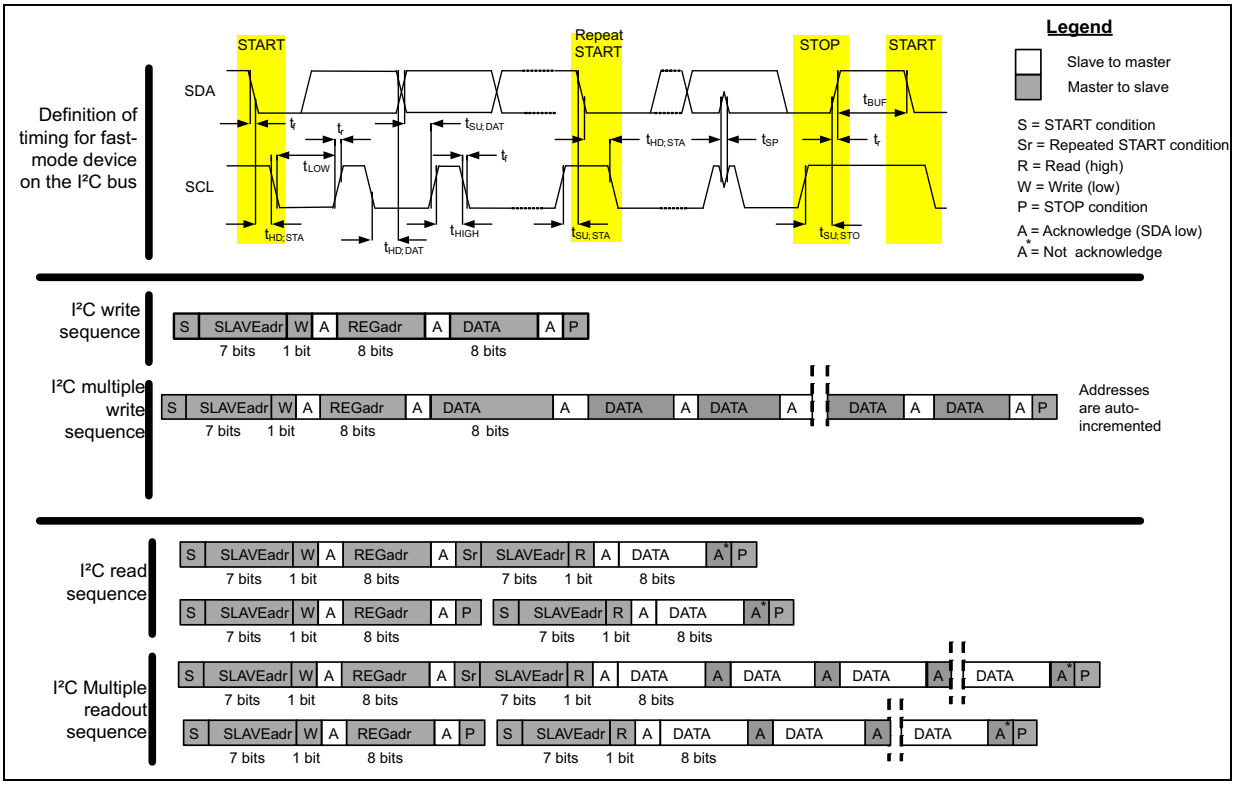
The PM2131 device works as a slave and supports the following data transfer mode: standard mode (100 kbit/s) and fast mode (400 kbit/s) as defined by the $I^2C\_bus^{TM}$ specification version 2.1 developed by Philips Semiconductor [*1*]. The PM2131 can also support an extended fast mode up to 3.4 Mbit/s in write mode for dedicated links.

The PM2131 device supports 7-bit address, plus one bit dedicated to write (0) or read (1) mode. The master initiates data transfer by generating a start condition. The start condition is when a transition from high to low occurs on SDA line while SCL is high. The master then generates the SCL pulses and transmits the 7-bit address for the device IDD plus 1 bit defining read/write operation.

The ID device slave address coded on 7 bits is 2C(h)

The device with a matching address only generates an acknowledge by pulling the SDA line low during the entire period of the 9^{th} SCL cycle. The SDA data is shifted MSB first. The master device sends 8 bits onto SDA corresponding to the register address followed by an acknowledge and 8-bit data field corresponding to the register content, which might be followed or not by another acknowledge. To signal the end of the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high. This releases the bus and stops the communication link to the addressed slave device.

Figure 6. I²C



Consecutive (page) read-out starts from the master by sending acknowledge instead of “not acknowledge” after the receipt of data. The I²C register bank is then incremented to the address pointer of the next I²C address and sends the data to the master. This procedure is repeated until the master sends a “not acknowledge” after the receipt of data.

6 Functional description

6.1 The PM2131 operation

6.1.1 No charger plug

When any external power source is plugged, the VSYSTEM voltage is directly supplied by the battery through the external FET. This is called reverse mode operation.

The control of the external FET in ON condition is managed by an internal circuitry.

The internal current source connected between the VSYSTEM and VBAT, used as internal charging circuitry when the FET is open (OFF mode), is in the OFF mode.

6.1.2 External power source plug

When the external power source is plugged, the PM2131 operates differently depending on the external FET status.

- If FET is open (OFF mode) and charging is enabled: this is called hardware control mode (default configuration):
  - VSYSTEM is regulated from the external power source to a predefined setting (3.6 V, 3.9 V, 4.3 V or 2.5 V) or is regulated in follower mode versus VBAT: this is called power path mode with internal current source charging.
  - The battery is charged using the internal charging current circuitry with predefined parameters until the boot. Charging parameters are predefined by the hardware settings.
  - After the boot operation, the software can change the charging parameters to speed up the charging.
  - The CC current can be increased by the software up to 1.1 A. However, it can be limited by the internal power dissipation related to the drop between the VSYSTEM and VBAT.
  - The end-of-charge is managed by the PM2131.
- If FET is closed (ON mode) and charging is enabled: usually under software control mode:
  - VSYSTEM is at same voltage as battery, charging path is using the external MOSFET, charging current can be increased up to 4 A.
  - When charging cycle is concluded (managed by the host), the external FET is put in OFF mode (through I^2C) and VSYSTEM keeps on being regulated by the external power source at VBAT+150 mV (or 300 mV). This allows the system, without sinking current from battery, to be supplied. If VSYSTEM load exceeds the

capability of external power source, the external FET is automatically turned ON (any I^2C control is needed) allowing battery to provide the extra current.

  - The end-of-charge is managed by the host only.
  - The register at address @26h bit0 is used to close the external FET and proceeds to high-current charging.

- If FET is open (OFF mode) and charging is disabled:
  - VSYSTEM is regulated by the external power source to predefined settings (3.6 V, 3.9 V, 4.3 V or 2.5 V) or is regulated in follower mode versus VBAT. This is called power path mode or aging mode if the battery is fully charged.
  - If the load on VSYSTEM node becomes higher than what the external power source provides, the PM2131 automatically goes to reverse mode, allowing the external FET to provide current from the battery line.

The transition from the internal charging source to the direct charging path is driven by the host to the write register @26h (FET ON control). This transition can only happen when VBAT reaches the minimum voltage requested by the system to run the application properly, this is a software decision.

When the external power source is plugged and the charging is allowed, the external FET is ON if register@26h is set to 1.

6.1.3 High external power source case

For applications with high external power source connector, USB balls and VPWR balls must be shorted. At the external power source plug, only one path is enabled, the USB path. The PM2131 waits for host's request to enable the VPWR path, delivering the maximum current for the charging or for the application load. The enable of the second path comes through I^2C request from register address @01h bit0.

6.2 Battery charging modes

6.2.1 Trickle mode

The trickle (pre-charge) mode is enabled when the battery voltage is below the trickle threshold voltage (programmable value). Trickle charging is handled by integrated current source. During this trickle mode, the battery is charged with the constant low predefined pre-charge current. The external MOSFET is automatically in OFF condition.

The pre-charge or trickle watchdog is set when the phase starts up. This safety watchdog is used to detect short-circuit on the battery.

The trickle mode runs when the battery is very low. The trickle mode is managed without any software update.

6.2.2 Constant current mode (CC mode or fast charge mode)

In fast charge mode, the fast charge current is defined by the dedicated CC mode current control register.

This register is set to a predefined value. The software can change the value of the current according to the charge profile.

In hardware control mode, a safety timer is active. In software control mode, the software must update the watchdog.

When the internal charging path is used:

- External FET is OFF.
- Integrated current source is used for the charging, CC charging current is programmable from 100 mA up to 1.1 A (register @05h [bit<3:0>]). The VSYSTEM voltage is generated at 3.6 V, 3.9 V, 4.3 V, 2.5 V or in follower mode versus VBAT voltage.
- The CC reduced current mode reduces the CC current when VBAT is low to provide some current to the application and avoid the rise of the power dissipation. This feature is disabled by default (see reg@0Ah, bit2-1).

When an external MOSFET charging path is used:

- External FET is ON.
- DC-DC charger is used for charging, CC charging current can be increased up to 2 A in single path mode (reg@01h, bit0=1) or 4 A in dual path mode (reg@01h, bit0=0).

6.2.3 Constant voltage mode (CV mode)

The CV mode is available only when the direct charging path is used:

- External FET is ON.
- DC-DC charger is used for charging.

6.2.3.1 Description

In the constant voltage mode (CV), the PM2131 output voltage is regulated according to the float voltage (programmable value) with a maximum accuracy of 1%.

This mode can run in autonomous or in software control mode. The CV mode terminates when the end-of-charge current is detected or when the watchdog timer elapses.

In software control mode, the watchdog timer can be deactivated. Further to the PM2131AST, the end-of-charge must be detected by the software.

While, concerning the PM2131AHT and the PM2131UHT, the end-of-charge is automatically detected.

The PM2131AHT/PM2131UHT send an interruption of ITbattFull to inform the software that the CV phase is complete. The software switches to power path mode by updating reg@01h, bit2=0.

6.2.3.2 CV mode and battery overshoot protection

A specific feature, enabled by register at address (x28h, bit0), is present in the PM2131 to avoid the overshoot voltage on battery line as consequence of a huge load transient (for example like a GSM burst load variation). This feature is an enhancement of the PSE requirement (JISC8714). When a load transient (from high to low value) occurs, the battery line can present an overshoot voltage versus the float voltage that is set for CV mode. Battery manufacturers recommend this overshoot to be avoided for Li-Ion battery safety.

A specific algorithm is implemented to keep the DC-DC charger path in the operating mode so to have very fast reaction to load transient. This allows, most of cases, no overshoot on battery line (also when charging current is set at maximum value) and no dependence on battery parameters (like intrinsic ESR).

6.2.3.3 End-of-charge feature

The end-of-charge current threshold is directly controlled by the software, especially when register at address (x26h, bit0) is set to 1. The PM2131 sends an interrupt to the software when the charging is going to CV phase.

Then the host must control the current flowing to the battery and detect when the end-of-charge is reached by gas gauge for example. The software stops the charger by I^2C register access, setting to 1 register at address (x01h, bit2).

6.2.4 Autonomous charging cycle

The PM2131 describes a full charging cycle with or without a minimum software support. The PM2131 manages a complete charging cycle using internal hardware settings to describe: the trickle phase, the constant current phase, the external FET, the constant voltage phase and the end-of-charge. In this specific case, the register at address (x26h, bit0) must be always kept to 0. The hardware watchdog secures the charging operation.

Note: In this case, the transition from internal charging source to direct charging source with external FET is performed thanks to an internal threshold detection (VBATLOWlevel) sensing the battery voltage node.This level is programmed by register at address @23h, 0-4-bit.

Warning: A specific order code is mandatory for this configuration (the PM2131AHT)

6.3 Input power optimization

6.3.1 Digital hardware input current optimization loop

Further to digital dichotomy algorithm, this feature automatically finds the maximum input current preventing the external voltage source from dropping under VALID threshold level or the SMPS in 100% PWM.

This loop is not recommended for those applications where VPWR-VSYSTEM or VUSB-VSYSTEM could be lower than 700 mV mainly due to high-current flows and parasitic resistive drops.

The VALID threshold level is at 4.75 V (4.4 V min.).

This feature can be activated through I^2C register at address x13h and x17h.

6.3.2 Analog hardware input voltage optimization loop

This feature regulates the input voltage at a programmed selected value when the USB or VPWR adapter is in current limitation and decreases the charging current to maximize the power from the USB or AC adapter.

The input charger voltage VUSB and VPWR drop down four different values 4.5 V (default), 4.6 V, 4.7 V, 4.8 V.

This feature can be activated by I^2C register at address x13h and x17h.

6.4 Input charger protection

The PM2131 has an integrated input charger overvoltage protection. The maximum voltage is programmable to run the PM2131 battery charging. The PM2131 sustains in OFF mode if the input supply is higher than maximum charger voltage. Maximum charger voltage must not be higher than 20 V. The PM2131 also integrates a reverse down to -2 V input voltage polarity protection.

6.5 USB compliance for charging operation

The PM2131 is compliant with USB battery charging specification 1.2 and USB standard 2.0.

When USB is plugged, the input current sink is limited to a default maximum setting= 500 mA until the host has completed the USB charger detection.

LPN/USBBC ball allows the input current limitation to be increased to higher values.

For high charging applications, the host enables the second path after charging recognition, having USB path and VPWR working in parallel.

6.6 BOOST mode and OTG mode

When an input path is not used for charging or VSYSTEM regulation, the boost mode can deliver power onto input connectors. The register at address (x25h) enables the boost mode on VUSB input, and also defines the boost voltage level among 4.5 V, 5 V, 7 V and 11 V settings. The commonly named OTG mode is enabled by register at address (x25h), bit0 at x01h.

The boost mode on VPWR path is enabled by register at address @05h bit4.

For those applications with VPWIN and USB balls shorted, the boost mode is enabled by reg@25h, bit0, by stopping any activity from VPWIN path (reg@18h, bit0 must be set to 1). If the boost mode is enabled by reg@05h, bit 4, any activity from VUSB path (reg@14h, bit0 must be set to 1) must be stopped.

In case of overcurrent load during the boost mode operation, an interrupt is generated to inform the host that the PM2131 cannot regulate correctly the voltage in boost mode anymore.

For safety reasons, the PM2131 could collapse automatically the boost mode in case of severe overload. An interruption is generated to inform the software that the boost mode has been disabled. The soft reads this interruption register before re-enabling the boost mode register.

The PM2131 detects 0% PWM activity of the SMPS during boost mode operation; this information is provided to the host with an interrupt. This feature detects the role swapping between device A and device B for example.

6.7 Internal regulator and internal clock

The PM2131 has an internal supply decoupled by the Cvis capacitor connected to the CVIS pin.

The PM2131 has a voltage reference decoupled by a capacitor connected to the VREF pin. This voltage is used internally for detection and monitoring comparators. The decoupling capacitor on VREF must be put as closer as possible to the die.

Internal oscillator is used for state machine, timers and to deliver clock to the DC-DC charger path.

6.8 Hardware/software control and safety watchdogs

6.8.1 Software control and software kick watchdog

The software kick watchdog informs the PM2131 that the software is alive and is controlling it.

To enable the software detection feature, the host writes through I²C WDCounter register at @70h.

The host regularly resets this timer every 32 s or less. Read or write WDCounter register at @70h through I²C must be performed or simple read one I²C register.

If software kick watchdog elapses, the PM2131 resets its parameters to their default value and goes back to hardware control mode.

To be in software control mode, the host must write in one of the following six register addresses (01h, 05h, 06h, 07h, 11h, and 15h) in addition or not to the software kick watchdog feature.

The software kick watchdog feature must be enabled and then software control mode actions can proceed.

When the AC adapter is unplugged, the host must stop toggling the software kick watchdog, in order to correctly reset the charging registers and control correctly the next charging phase without remaining information from the previous charging cycle.

6.8.2 Software charging and auto timeout watchdog

This watchdog is controlled by ChWDautotimeout register at @04h.

When an external power source is plugged and the auto timeout watchdog is enabled, the PM2131 starts the charging in an autonomous way, using its own hardware charging parameters during 20 minutes maximum.

Within these 20 minutes, host writes to one of the following six register addresses (01h, 05h, 06h, 07h, 11h, and 15h).

Otherwise the PM2131 automatically stops the charging and sends an interruption.

When the PM2131 is used in fully autonomous charging, the auto timeout watchdog is disabled.

6.8.3 Autonomous charging phase watchdog

Dedicated watchdog registers are used during the charging phases (trickle, CC and CV). If the predefined time elapses, the PM2131 stops charging, goes to the error state and sends an interrupt. The LED indicator is also stopped. Those dedicated watchdog registers are defined by hardware settings and can be updated through I^2C.

6.9 The PM2131 startup and charging sequence timing diagram

Figure 7 illustrates an example of a start-up sequence on a dead battery.

About 100 ms after the external power source has been plugged, the WAKEUP signal is available and the PM2131 regulates VSYSTEM node according to predefined settings 3.6 V, 3.9 V, 4.3 V or 2.5 V. It allows the application to be powered up.

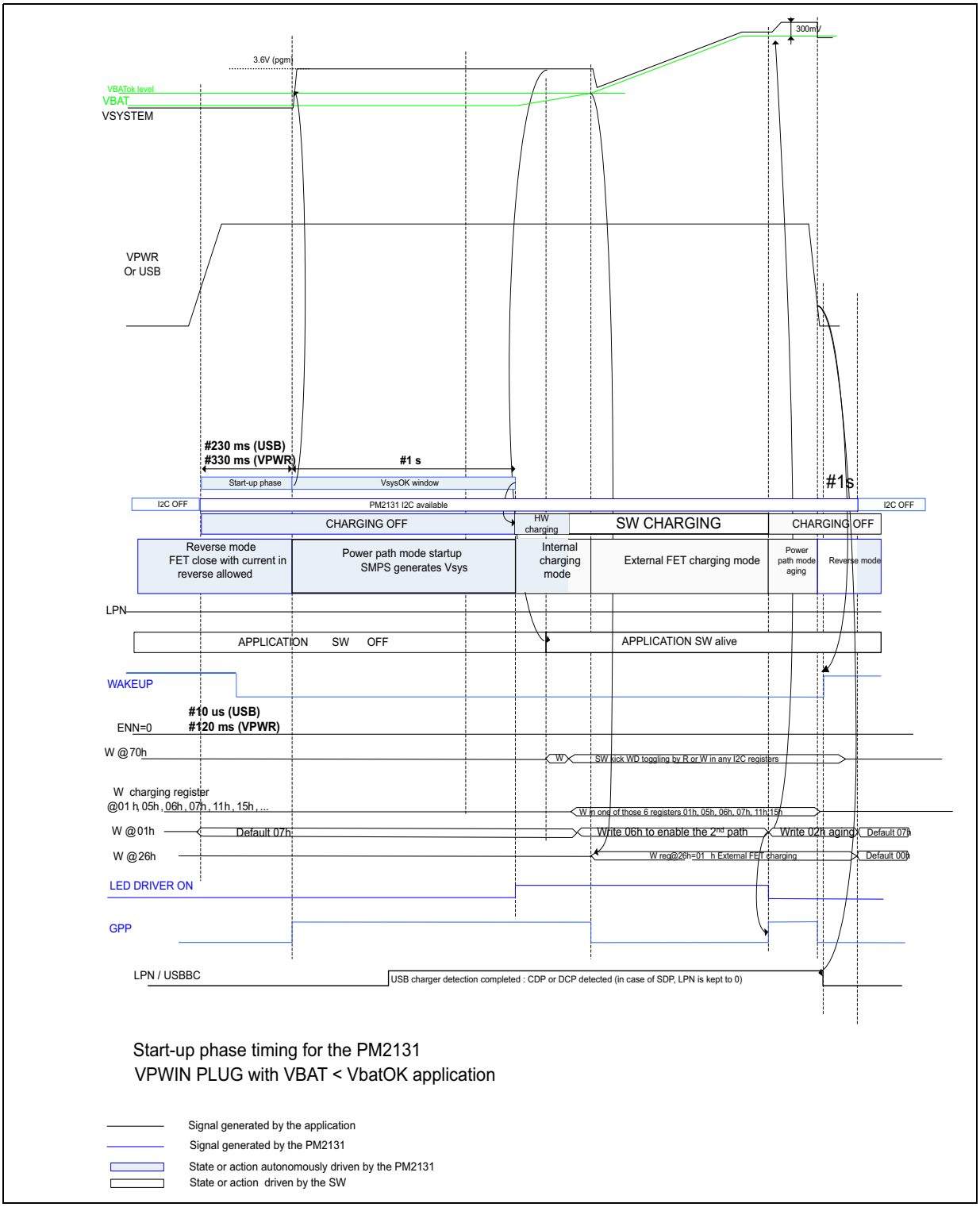
The charging starts about 1 s later, probably directly under software control. Charging parameters can be updated by the software.

The charging is performed through the internal charging mode till VBAT reaches VBATok of the application. Then the host proceeds to fast charging operation or direct charging. Charging current can be up to 4 A when singlePath bit is set to 1. The external FET is closed.

The host manages the end-of-charge by stopping through I^2C the charging. The PM2131 goes to power path mode, regulating VSYSTEM in follower mode +150 mV (+300 mV) over VBAT without charging (external FET is OFF).

On external power source unplugged, the PM2131 goes to low power mode and any I^2C communication is available with the PM2131. The external FET is driven to reverse mode allowing current flow from battery.

Figure 7. Example of start-up sequence on a dead battery



Start-up phase timing for the PM2131
VPWIN PLUG with VBAT < VbatOK application

Signal generated by the application
Signal generated by the PM2131
State or action autonomously driven by the PM2131
State or action driven by the SW

6.10 Dedicate interrupt management

The PM2131 integrates a dedicated open drain output (active low) to inform the system that an event has occurred. This ball provides the system with the information about the external power source plug/unplug, battery charging phases, the battery temperature monitoring, safety watchdogs and other safety features charging or to request specific actions from the host.

Interrupt register informs the host about the source or nature of the interrupt through I²C. These flagged registers are reset after the read action.

There are three sets of interrupt registers:

- Interrupt latches are only read and are located on BASE ADDRESS + 0. Latches are set by an interrupt event and reset by I^2C.
- Interrupt mask registers are read/write and are located on BASE ADDRESS + 10h. The 0 value means that interrupt is generated, 1 = interrupt is masked.
- Interrupt sources are only read and are located on BASE ADDRESS + 20h. Sources reflect the current state of signals causing interrupts.

6.11 Current and voltage monitoring

6.11.1 Current monitoring

The current provided to the VSYSTEM is always monitored by the PM2131.

6.11.2 Voltage monitoring

The PM2131 monitors different voltages related to the battery and the charger.

- Battery pre-charge voltage monitoring: programmable threshold from a pre-charge mode to the fast charge mode (CC mode).
- Battery CV mode voltage monitoring: programmable threshold from the fast charge mode (CC mode) to the CV mode.
- Battery resume voltage monitoring: in autonomous mode, the detection of this threshold allows the battery charging to restart if the external power source is still plugged. In software control mode this feature is performed by the software.
- Input overvoltage: this voltage detection forces the battery charging in OFF mode as the PM2131 input voltage is too high. The battery charging can restart if the PM2131 input voltage goes back to the operating range.
- Battery low voltage detection monitoring: programmable threshold informs the host about the low battery voltage level.
- VSYSTEM overvoltage monitoring: this voltage detection forces the DC-DC in OFF mode as it indicates some misbehavior. An interrupt is generated and battery charging can restart only if the external power source re-plug event is detected.

6.12 Temperature monitoring

6.12.1 Battery temperature monitoring

The battery temperature monitoring feature is performed using voltage detection on NTC resistor connected to the PM2131. In this case, the PM2131 allows the battery charging only when battery temperature is within the programmed range.

The battery temperature monitoring can be disabled through I^2C to allow software to manage it.

When the battery temperature feature is enabled, the battery charger performs the battery temperature measurement through the NTC resistor only when the external power source is plugged. The NTC resistor values are defined by the predefined register values.

The low temperature and high temperature limits are programmable.

When the NTC resistor is not connected or the function is disabled (by software or no charger plug), the ball NTC is internally grounded.

6.12.2 Device internal temperature monitoring

The die temperature is also monitored. If the die temperature exceeds the warning temperature threshold, the system is informed by the PM2131 interrupt.

If the die temperature exceeds the shutdown threshold temperature, the PM2131 automatically stops the charge and informs the host through an interrupt. When the temperature recovers, the charging starts again.

6.13 Resume feature

The resume feature allows the battery charging to be restarted only when the below conditions are verified:

- Battery charging has been concluded in autonomous mode by the PM2131. This means that register at address 26h, bit0 is kept to 0, and register at address 01h, bit2 is still at 1.
- External power source remains plugged after battery charging is over.
- Battery voltage is decreasing down the VBATresume threshold.

The battery resume threshold is programmable and this feature can be disabled by I^2C. VBATresume threshold must be set to 300 mV below the CV battery threshold.

In any case, the software can start the charge even if the battery voltage is above this threshold by writing the charging enable through I^2C.

If the PM2131 is under software control, the resume feature is exclusively performed by the software decision.

6.14 Register reset

The reset of the PM2131 leads to get all predefined parameters set as default parameters. In order to use the enhanced safety feature, the reset is defined at different levels:

- Reset after external power source disconnection.

  This reset occurs in standalone and in software controlled mode. The following registers are reset on the external power source unplug (address 11h,13h,15h,17h,29h).
- Reset after that the PM2131 has not received the software kick watchdog.

  The PM2131 goes to the hardware control mode. Below registers are reset to default value addresses (1h,5h,7h,9h,10h,11h,13h,14h, 15h,17h, 18h, 26h, 28h).
- Reset linked to battery disconnection when the PM2131 has detected that the battery is not present.

  Below registers are reset in this case (address 02h, 03h, 06h, 08h).
- Reset in low power mode: LPN pin at low level and any external power source is plugged. All registers are reset to the default values and the circuit goes to low power mode.

6.15 The LED indicator

The LED indicator feature indicates through a light emission diode (LED) when the PM2131 battery charging is active. It is built thanks to a current source internally supplied by battery voltage or by an internal pre-regulated power source voltage.

The LED indicator is OFF in the following conditions:

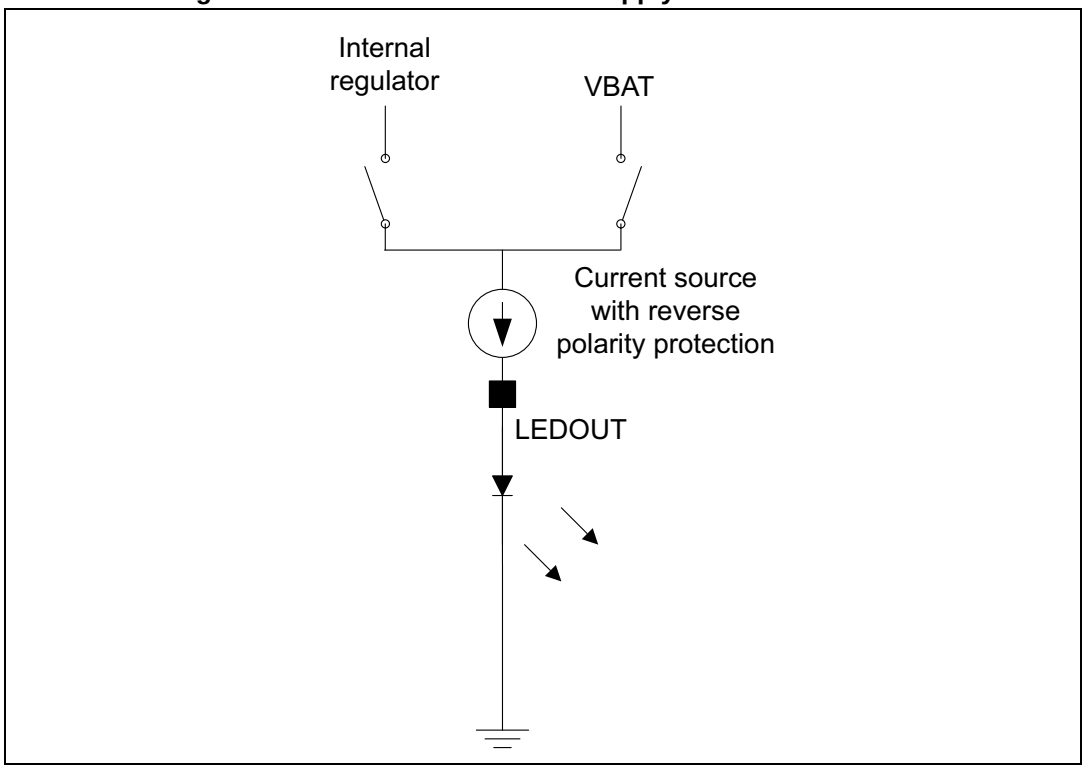
- The PM2131 battery charging is OFF (for any reason).
- When the software writes to the correspondent register to disable this feature.

The LED indicator current source is designed to have high impedance on the LED pin when it is in OFF mode. In this manner, the same LED is shared with other products inside the application.

The LED current is programmed by software through I^2C. The default value is 2.5 mA. Additional values are 1 mA, 5 mA, 10 mA. The LED charging current is programmable.

The LED indicator feature is always enabled when the PM2131 works in autonomous mode and in the hardware control mode.

Figure 8. PM2131 schematic and supply for LED indicators



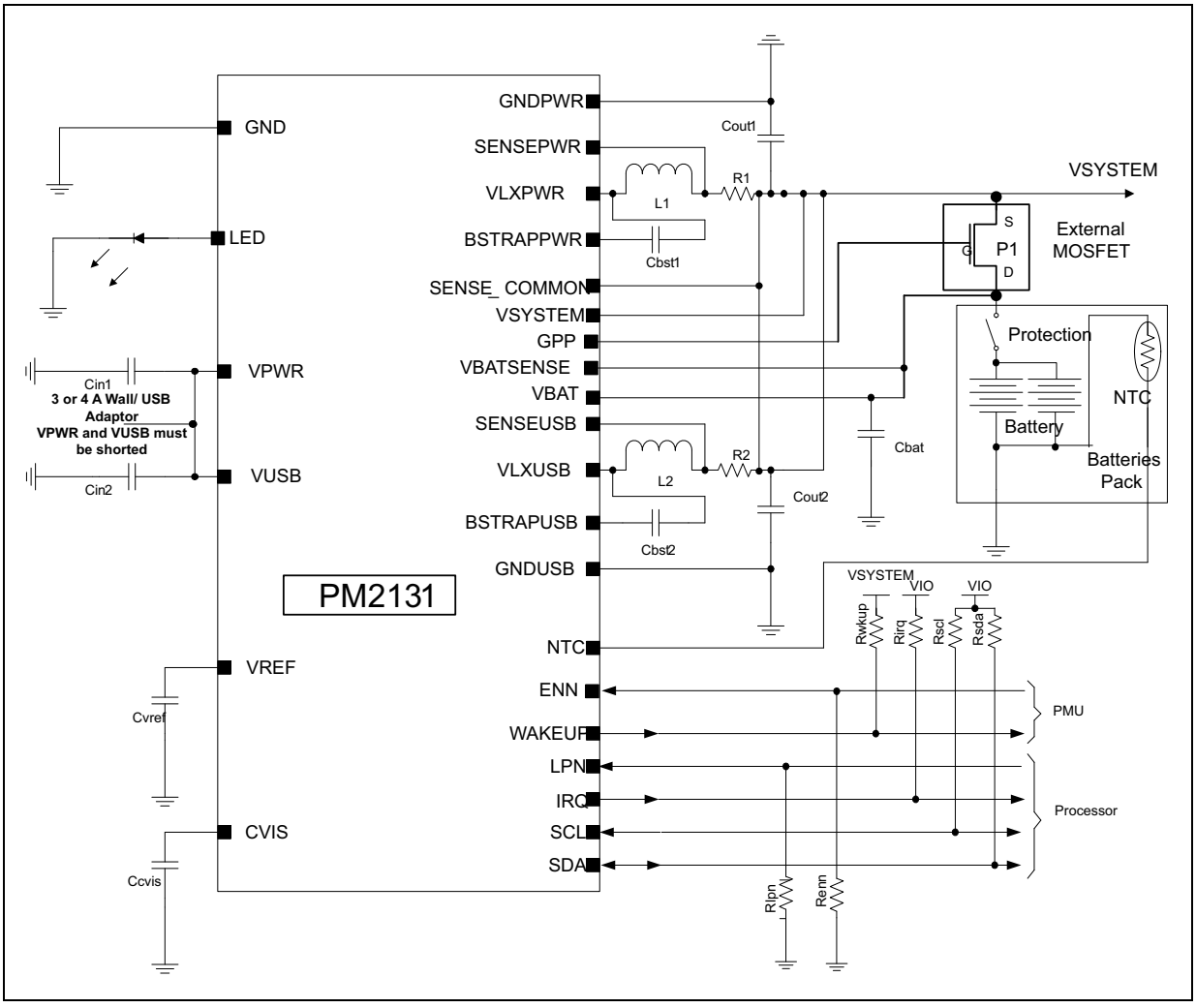
7 Application hints

This section presents the application hints and describes the schematic and the minimum components to properly run the application.

7.1 The PM2131 typical application

Figure 9 shows the PM2131 typical application: the battery charging.

Figure 9. The PM2131 battery charger schematic diagram



7.2 Typical component list

Table 11 provides the list of the required components to run the application.

Table 11. Typical component list

Component name	Value	Unit	Comments
L1	1	µH	Coil for DC-DC charger Saturation current Isat > 3.2 A with R1 = 47 mΩ
L2	1	µH	Coil for DC-DC charger Saturation current Isat > 3.2 A
R1	68	mΩ	Power dissipation minimum P > 150 mW Resistance accuracy is 1% To limit charging current to 1.5 A in VPWR path
	47	mΩ	Power dissipation minimum P > 150 mW Resistance accuracy is 1% To limit charging current to 2.0 A in VPWR path
R2	68	mΩ	Power dissipation minimum P > 150 mW Resistance accuracy is 1% To limit charging current to 1.5 A in USB path
	47	mΩ	Power dissipation minimum P > 150 mW Resistance accuracy is 1% To limit charging current to 2.0 A in USB path (with 145 mA max. input current at charger plug)
Cin1 and Cin2	4.7	µF	Decoupling VPWR and VUSB, minimum voltage is 16 V, low equivalent series resistance (ESR)
Cbst1 and Cbst2	10	nF	Boost capacitor for high-side MOS gate driving, minimum voltage 16 V
Cout1 and Cout2	22	µF	DC-DC battery charger capacitor, minimum voltage 6.3 V
Cbat	4.7	µF	Battery voltage decoupling capacitor
Cbatsense	22 (optional)	µF	Optional: anti-overshoot feature minimizes the overshoot on VBAT during load/transient
Cvis	1	µF	Cvis decoupling capacitor, minimum voltage 6.3 V
Cvref	1	µF	Cvref decoupling capacitor, minimum voltage 6.3 V
NTC	10 to 100	kΩ	See the programmed value
LED	/	/	/
Rsda	10	kΩ	Value must be taken as typical value
Rscl	10	kΩ	Value must be taken as typical value
Rirqt	10	kΩ	Value must be taken as typical value
Renn	10	kΩ	Value must be taken as typical value
Rlpn	10	kΩ	Value must be taken as typical value
Rwkup	10	kΩ	Value must be taken as typical value
P1			External MOSFET (FDZ371PZ)

7.3 FMEA protection feature

The PM2131 detects external component connections, this is called FMEA protection detection. R1 and R2 presence detection and VBATSENSE feedback connections are checked. In case of failure, DC-DC is stopped.

Warning: This feature must be disabled after plugging the charger, just before enabling the second charging path for high-current charging (register address x28h, bit4 set to 1).

8 Register description

8.1 Battery charger registers

All current values are provided with R1 and R2 = 47 mΩ. When R1 and R2 values are different, the current values must be multiplied by a ratio equal to (R1 / 47 mΩ) or (R2 / 47 mΩ) respectively.

Specific ordering codes are proposed to select some “predefined parameters” to fit customer application needs.

8.1.1 Battery charger control register 1, address = 00h

7	6	5	4	3	2	1	0
RESERVED							ChResume
R							R/W/Autoreset

Address: 00h

Type: R/W/autoreset

Reset: Watchdog expiration or low power mode

Description:

[7:1] RESERVED

[0] ChResume: forces resume of charging after reaching EOC – restarts the charge even if battery is above the resume voltage threshold

0: nothing happens

1: resume charging - it is automatically reset when the charger starts charging

8.1.2 Battery charger control register 2, address = 01h

7	6	5	4	3	2	1	0
RESERVED					ChargerEna	chAutoresume	Singlepath
R					R/W	R/W	R/W

Address: 01h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:3} RESERVED

[2] ChargerEna: charger is enabled (predefined parameters)
0: charging is disabled
1: charging is enabled (PM2131AST, PM2131UHT, PM2131AHT)

[1] ChAutoresume: charger control may restart charging automatically when VBAT drops below Vresume threshold
0: charger auto-resume is disabled
1: charger auto-resume is enabled (default)

[0] Singlepath: to enable the second path in parallel with the first one (predefined parameters) – it is mandatory to disable FMEA protection bit reg@28h, bit4
0: both paths are enabled in parallel (PM2131AHT)
1: only 1 path is enabled according to PPVPWRpriority bit (register at address @10h and OTP) (PM2131AST, PM2131UHT)

8.1.3 Battery charger control register 3(watchdog control), address = 02h

7	6	5	4	3	2	1	0
RESERVED		ChWDccphase			ChWDcccvphase		
R		R/W			R/W		

Address: 02h

Type: R/W

Reset: Battery disconnection or low power mode

Description:

[7:6] RESERVED

[5:3] ChWDccphase: fast charge watchdog timer (battery charger constant current -CC mode) (OFF, 60 min., 120 min. and 240 min. are predefined parameters)

000 OFF

001 5 min.

010 10 min.

011 30 min.

100 60 min.

101 120 min.

110 240 min. (PM2131AST, PM2131AHT, PM2131UHT)

111 360 min.

[2:0] ChWDcvphase: constant voltage charger watchdog timer (OFF, 60 min., 120 min. and 240 min. are predefined parameters)

000 OFF

001: 5 min.

010: 10 min.

011: 30 min.

100: 60 min.

101: 120 min.

110: 240 min. (PM2131AST, PM2131AHT, PM2131UHT)

111: 360 min.

8.1.4 Battery charger control register 4 (watchdog control), address = 03h

7	6	5	4	3	2	1	0
RESERVED					ChWDprechphase		
R					R/W		

Address: 03h

Type: R/W

Reset: Battery disconnection or low power mode

Description:

[7:3] RESERVED

[2:0] ChWDprechphase: battery pre-charge timeout (OFF, 30 min. are predefined parameters)
000 OFF (PM2131UHT, PM2131AHT)
001: 1 min.
010: 5 min.
011: 10 min.
100: 30 min. (PM2131AST)
101: 60 min.
110: 120 min.
111: 240 min.

8.1.5 Battery charger control register 5 (watchdog control), address = 04h

7	6	5	4	3	2	1	0
RESERVED							ChWDautotimeout
R							R/W

Address: 04h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:1] RESERVED

[0] ChWDautotimeout: a watchdog, which is not reset within 20 min., stops the charging. To disable the watchdog specific, I^2C registers have to be in software control mode (predefined parameters)
0: no timeout (PM2131AHT, PM2131UHT)
1: timeout is 20 min. (PM2131AST)

8.1.6 Battery charger control register 6 (current control), address = 05h

7	6	5	4	3	2	1	0
ChEoccurrentLevel		RESERVED	VPWRboostena	ChCCcurrentLevel			
R/W		R	R/W	R/W			

Address: 05h

Type: R/W

Reset: Software watchdog expiration or low power mode or battery disconnection

Description:

[7:6] ChEoccurrentLevel: current level detects end-of-charge condition (215 mA and 580 mA are predefined parameters) with R1 or R2 = 47 mΩ
00: 145 mA
01: 215 mA (PM2131UHT)
10: 435 mA
11: 580 mA (PM2131AST, PM2131AHT)

[5] RESERVED

[4] VPWRboostena: enables boost on VPWR (predefined parameters)
0: boost is disabled (PM2131AST, PM2131AHT, PM2131UHT)
1: boost is enabled

[3:0] ChCCcurrentLevel: constant current programming (predefined parameters) with R1 or R2 = 47 mΩ

when internal charging mode (register at address @26h, bit0=0 or VBAT<VBATlow level):

0000: 100 mA
0001: 100 mA
0010: 200 mA
0011: 300 mA
0100: 400 mA
0101: 500 mA (PM2131AST)
0110: 600 mA
0111: 700 mA
1000: 800 mA
1001: 900 mA
1010: 1000 mA
1011: 1100 mA
1100: 1100 mA
1101: 1100 mA
1110: 1100 mA
1111: 1100 mA

when direct charging mode (register at address @26h, bit0=1 or VBAT > VBATlow level & Singlepath =1(reg@01h, bit0=1)

0000: 145 mA
0001: 145 mA
0010: 290 mA
0011: 435 mA
0100: 580 mA
0101: 725 mA
0110: 868 mA
0111: 1010 mA
1000: 1150 mA
1001: 1360 mA
1010: 1440 mA (PM2131UHT)
1011: 590 mA
1100: 1736 mA
1101: 1880 mA
1110: 2025 mA
1111: 2170 mA

[3:0] ChCCcurrentLevel (continued)

when direct charging mode (register at address @26h, bit0=1 or VBAT>VBATlow level) and Singlepath =0 (reg@01h, bit0=0)

0000: 290 mA 0001: 290 mA
0010: 580 mA 0011: 870 mA
0100: 1160 mA 0101: 1450 mA
0110: 1736 mA 0111: 2020 mA
1000: 2300 mA 1001: 2720 mA
1010: 2880 mA (PM2131AHT)1011: 3180 mA
1100: 3472 mA 1101: 3760 mA
1110: 4050 mA 1111: 4340 mA

8.1.7 Battery charger control register 7 (voltage control), address = 06h

7	6	5	4	3	2	1	0
RESERVED				ChVresumeVoltLevel		RESERVED	
R				R/W		R	

Address: 06h

Type: R/W

Reset: Battery disconnection or low power mode

Description:

[7:4] RESERVED

[3:2] ChVresumeVoltLevel: battery voltage threshold restarts the charger (limits the battery charge cycle) (3.6 V and 4.0 V are predefined parameters)

00: 3.4 V

01: 3.6 V (PM2131AST)

10: 3.8 V

11: 4.0 V (PM2131AHT, PM2131UHT)

[1:0] RESERVED

8.1.8 Battery charger control register 8 (voltage control), address = 07h

7	6	5	4	3	2	1	0
RESERVED		ChVoltLevel					
R		R/W					

Address: 07h

Type: R/W

Reset: Software watchdog expiration or low power mode or battery disconnection

Description:

[7:6] RESERVED

[5:3] ChVoltLevel: float voltage charger level (3.8 V, 4.2 V, 4.275 V and 4.3 V are predefined parameters)
000000: 3.5 V
000001: 3.525 V
000100: 3.6 V
…
001000: 3.7 V
…
001100: 3.8 V (PM2131AST)
…

010100: 4.0 V
…
011011: 4.175 V
011100: 4.2 V (PM2131AHT, PM2131UHT)
…
011111: 4.275 V
100000: 4.3 V
…
100100: 4.4 V
100101: 4.425 V
100110: 4.45 V
100111: 4.475 V
101000: 4.5 V (max.)

8.1.9 NTC control register 1, address = 08h

7	6	5	4	3	2	1	0
RESERVED			BTempLowTh		BTempHighTh		
R			R/W		R/W		

Address: 08h

Type: R/W

Reset: Battery disconnection or low power mode

Description:

[7:5] RESERVED

[4:3] BTempLowTh: lower battery temperature range allowing the charge (predefined parameters)
00: -5 °C
01: 0 °C (PM2131AST, PM2131AHT, PM2131UHT)
10: 5 °C
11: 10 °C

[2:0} BTempHighTh: upper battery temperature range allowing the charge (45 °C, 55 °C, 60 °C and 65 °C are predefined parameters)
000: 45 °C (PM2131AST, PM2131AHT, PM2131UHT)
001: 50 °C
010: 55 °C
011: 60 °C
100: 65 °C
101: RESERVED
111: RESERVED

8.1.10 NTC control register 2, address = 09h

7	6	5	4	3	2	1	0
RESERVED					NTCresvalue		OUTCurrentMax
R					R/W		R/W

Address: 09h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:3] RESERVED

[2:1] NTCresvalue: selects the external thermal resistance (predefined parameters)
00: 10 kΩ, ß = 3964 (1%) (PM2131AHT)
01: 47 kΩ, ß = 3964 (1%) (PM2131AST, PM2131UHT)
10: 100 kΩ, ß = 3964 (1%)
11: no NTC

[0] OUTCurrentMax: increases to maximum output current setting when VBAT is overcharged voltage level (predefined parameter).
0: output current of the DC-DC is limited to charging current settings during the external charging mode (PM2131AST, PM2131AHT, PM2131UHT).
1: output current of the DC-DC is set to maximum during external charging mode as soon as the charge voltage level is reached.

8.1.11 Battery charger control register 9 (current control), address = 0Ah

7	6	5	4	3	2	1	0
RESERVED			150mVdrop	SWregulchargingcurrEna	ChCCreducedcurrent<1:0>		ChCCmodedrop
R			R/W	R/W	R/W		R/W

Address: 0Ah

Type: R/W

Reset: Low power mode

Description:

[7:5] RESERVED

[4] 150mVdrop: selects voltage drop between VBAT and VSYSTEM in hardware charging mode or in aging mode.

0: 300 mV drop between VSYSTEM and VBAT

1: 150 mV drop between VSYSTEM and VBAT (default)

[3] SWregulchargingcurrEna: enables interrupt when charging current is regulated due to high application loads

0: interruption is disabled (default)

1: interruption is enabled

[2:1] CCreducedcurrent level applied between Vprecharge and follower mode to reduce the power dissipation on the die

00: 100 mA charging current

01: 200 mA charging current

10 :400 mA charging current

11: equal to ChCCcurrentLevel from reg@05h (default)

[0] ChCCmodedrop: disable bit for CC current reduction

0: reduction of current when it is not in follower mode (default)

1: no reduced current in CC

8.1.12 Battery charger status register 1, address = 0Bh

7	6	5	4	3	2	1	0
RESERVED		VPWRrecognition_status			Chgstatus		
R		R			R		

Address: 0Bh

Type: R

Reset: NA

Description:

[7:6] RESERVED

[5:3] VPWRrecognition_status
000: wait for VPWR plug – no charger plug
001: VPWR sine wave detection pass successfully
010: CharrecEna1 (1st step of detection)
011: CharrecEna2 (2nd step of detection)
100: CharrecEna3 (3rd step of detection – sink current enable)
101: CharrecEna4 (4th step of detection – sine wave detection)
110: CharrecOVV ‡ overvoltage detected at plug: wait for the unplug
111: CharrecPirate ‡ Sine wave charger detected: wait for the unplug

[2:0] Chgdtatus: charger state indication bits
000: charging OFF
001: charging ON
010: battery fully charged
011: error (see battery charger error interrupt)
100: wait (NTC out of range)
101: no battery attached
110: RESERVED
111: RESERVED

8.1.13 Charger priority (VUSB or VPWR input), address = 10h

7	6	5	4	3	2	1	0
PPVSYSTEMLevel_extpp		VPWR PRIORITY	Res.	Res.	Res.	Res.	Res.
R/W		R/W					

Address: 10h

Type: R/W

Reset: Software watchdog expiration or external power source unplug or low power mode

Description:

[7:6] PPVSYSTEMLevel_extpp: VSYSTEM voltage programming (predefined parameters)
00 2.5 V
01 3.6 V
10 3.9 V (PM2131AST, PM2131UHT)
11 4.3 V (PM2131AHT)

[5] VPWR PRIORITY (predefined parameter)
0 VUSB used if both sources are connected (PM2131AST, PM2131AHT, PM2131UHT)
1 VPWR used if both sources are connected

[4:0] RESERVED

8.1.14 Input charger voltage VUSB, address = 11h

7	6	5	4	3	2	1	0
PPUSBnodroprecognEna	PPUSBCurrentLim				PPUSBOVVlevel		
R/W	R/W				R/W		

Address: 11h

Type: R/W

Reset: Software watchdog expiration or external power source unplug or low power mode

Description:

[7] PPUSBnodroprecognEna: enables automatic searching of maximum input current limit before enumeration

0: input current fixed by PPUSBCurrentLim before enumeration (default)

1: iterations to find maximum input current limit, which doesn't cause drop

[6:3] PPUSBCurrentLim: input current limit with R2 = 47 mΩ (predefined parameters are 75 mA, 145 mA, 435 mA, 650 mA, 725 mA, 1.3 A, 1.7 A, 2.17 A) & USBBC ball =0

0000: 75 mA

0001: 145 mA (PM2131AHT)

0010: 290 mA

0011: 435 mA (PM2131AST, PM2131UHT)

0100: 580 mA

0101: 650 mA

0110: 725 mA

0111: 865 mA

1000: 1010 mA

1001: 1150 mA

1010: 1300 mA

1011: 1440 mA

1100: 1590 mA

1101: 1735 mA

1110: 1880 mA

1111: 2170 mA

[6:3] Continued
PPUSBCurrentLim: input current limit with R2 = 47 mΩ (predefined parameters are 650 mA, 725 mA, 1.3 A, 2.17 A) & USBBC ball =1
0000: 75 mA
0001: 145 mA
0010: 290 mA
0011: 435 mA
0100: 580 mA
0101: 650 mA
0110: 725 mA
0111: 865 mA
1000: 1010 mA
1001: 1150 mA
1010: 1300 mA
1011: 1440 mA
1100: 1590 mA
1101: 1735 mA
1110: 1880 mA
1111: 2170 mA (PM2131AST, PM2131AHT, PM2131UHT)

[2:0] VUSBOVVlevel: level of overvoltage detection (predefined parameters)
000: 6.0 V
001: 6.5 V (PM2131UHT)
010: 7.5 V
011: 10.5 V
100: 12 V (PM2131AHT)
101: 14 V (PM2131AST)
110: 16 V
111: 10.5 V

8.1.15 Input charger drop PPUSB, address = 13h

7	6	5	4	3	2	1	0
PPUSBanaipoprog		PPUSBipomodeena		PPUSB ValidEna	PPUSB DropEna	PPUSBrefreshinputcurrent	
R/W		R/W		R/W	R/W	R/W	

Address: 13h

Type: R/W

Reset: Software watchdog expiration or the external power source unplug or low power mode

Description:

[7:6] PPUSBanaipoprog: programs analog IPO function to different voltage values (4.5 V or 4.7 V are predefined parameters)

00: 4.5 V regulation on VUSB (PM2131AST, PM2131AHT, PM2131UHT)

01: 4.6 V regulation on VUSB

10: 4.7 V regulation on VUSB

11: 4.8 V regulation on VUSB

[5:4] PPUSBipomodeena: enables IPO (input power optimization) feature in different modes (predefined parameters)

00: IPO loops disabled

01: digital IPO enabled

10: analog IPO enabled (PM2131AST, PM2131AHT, PM2131UHT)

11: IPO loops disabled + ICC loop disabled

[3] PPUSBValidEna: comparator indicates when VUSB voltage is over the detection threshold (min. 4.4 V)

0: comparator is disabled (default)

1: comparator is enabled

[2] PPUSBDropEna: enables VUSB voltage drop detection

0: VUSB input voltage drop close to VYSTEM or VBAT (default)

1: VUSB voltage cannot drop to VBAT below VUSBValidEna (also PPUSBValidEna must be set to 1 to support this function, otherwise it is ignored)

[1:0] PPUSBrefreshinputcurrent: enables to increase the input current limit when the external supply has not dropped for a certain lap of time

00: allows input current to increase all time (default)

01: 1 min. after last drop

10: 5 min. after last drop

11: 10 min. after last drop

8.1.16 PPUSB4, address = 14h

7	6	5	4	3	2	1	0
RESERVED						VUSBicsdisable	VUSBsuspend
R						R/W	R/W

Address: 14h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:2] RESERVED

[1] VUSBicsdisable: disables ICS on USB path (predefined parameters)
0: ICS is enabled (PM2131AST, PM2131AHT, PM2131UHT)
1: ICS is disabled

[0] VUSBsuspend: written by software when it decides to be in suspend mode from USB input, this means that neither charging nor SMPS is running. Low power consumption on VUSB input.
0: suspend is not detected (default)
1: suspend is detected => device must not draw current from the USB

8.1.17 Input charger voltage VPWR, address = 15h

7	6	5	4	3	2	1	0
VPWRnodroprecognEna	VPWRCurrentLim				VPWROVVlevel		
R/W	R/W				R/W		

Address: 15h

Type: R/W

Reset: **S**oftware watchdog expiration or external power source unplug or low power mode

Description:

[7] VPWRnodroprecognEna: enables automatic searching of maximum input current limit before enumeration

0: input current fixed by PPPWRCurrentLim before enumeration (default)

1: iterations to find maximum input current limit, which doesn't cause drop

[6:3] VPWRCurrentLim: input current limit with R1 = 47 mΩ (predefined parameters are 75 mA, 145 mA, 435 mA, 650 mA, 725 mA, 1.3 A, 1.7 A, 2.17 A) & USBBC ball =0

0000: 75 mA

0001: 145 mA (PM2131AHT)

0010: 290 mA

0011: 435 mA

0100: 580 mA

0101: 650 mA

0110: 725 mA

0111: 865 mA

1000: 1010 mA

1001: 1150 mA

1010: 1300 mA

1011: 1440 mA

1100: 1590 mA

1101: 1735 mA

1110 1880 mA

1111: 2170 mA (PM2131AST, PM2131UHT)

[6:3] Continued
VPWRCurrentLim: input current limit with R1 = 47 mΩ (predefined parameters are 650 mA, 725 mA, 1.3 A, 2.17 A) & USBBC ball =1
0000: 75 mA
0001: 145 mA
0010: 290 mA
0011: 435 mA
0100: 580 mA
0101: 650 mA
0110: 725 mA
0111: 865 mA
1000: 1010 mA
1001: 1150 mA
1010: 1300 mA
1011: 1440 mA
1100: 1590 mA
1101: 1735 mA
1110: 1880 mA
1111: 2170 mA (PM2131AST, PM2131AHT, PM2131UHT)

[2:0] VPWROVVlevel: level of overvoltage detection (predefined parameters)
000: 6.0 V
001: 6.5 V (PM2131UHT)
010: 7.5 V
011: 10.5 V
100: 12 V(PM2131AHT)
101: 14 V(PM2131AST)
110: 16 V
111: 10.5 V

8.1.18 Input charger drop VPWR, address = 17h

7	6	5	4	3	2	1	0
VPWRanaipoprog		VPWRipomodeena		VPWR ValidEna	VPWR DropEna	VPWRrefreshinputcurrent	
R/W		R/W		R/W	R/W	R/W	

Address: 17h

Type: R/W

Reset: Software watchdog expiration or external power source unplug or low power mode

Description:

[7:6] VPWRanaipoprog: programs analog IPO function to different voltage values (4.5 V and 4.7 V are predefined parameters).
00: 4.5 V regulation on VPWR (PM2131AST, PM2131AHT, PM2131UHT)
01: 4.6 V regulation on VPWR
10: 4.7 V regulation on VPWR
11: 4.8 V regulation on VPWR

[5:4] VPWRipomodeena: enables IPO (input power optimization) feature in different modes (predefined parameters).
00: IPO loops are disabled
01: digital IPO is enabled
10: analog IPO is enabled (PM2131AST, PM2131AHT, PM2131UHT)
11: IPO loops are disabled + ICC loop is disabled

[3] VPWRValidEna: comparator indicates when VPWR voltage is over the detection threshold (min. 4.4 V)
0: comparator is disabled (default)
1: comparator is enabled

[2] VPWRDropEna: enables VUSB voltage drop detection
0: VUSB input voltage can drop close to VYSTEM or VBAT (default)
1: VUSB voltage cannot drop below VPWRValidEna (also VPWRValidEna must be set to 1 to support this function, otherwise it is ignored)

[1:0] VPWRefreshinputcurrent: enables the rise of the input current limit when the external supply has not dropped for a certain period of time
00 allows input current to increase all time (default)
01 1 min. after last drop
10 5 min. after last drop
11 10 min. after last drop

8.1.19 Input charger mode for VPWR at 18h

7	6	5	4	3	2	1	0
RESERVED						VPWRicsdisable	VPWRsuspend
R						R/W	R/W

Address: 18h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:2] RESERVED

[1] VPWRicsdisable: disables ICS on PWR path (predefined parameter).
0: ICS is enabled (PM2131AST, PM2131AHT, PM2131UHT)
1: ICS disabled

[0] VPWRsuspend: written by software when it decides to be in suspend mode, this means that neither charging nor SMPS are running, low power consumption on VPWR input
0: suspend is not detected (default)
1: suspend is detected => device must not draw current from USB

8.1.20 Battery charger watchdog-kick control, address = 70h

7	6	5	4	3	2	1	0
WDCounter							
R/W							

Address: 70h

Type: R/W

Reset: 0000_0000

Description:

[7:0] WDcounter: writing any value allows watchdog to start or re-start. The watchdog must then be cleared regularly by any I^2C access (read/write). At external power source unplug, it is recommended that watchdog register should not be kicked in order to force the reset of all registers controlling the charging.
The reading of the register shows the last value of WD counter in 1/8 s. The maximum value 0xFF causes WD expiration and resets some registers to their initial values. The reading causes the reset of the WD counter just like any other I^2C access.

8.2 Miscellaneous control registers

8.2.1 Device version status, address = 0Ch

7	6	5	4	3	2	1	0
Version				Sub-version			
R				R			

Address: 0Ch

Type: R

Reset: 0001_0001

Description:

[7:4] Device version

[3:0] Device sub-version

8.2.2 Thermal Warning control register, address = 20h

7	6	5	4	3	2	1	0
RESERVED						ThWarningThreshold	
R						R/W	

Address: 20h

Type: R/W

Reset: Low power mode

Description:

[7:2] RESERVED

[1:0] ThWarningThreshold: die thermal warning temperature threshold
00: 110 °C
01: 120 °C
10: 130 °C (default)
11: 140 °C

8.2.3 Battery disconnect register, address = 21h

7	6	5	4	3	2	1	0
RESERVED							BatDisconnect
R							R/W

Address: 21h

Type: R/W

Reset: 0000_0000 low power mode

Description:

[7:1] RESERVED

[0] BatDisconnect: if the application processor has some features, which recognize a missing battery, this bit should be set according to current battery status

0: battery is present (default)

1: battery is not present

8.2.4 Battery low level comparator control register, address = 22h

7	6	5	4	3	2	1	0
RESERVED							VBATlowmonitoringEna
R							R/W

Address: 22h

Type: R/W

Reset: Low power mode

Description:

[7:1] RESERVED

[0] VBATlowmonitoringEna: enables/disables low level comparator for battery voltage detection (predefined parameter). It controls the transition from internal charging to external charging autonomously.

0: disabled (PM2131AST)

1: enabled (PM2131AHT, PM2131UHT)

8.2.5 Battery low level value control register, address = 23h

7	6	5	4	3	2	1	0
RESERVED			VBATlowlevel				
R	R		R/W				

Address: 23h

Type: R/W

Reset: Low power mode

Description:

[7:5] RESERVED

[4:0] VBATlowlevel: VBAT low level threshold (2.5 V, 3.6 V, 3.9 V or 4.2 V are predefined parameters)
00000: 2.3 V
00001: 2.4 V
00010: 2.5 V
…
01001: 3.2 V
01101: 3.6 V (PM2131AHT)
…
10000: 3.9 V (PM2131UHT)
…
10010: 4.1 V
10011…
11111: 4.2 V

8.2.6 I²C pad control register, address = 24h

7	6	5	4	3	2	1	0
RESERVED						I^2CinternaPullupEna	I^2ChsEna
R						R/W	R/W

Address: 24h

Type: R/W

Reset: Low power mode

Description:

[7:2] RESERVED

[1] I^2CinternaPullupEna: enables internal pull up on I²C pad
0: disabled (default)
1: enabled

[0] I^2ChsEna: enables high speed drivers on I²C pads active slope control
0: disabled: standard drivers (up to 400 kHz) (default)
1: enabled: high speed drivers

8.2.7 VPWR BOOST control register, address = 25h

7	6	5	4	3	2	1	0
RESERVED		VPWRboostprog		USBboostprog		RESERVED	USBboostena
R		R/W		R/W		R	R/W

Address: 25h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:6] RESERVED

[5:4] VPWRboostprog: programs boost voltage on VPWR path.The register bit enables the boost mode on VPWRpath, located at address @05h, bit4
00: 5.0 V (default)
01: 4.5 V
10: 7.0 V
11: 11.0 V

[3:2] USBboostprog: programs boost voltage on VUSB path
00: 5.0 V (default) (commonly named OTG mode)
01: 4.5 V
10: 7.0 V
11: 11.0 V

[1] RESERVED

[0] USBboostena: enables boost on VUSB
0: boost is disabled (default)
1: boost is enabled

8.2.8 EXTERNAL FET control register, address = 26h

7	6	5	4	3	2	1	0
RESERVED							FETCTRL
R							R/W

Address: 26h

Type: R/W

Reset: Software watchdog expiration or low power mode

[7:1] RESERVED

[0] FETCTRL: external FET control and end-of-charge controlled by software

0: external FET is OFF during charging in autonomous mode (default) (PM2131AHT, PM2131UHT) and EOC is managed autonomously by hardware

1: external FET is closed for charging operation (with reg @01h bit<2>=1), software is managing EOC

8.2.9 Free register, address = 27h

7	6	5	4	3	2	1	0
RESERVED							
R							

Address: 27h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:0] RESERVED

8.2.10 LED driver control register @ 28h

7	6	5	4	3	2	1	0
RESERVED			FMEAPROTDIS	LEDcurrent		LEDselect	antiovershoot
R			R/W	R/W		R/W	R/W

Address: 28h

Type: R/W

Reset: Software watchdog expiration or low power mode

Description:

[7:5] RESERVED

[4] FMEAPROTDIS
0: protection circuitry is enabled (default)
1: protection circuitry must be disabled for high-current applications. it is mandatory to set to 1 as soon as high-current charging mode in double path operation is set.

[3:2] LEDcurrent: LED current limitation
00: 2.5 mA (default)
01: 1 mA
10: 5 mA
11: 10 mA

[1] LEDselect: enables/disables the LED driver
0: enabled (default)
1: disabled

[0] Antiovershoot feature in CV charging mode (predefined parameter)
0: disables anti-overshoot feature (default)
1: enables anti-overshoot feature for CV mode

8.2.11 Digital state machine status @ 30h

7	6	5	4	3	2	1	0
RESERVED			Digital state machine status <4:0>				
R			R				

Address: 30h

Type: R

Reset: Not applicable

Description:

[7:5] RESERVED

[4:0] Digital state machine register bits
00000: reserved
00011: OTP loaded
00110: power ON mode (wait for plug, suspend mode, safety mode)
01000: direct mode charging allowed USB path priority
01001: direct mode charging allowed USB path priority
01010: transition from internal charging to external charging
10001: power path ON – charging allowed
10110: aging mode after EOC and external charging–charging is not allowed

8.3 Interrupt registers

8.3.1 Interrupt register 1 (battery charger interrupts), address = 40h

7	6	5	4	3	2	1	0
RESERVED				ITvbatlowF	ITvbatlowR	ITvbatdisconnect	ITVSYSTEMshort
R				R	R	R	R

Address: 40h

Type: R

Reset: 0000_0000

Description:

[7:4] RESERVED

[3] ITvbatlowF: falling edge of VBAT low signal (VBAT drops below VBAT LOW level)
0: no event (default)
1: VBAT below VBAT LOW level

[2] ITvbatlowR: rising edge of VBAT low signal (VBAT rises above VBAT LOW level)
0: no event (default)
1: VBAT above VBAT LOW level

[1] ITvbatdisconnect: battery is detected as disconnected
0: no event (default)
1: battery is detected as disconnected

[0] ITVSYSTEMshort: corrects VSYSTEM startup without any overload
0: no event (default)
1: VSYSTEM cannot start correctly, probably overload issues

8.3.2 Interrupt mask register 1 (battery charger interrupt masks), address = 50h

7	6	5	4	3	2	1	0
RESERVED				M_ITvbatlowF	M_ITvbatlowR	M_ITvbatdisconnect	M_ITVSYSTEMshort
R				R/W	R/W	R/W	R

Address: 50h

Type: R/W

Reset: 0000_0000

Description:

[7:4] RESERVED

[3] M_ITvbatlowF: masks the falling edge of VBAT low signal (VBAT drops below VBAT LOW level)
0: not masked (default)
1: masked

[2] M_ITvbatlowR: masks rising edge of VBAT low signal (VBAT grows above VBAT LOW level)
0: not masked (default)
1: masked

[1] M_ITvbatdisconnect: masks the battery disconnection indicated by internal state machine
0: not masked (default)
1: masked

[0] M_ITVSYSTEMshort: masks the VSYSTEM correct startup detection
0: not masked (default)
1: masked

8.3.3 Interrupt source register 1 (battery charger interrupt source), address = 60h

7	6	5	4	3	2	1	0
RESERVED				S_ITvbatlow	S_ITvbatlow	S_ITvbatdisconnect	S_ITVSYSTEMshort
R				R	R	R	R

Address: 60h

Type: R

Reset: 0000_0000

Description:

[7:4] RESERVED

[3:2] S_ITvbatlow: source for interruption on VBAT low signal
0: VBAT < VBATlow
1: VBAT > VBATlow

[1] S_ITvbatdisconnect: source for interruption on the battery disconnection indicated by internal state machine
0: battery is present (default)
1: battery detected is not present

[0] S_ITVSYSTEMshort
0: corrects VSYSTEM startup
1: start-up problem on VSYSTEM, overload issue

8.3.4 Interrupt register 2 (battery charger interrupt), address = 41h

7	6	5	4	3	2	1	0
ITVUSBboostoverload	ITVPWRboostoverload	ITVUSBboostOFFsafety	ITVPWRboostOFFsafety	ITVPWRunplug	ITVPWRplug	ITVUSBunplug	ITVUSBplug
R	R	R	R	R	R	R	R

Address: 41h

Type: R

Reset: 0000_0000

Description:

[7] ITVUSBboostoverload: overload current detected in VUSB boost mode. VBUS boost mode voltage decreases due to overload
0: no event (default)
1: overcurrent detected in VUSB boost mode

[6] ITVPWRboostoverload: overload current detected in VPWR boost mode. VPWR boost mode voltage decreases due to overload
0: no event (default)
1: overcurrent detected in VPWR boost mode

[5] ITVUSBboostOFFsafety: boost mode on VUSB path has collapsed for safety reasons
0: no event (default)
1: boost mode on USBpath is shutdown

[4] ITVPWRboostOFFsafety: boost mode on VPWRpath has collapsed for safety reasons
0: no event (default)
1: boost mode on VPWR path is shutdown

[3] ITVPWRunplug: external supply removed from VPWR
0: no event (default)
1: external supply removed from VPWR

[2] ITVPWRplug: external supply detected on VPWR
0: no event (default)
1: external supply detected on VPWR

[1] ITVUSBunplug: external supply removed from VUSB
0: no event (default)
1: external supply removed from VUSB

[0] ITVUSBplug: external supply detected on VUSB
0: no event (default)
1: external supply detected on VUSB

8.3.5 Interrupt mask register 2 (battery charger interrupt masks), address = 51h

7	6	5	4	3	2	1	0
M_ITVUSBboostoverload	M_ITVPWRboostoverload	M_ITVUSBboostOFFsafety	M_ITVPWRboostOFFsafety	M_ITVPWRunplug	M_ITVPWRplug	M_ITVUSBunplug	M_ITVUSBplug
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 51h

Type: R/W

Reset: 0000_0000

Description:

[7] M_ITVUSBboostoverload: masks overload current detected in VUSB boost mode
0: not masked (default)
1: masked

[6] M_ITVPWRboostoverload: masks overload current detected in VPWR boost mode
0: not masked (default)
1: masked

[5] M_ ITVUSBboostOFFsafety: masks USB shutdown event for safety reasons
0: not masked (default)
1: masked

[4] M_ ITVPWRboostOFFsafety: masks VPWR shutdown event for safety reasons
0: not masked (default)
1: masked

[3] M_ITVPWRunplug: masks the external supply removed from VPWR
0: not masked (default)
1: masked

[2] M_ITVPWRplug: masks external supply detected on VPWR
0: not masked (default)
1: masked

[1] M_ITVUSBunplug: masks the external supply removed from VUSB
0: not masked (default)
1: masked

[0] M_ITVUSBplug: masks the external supply detected on VUSB
0: not masked (default)
1: masked

8.3.6 Interrupt source register 2 (battery charger interrupt sources), address = 61h

7	6	5	4	3	2	1	0
S_ITVUSB boostoverload	S_ITVPWR boostoverload	S_ ITVUSBboostOFFsafety	S_ ITVPWRboostOFFsafety	S_ITVPWRplug		S_ITVUSBplug	
R	R	R	R	R		R	

Address: 61h

Type: R

Reset: 0000_0000

Description:

[7] S_ITVUSBboostoverload: overload current detected in VUSB boost mode
0: no event
1: overcurrent detected in VUSB boost mode

[6] S_ITVPWRboostoverload: overload current detected in VPWR boost mode
0: no event
1: overcurrent detected in VPWR boost mode

[5] S_ ITVUSBboostOFFsafety: VUSB boost mode collapses for safety reasons
0: VUSB correctly generated in boost mode
1: VUSB boost mode has collapsed for safety reasons

[4] S_ ITVPWRboostOFFsafety: VPWR boost mode collapses for safety reasons
0: VPWR correctly generated in boost mode
1: VPWR boost mode has collapsed for safety reasons

[3:2] S_ITVPWRplug: source for interruption on external supply plug on VPWR
0: no plug (default)
1: external supply plug on VPWR

[1:0] S_ ITVUSBplug: source for interruption on external supply plug on VUSB
0: no plug (default)
1: external supply plug on VUSB

8.3.7 Interrupt register 3 (battery charger interrupt), address = 42h

7	6	5	4	3	2	1	0
RESERVED				ITautotimeoutwd	ITchcvwd	ITchccwd	ITchprechargewd
R				R	R	R	R

Address: 42h

Type: R

Reset: 0000_0000

Description:

[7:4] RESERVED

[3] ITautotimeoutwd: auto timeout watchdog has expired (20 minutes elapsed time from start-up phase without any software activity)

0: no event (default)

1: auto timeout watchdog has expired (start-up phase lasts more than 20 minutes without software activity)

[2] ITchcvwd: CV phase watchdog has expired

0: no event (default)

1: CV phase watchdog has expired

[1] ITchccwd: CC phase watchdog has expired

0: no event (default)

1: CC phase watchdog has expired

[0] ITchprechargewd: pre-charge phase watchdog has expired

0: no event (default)

1: pre-charge phase watchdog has expired

8.3.8 Interrupt mask register 3 (battery charger interrupt masks), address = 52h

7	6	5	4	3	2	1	0
RESERVED				M_ITautotimeoutwd	M_ITchcvwd	M_ITchccwd	M_ITchprechargewd
R				R/W	R/W	R/W	R/W

Address: 52h

Type: R/W

Reset: 0000_0000

Description:

[7:4] RESERVED

[3] M_ITautotimeoutwd: auto timeout watchdog has expired (20 minutes elapsed time from start-up phase without any software activity)
0: not masked (default)
1: masked

[2] M M_ITchcvwd: CV phase watchdog has expired
0: not masked (default)
1: masked

[1] M_ITchccwd: CC phase watchdog has expired
0: not masked (default)
1: masked

[0] M_ITchprechargewd: pre-charge phase watchdog has expired
0: not masked (default)
1: masked

8.3.9 Interrupt source register 3 (battery charger interrupt sources), address = 62h

7	6	5	4	3	2	1	0
RESERVED				S_ITautotimeoutwd	S_ITchcvwd	S_ITchccwd	S_ITchprechargewd
R				R	R	R	R

Address: 62h

Type: R

Reset: 0000_0000

Description:

[7:4] RESERVED

[3] S_ITautotimeoutwd: source for interruption on auto timeout watchdog has expired (20 minutes elapsed time from start-up phase without any software activity)

0: no event (default)

1: auto timeout watchdog has expired (start-up phase lasts more than 20 minutes without any software activity)

[2] S_ITchcvwd: source for interruption on CV phase watchdog expiration

0: no event (default)

1: CV phase watchdog has expired

[1] S_ITchccwd: source for interruption on CC phase watchdog expiration

0: no event (default)

1: external supply removed from VPWR

[0] S_ITchprechargewd: source for interruption on pre-charge phase watchdog expiration

0: no event (default)

1: pre-charge phase watchdog has expired

8.3.10 Interrupt register 4 (battery charger interrupt), address = 43h

7	6	5	4	3	2	1	0
ITcvphase	ITbattfull	ITvresume	ITchargingon	ITVPWRovv	ITVUSBovv	ITbattemphot	ITbattempcold
R	R	R	R	R	R	R	R

Address: 43h

Type: R

Reset: 0000_0000

Description:

[7] ITcvphase: charging reached constant voltage phase
0: no event (default)
1: battery in CV phase

[6] ITbattfull: end-of-charge has been detected (no more charging phase until Vresume threshold is crossed or charging resume bit is set even if battery voltage is above Vresume)
0: no event (default)
1: battery is fully charged

[5] ITvresume: battery is discharged down to Vresume threshold
0: no event (default)
1: new charging cycle can be restarted by Vresume voltage

[4] ITchargingon: the charging operation has started
0: no event (default)
1: the charging operation has started

[3] ITVPWRovv: overvoltage is detected on VPWR
0: no event (default)
1: overvoltage is detected on VPWR

[2] ITVUSBovv: overvoltage is detected on VUSB
0: no event (default)
1: overvoltage is detected on VUSB

[1] ITbattemphot: battery temperature is too high for charging
0: no event (default)
1: battery temperature is too high for charging

[0] ITbattempcold: battery temperature is too low for charging
0: no event (default)
1: battery temperature is too low for charging

8.3.11 Interrupt mask register 4 (battery charger interrupt masks), address = 53h

7	6	5	4	3	2	1	0
M_ ITcvphase.	M_ ITbattfull	M_ IT vresume	M_ ITchargingon	M_ ITVPWRovv	M_ ITVUSBovv	M_ ITbattemphot	M_ ITbattempcold
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 53h

Type: R/W

Reset: 0000_0000

Description:

[7] M_ITcvphase: charging is in constant voltage phase with 1 C charging current
0: not masked (default)
1: masked

[6] M_ITbattfull: end-of-charge has been detected (no more charging phase until Vresume threshold is crossed or charging resume bit is set even if battery voltage is above Vresume)
0: not masked (default)
1: masked

[5] M_ITvresume: battery is discharged down to Vresume threshold
0: not masked (default)
1: masked

[4] M_ ITchargingon: the charging operation has started
0: not masked (default)
1: masked

[3] M_ITVPWRovv: overvoltage is detected on VPWR
0: not masked (default)
1: masked

[2] M_ITVUSBovv: overvoltage is detected on VUSB
0: not masked (default)
1: masked

[1] M_ITbattemphot: battery temperature is too high for charging
0: not masked (default)
1: masked

[0] M_ITbattempcold: battery temperature is too low for charging
0: not masked (default)
1: masked

8.3.12 Interrupt source register 4 (battery charger interrupt sources), address = 63h

7	6	5	4	3	2	1	0
S_ITcvphase	S_ITbattfull	S_ITvresume	S_ITchargingon	S_ITVPWRovv	S_ITVUSBovv	S_ITbattemphot	S_ITbattempcold
R	R	R	R	R	R	R	R

Address: 63h

Type: R

Reset: 0000_0000

Description:

[7] S_ITcvphase: source for interruption detecting constant voltage phase with 0.5 C charging current.
0: no event (default)
1: battery in CV phase at 1C

[6] S_ITbattfull: source for interruption detecting end-of-charge has been detected ((no more charging phase until Vresume threshold is crossed or charging resume bit is set even if battery voltage is above Vresume))
0: no event (default)
1: battery is fully charged

[5] S_ITvresume: source for interruption detecting battery voltage discharged down to Vresume threshold
0: no event (default)
1: new charging cycle can be restarted by Vresume voltage

[4] S_ITchargingon: source for interruption detecting the charging operation has started
0: no event (default)
1: the charging operation has started

[3] S_ITVPWRovv: source for interruption detecting overvoltage detected on VPWR
0: no event (default)
1: overvoltage detected on VPWR

[2] S_ITVUSBovv: source for interruption detecting overvoltage detected on VUSB
0: no event (default)
1: overvoltage detected on VUSB

[1] S_ITbattemphot: source for interruption detection battery temperature is too high for charging
0: no event (default)
1: battery temperature is too high for charging

[0] S_ITbattempcold: source for interruption detecting battery temperature is too low for charging
0: no event (default)
1: battery temperature is too low for charging

8.3.13 Interrupt register 5 (charger and die temperature interrupt), address = 44h

7	6	5	4	3	2	1	0
RESERVED			ITVSYSTEMovv	ITthermal Warningfall	ITthermal warningrise	ITthermal shutdownfall	ITthermal shutdownrise
R			R	R	R	R	R

Address: 44h

Type: R

Reset: 0000_0000

Description:

[7:5] RESERVED

[4] ITVSYSTEMovv: overvoltage is detected on VSYSTEM node
0: no event (default)
1: VSYSTEM overvoltage is detected

[3] ITthermalwarningfall: die temperature has dropped below warning level
0: not masked (default)
1: temperature decreases below the warning threshold

[2] ITthermalwarningrise: die temperature has reached the warning level
0: no event (default)
1: temperature increases above the warning threshold

[1] ITthermalshutdownfall: die temperature has dropped below shutdown level
0: no event (default)
1: temperature decreases below the shutdown threshold

[0] ITthermalshutdownrise: die temperature has reached the shutdown level
0: no event (default)
1: temperature increases above the shutdown threshold

8.3.14 Interrupt mask register 5 (charger and die temperature mask), address = 54h

7	6	5	4	3	2	1	0
RESERVED			M_ITVSYSTEMovv	M_ITthermal Warningfall	M_ITthermal warningrise	M_ITthermal shutdownfall	M_ITthermal shutdownrise
R			R/W	R/W	R/W	R/W	R/W

Address: 54h

Type: R/W

Reset: 0000_0000

Description:

[7:5] RESERVED

[4] M_ITVSYSTEMovv: overvoltage is detected on VSYSTEM node
0: not masked (default)
1: masked

[3] M_ITthermalwarningfall: die temperature has dropped below the warning level
0: not masked (default)
1: masked

[2] M_ITthermalwarningrise: die temperature has reached the warning level
0: not masked (default)
1: masked

[1] M_ITthermalshutdownfall: die temperature has dropped below shutdown level
0: not masked (default)
1: masked

[0] M_ITthermalshutdownrise: die temperature has reached the shutdown level
0: not masked (default)
1: masked

8.3.15 Interrupt source register 5 (charger and die temperature interrupt sources), address = 64h

7	6	5	4	3	2	1	0
RESERVED			S_ITVSYSTEMovv	S_ITthermal Warning	S_ITthermal Warning	S_ITthermal shutdown	S_ITthermal shutdown
R			R	R	R	R	R

Address: 64h

Type: R

Reset: 0000_0000

Description:

[7:5] RESERVED

[4] S_ITVSYSTEMovv: source for interruption detecting overvoltage on VSYSTEM node
0: no event (default)
1: VSYSTEM overvoltage detected

[3] S_ITthermalwarningfall: source for interruption detecting die temperature has reached warning level
0: no thermal warning (default)
1: temperature has reached the warning threshold

[2] S_ITthermalwarningfall: source for interruption detecting die temperature has reached the warning level
0: no thermal warning (default)
1: temperature has reached the warning threshold

[1] S_ITthermalshutdown: source for interruption detecting die temperature has reached the shutdown level
0: no thermal shutdown (default)
1: temperature has reached the shutdown threshold

[0] S_ITthermalshutdown: source for interruption detecting die temperature has reached the shutdown level
0: no thermal shutdown (default)
1: temperature has reached the shutdown threshold

8.3.16 Interrupt register 6 (charger interrupt), address = 45h

7	6	5	4	3	2	1	0
ITFMEAprotfall.	ITFMEAprotrise	ITVPWRvalid fall	ITVPWRvalid rise	ITVUSBvalid fall	ITVPW2valid rise	ITVPWRdrop	ITVUSBdrop
R	R	R	R	R	R	R	R

Address: 45h

Type: R

Reset: 0000_0000

Description:

[7] ITFMEAprotfall
0: no event (default)
1: falling edge of FMEA protection signal

[6] ITFMEAprotrise
0: no event (default)
1: rising edge of FMEA protection signal

[5] ITVPWRvalidfall: falling edge of WPWRvalid signal
0: no event (default)
1: falling edge of WPWRvalid signal

[4] ITVPWRvalidrise: rising edge of WPWRvalid signal
0: no event (default)
1: rising edge of WPWRvalid signal

[3] ITVUSBvalidfall: falling edge of VUSBvalid signal
0: no event (default)
1: falling edge of WUSBvalid signal

[2] ITVUSBvalidrise: rising edge of VUSBvalid signal
0: no event (default)
1: rising edge of VUSBvalid signal

[1] ITVPWRdrop: indicates that VPWR has dropped to VBAT level
0: not event (default)
1: VPWR drop

[0] ITVUSBdrop: indicates that VUSB has dropped to VBAT level
0: not event (default)
1: WUSB drop

8.3.17 Interrupt mask register 6 (battery charger masks), address = 55h

7	6	5	4	3	2	1	0
M_ ITFMEAprotfall	M_ ITFMEAprotrise	M_ITVPWRvalidfall	M_ITVPWRvalidrise	M_ITVUSBvalidfall	M_ITVUSBvalidrise	M_ITVPWRdrop	M_ITVUSBdrop
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 55h

Type: R/W

Reset: 0000_0000

Description:

[7] M_ ITFMEAprotfall: falling edge of FMEAprot signal
0: not masked (default)
1: masked

[6] M_ ITFMEAprotrise: rising edge of FMEAprot signal
0: not masked (default)
1: masked

[5] M_ITVPWRvalidfall: falling edge of WPWRvalid signal
0: not masked (default)
1: masked

[4] M_ITVPWRvalidrise: rising edge of WPWRvalid signal
0: not masked (default)
1: masked

[3] M_ITVUSBvalidfall: falling edge of VUSBvalid signal
0: not masked (default)
1: masked

[2] M_ITVUSBvalidrise: rising edge of VUSBvalid signal
0: not masked (default)
1: masked

[1] M_ITVPWRdrop: indicates that WPWR has dropped to VBAT level
0: not masked (default)
1: masked

[0] M_ITVUSBdrop: indicates that WUSB has dropped to VBAT level
0: not masked (default)
1: masked

8.3.18 Interrupt source register 6 (charger interrupt sources), address = 65h

7	6	5	4	3	2	1	0
S_ ITFMEAprol	S_ ITFMEAprot	S_ITVPWR valid	S_ITVPWR valid	S_ITVUSB valid	S_ITVPW2 valid	S_ITVPWRdrop	ITVUSBdrop
R	R	R	R	R	R	R	R

Address: 65h

Type: R

Reset: 0000_0000

Description:

[7] S_ ITFMEAprot: source for interruption, detecting FMEA protection, is detected
0: no FMEA protection event present (default)
1: FMEA protection event detected

[6] S_ ITFMEAprot: source for interruption detecting FMEA protection is detected
0: no FMEA protection event present (default)
1: FMEA protection event detected

[5] S_ ITVPWRvalid: source for interruption, detecting WPWR, has reached WPWRvalid threshold
0: below WPWRvalid threshold (default)
1: over WPWRvalid threshold

[4] S_ ITVPWRvalid: source for interruption, detecting WPWR, has reached WPWRvalid threshold
0: below WPWRvalid threshold (default)
1: over WPWRvalid threshold

[3] S_ITVUSBvalid: source for interruption, detecting WUSB, has reached WUSBvalid threshold
0: below VUSBvalid threshold (default)
1: over VUSBvalid threshold

[2] S_ITVUSBvalid: source for interruption, detecting WUSB, has reached WUSBvalid threshold
0: below VUSBvalid threshold (default)
1: over VUSBvalid threshold

[1] ITVPWRdrop: indicates that VPWR has dropped to VBAT level
0: not event (default)
1: VPWR drop

[0] ITVUSBdrop: indicates that VUSB has dropped to VBAT level
0: not event (default)
1: WUSB drop

8.3.19 Interrupt register 7 (charger interrupt), address = 46h

7	6	5	4	3	2	1	0
RESERVED			ITVUSBboost0pwmdet	ITVPWRboost0pwmdet	IToverloadversuscharging	RESERVED	
R			R	R	R	R	

Address: 46h

Type: R

Reset: 0000_0000

Description:

[7:5] RESERVED

[4] ITVUSBboost0pwmdet: detects 0%PWM (open loop) on VUSB boost
0: no event (default)
1: rising edge of the 0% PWM comparator

[3] ITVPWRboost0pwmdet: detects 0%PWM (open loop) on VPWR boost
0: no event (default)
1: rising edge of the 0% PWM comparator

[2] IToverloadversuscharging: indicates that application takes too much power and internal charging mode cannot be performed correctly
0: no event (default)
1: application is taking too much current and charging cannot be performed

[1:0] RESERVED

8.3.20 Interrupt mask register 7 (battery charger masks), address = 56h

7	6	5	4	3	2	1	0
RESERVED			M_ITVUSBboost0pwmdet	M_ITVPWRboost0pwmdet	M_IToverloadversuscharging	RESERVED	
R			R/W	R/W	R/W	R	

Address: 56h

Type: R/W

Reset: 0000_0000

Description:

[7:5] RESERVED

[4] M_ITVUSBboost0pwmdet: rising edge of the 0%PWM detection comparator (VUSB boost)
0: not masked (default)
1: masked

[3] M_ITVPWRboost0pwmdet: rising edge of the 0%PWM detection comparator (VPWR boost)
0: not masked (default)
1: masked

[2] M_IToverloadversuscharging: application is taking too much current and charging cannot be performed
0: not masked (default)
1: masked

[1:0] RESERVED

8.3.21 Interrupt source register7 (charger interrupt sources), address = 66h

7	6	5	4	3	2	1	0
RESERVED			S_ITVUSBboost0pwmdet	S_ITVPWRboost0pwmdet	S_IToverloadversuscharging	RESERVED	
R			R	R	R	R	

Address: 66h

Type: R

Reset: 0000_0000

Description:

[7:5] RESERVED

[4] S_ITVUSBboost0pwmdet: source for interruption 0%PWM (open loop) on VUSB boost
0: no event
1: 0%PWM (open loop) on VUSB boost

[3] S_ITVPWRboost0pwmdet: source of interruption 0%PWM (open loop) on VPWR boost
0: not event (default)
1: 0%PWM (open loop) on VPWR boost

[2] S_IToverloadversuscharging: source for interruption is detecting that application takes too much power and charging cannot be performed
0: no event
1: application is taking too much current and charging cannot be performed

[1:0] RESERVED

9 Package mechanical data

The PM2131 package is a wafer level chip scale package (WLCSP).

The package code is 01C1 (Line TC36)

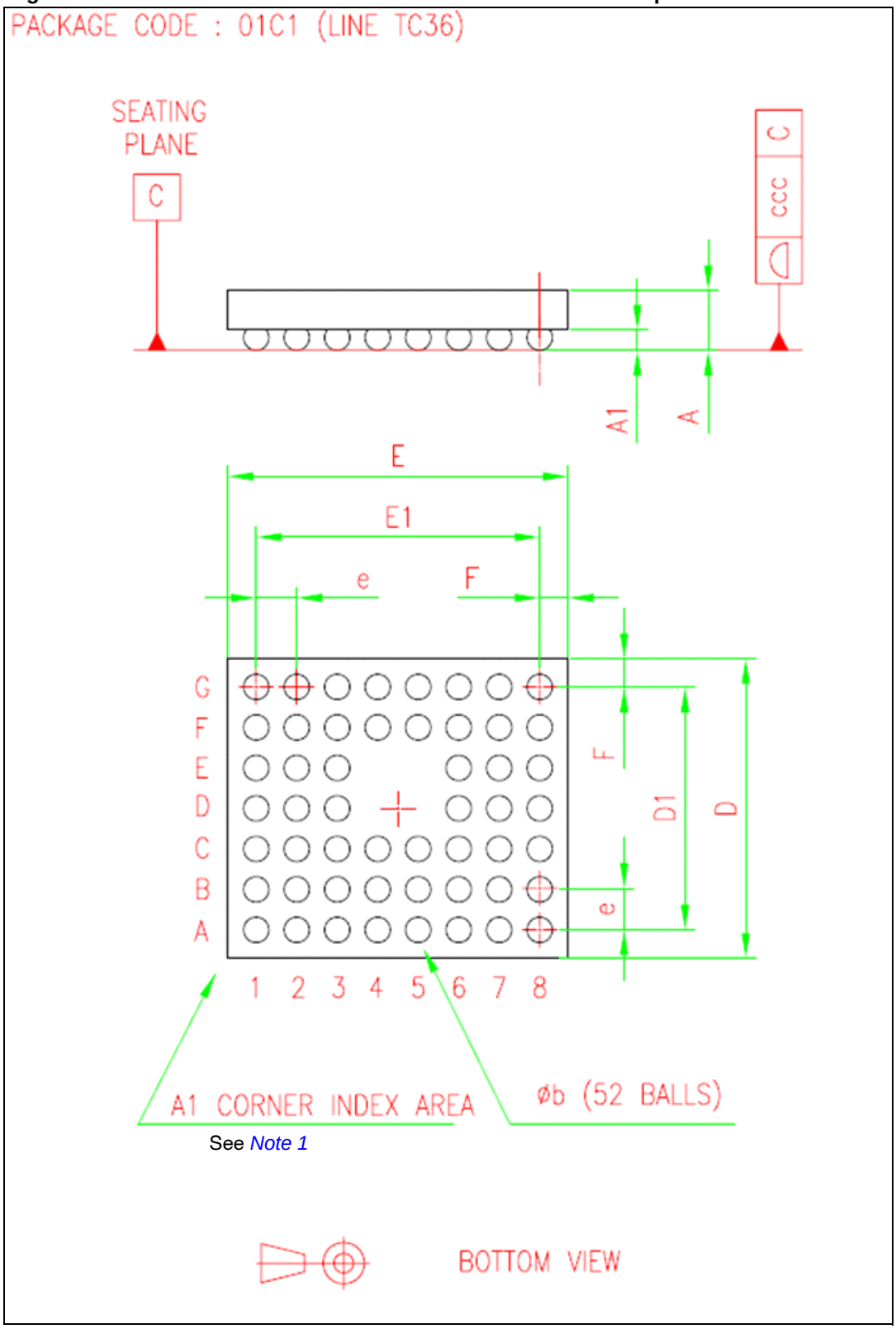
JEDEC/EIAJ reference number = NA

Table 12. WLCSP 3.36 mm x 2.96 mm x 0.59 mm with 0.4 mm pitch and 0.25 mm ball

	Min.	Typ.	Max.	Unit
A			0.59	mm
A1	0.13			mm
b(1)	0.22	0.27	0.32	mm
D	2.90	2.96	2.98	mm
D1		2.40		mm
E	3.30	3.36	3.38	mm
E1		2.80		mm
e		0.40		mm
F(2)		0.28		mm
ccc			0.03	mm

1. The typical ball diameter before mounting is 0.25 mm.
2. The ball matrix array is not symmetrical (balls D4, D5, E4, E5 out).

Figure 10. WLCSP 3.36 mm x 2.96 mm x 0.59 mm with 0.4 mm pitch and 0.25 mm ball



1. The terminal A1 corner must be identified on the top surface by using a laser marking dot.

10 Ordering information

Table 13. Ordering information

Order code	Marking	Package	Base quantity	Delivery mode
PM2131AST	PM2131AS	WLCSP 3.36 mm x 2.96 mm x 0.59 mm with 0.4 mm pitch and 0.25 mm ball	5000	Tape and reel
PM2131AHT	PM2131AH	WLCSP 3.36 mm x 2.96 mm x 0.59 mm with 0.4 mm pitch and 0.25 mm ball	5000	Tape and reel
PM2131UHT	PM2131UH	WLCSP 3.36 mm x 2.96 mm x 0.59 mm with 0.4 mm pitch and 0.25 mm ball	5000	Tape and reel

11 Glossary

CC	Constant current
CCCV	Constant current constant voltage
CDM	Charged device model
CDP	Charger down stream USB port
DC	Direct current
DCP	Dedicated charger USB port
ESD	Electrostatic discharge
ESR	Equivalent series resistance
FET	Field-effect transistor
GSM	Global system for mobile communication
HBM	Human body model
I/O	Input/output
ID	Identification
IEEE	Institute of Electrical and Electronics Engineers
IRQ	Interrupt request ARM™ (normal)
MOSFET	Metal-oxide-semiconductor field-effect transistor
NTC	Negative temperature coefficient
OTG	On-The-Go
PWM	Pulse width modulation
SCL	Serial clock
SDP	Standard down stream USB port

12 References

1. Universal Serial Bus (USB) Specification - Rev. 2.0 - *http://www.usb.org/developers/docs/*
2. USB Battery Charging Specification - Rev. 1.2 - *http://www.usb.org/developers/devclass_docs*

13 Revision history

Table 14. Document revision history

Date	Revision	Changes
09-Aug-2012	1	Initial release.
01-Sep-2012	2	Updated the following: – Timing diagrams – Application figure – Registers Applied some editorial changes
07-May-2013	3	Updated the following – *Table 6: Electrical characteristics for DC-DC charger* – *Table 8: Temperature monitoring* – *Chapter 5: Device interface* – *Chapter 6: Functional description* – *Chapter 7: Application hints* – *Chapter 8: Register description*
03-Jun-2013	4	Updates in the following parts of the document – *Chapter 3: Electrical characteristics* – *Chapter 4: DC-DC battery charger with power path* – *Chapter 5: Device interface* – *Chapter 6: Functional description* – *Chapter 8: Register description*
18-Dec-2013	5	Document modified to ST branding. Minor text changes.

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