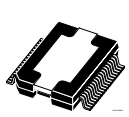
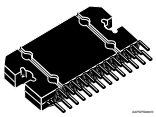
TDA7802

High efficiency digital input quad power amplifier with built-in diagnostics features, 'start stop' compatible

Datasheet - production data



PowerSO36



Flexiwatt27

Features

- 24-bit resolution
- 110 dB dynamic range (A-weighted)
- SB-I (SB - improved) high efficiency operation the highest 'non - class D' efficiency
- 1 Ohm driving capability (only in PowerSO36 package)
  - High output power capability: 4 x 28 W 4 Ω @ 14.4 V, 1 kHz, THD = 10 %
  - Max output power: 4 x 72 W 2 Ω
- Flexible mode control:
  - Full I^2C bus driving 1.8V/3.3V) with four addresses selectable (only for PowerSO36 package option)
  - Independent front/rear play/ mute
  - Four selectable gains for very-low noise line-out function
  - Digital diagnostic with DC and AC load detections
- Optional H/W control (no I^2C bus)
- Start-stop compatibility (operation down to 6V)
- Sample rates: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Flexible serial data port (1.8 V / 3.3 V):
  - I^2S standard, TDM 4Ch, TDM 8Ch, TDM 16Ch
- Offset detector (play or mute mode)
- Independent front/rear clipping detector
- Programmable diagnostic pin
- CMOS compatible enable pin
- Thermal protection

Description

The TDA7802 is a single chip quad bridge amplifier integrating a full D/A converter and digital input for direct connection to I^2S (or TDM) together with powerful MOSFET output stages, thanks to the advanced BCD technology adopted.

The integrated D/A converter allows the performance to reach an outstanding 115 dB S/N ratio with more than 110 dB of dynamic range.

Moreover the TDA7802 integrates an innovative high efficiency concept, optimized also for uncorrelated music signals, that makes it the most suitable device to simplify the thermal management in high power sets.

Thanks to this concept, the dissipated output power under average listening conditions can be reduced up to 50% when it is compared to the level provided by conventional class AB solutions.

The TDA7802 integrates also a programmable PLL that is able to lock at the input frequencies of 64*Fs and 50*Fs for all the input configurations.

Thanks to the digital concept, the TDA7802 is equipped with a full diagnostics array that communicates the status of each speaker through the I^2C bus. It is moreover possible to control the configuration and behavior of the device through the I^2C bus.

TDA7802 is moreover able to play music down to 6 V supply voltage - so it is compatible with the so called 'start stop' battery profile recently adopted by several car makers (in order to optimize the fuel consumption and to reduce the impact over the environment).

Table 1. Device summary

Order code	Package	Packing
TDA7802	Flexiwatt27	Tube
TDA7802PD	PowerSO36	Tube
TDA7802PDTR	PowerSO36	Tape and reel

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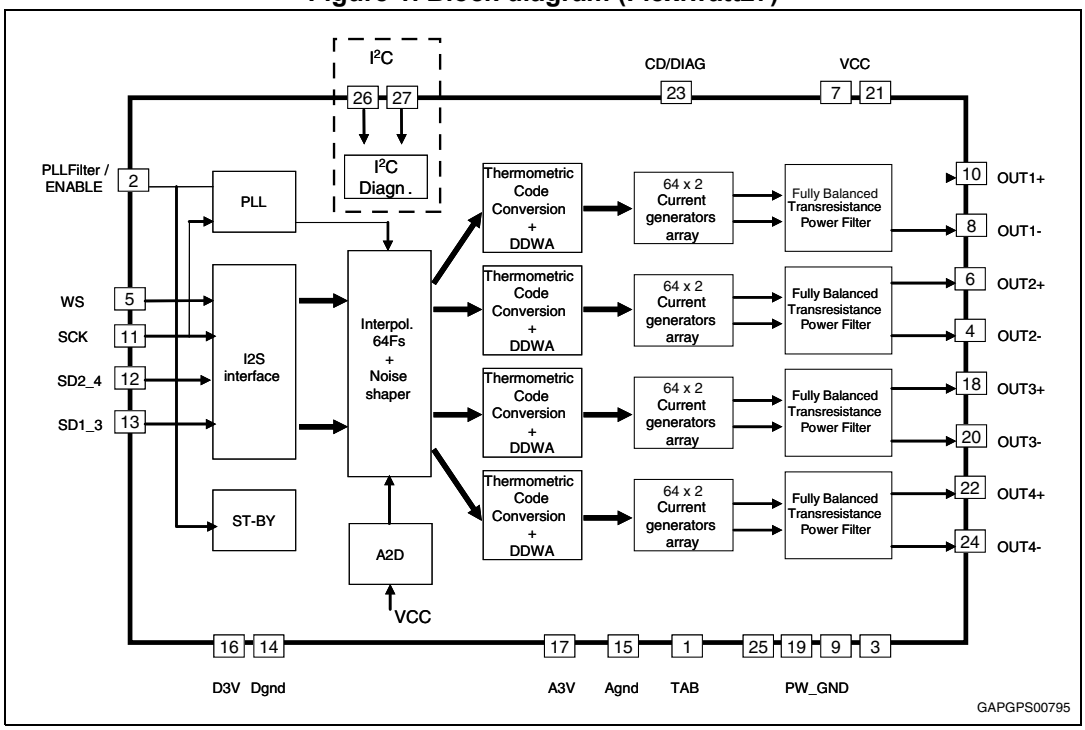
1.1 Block diagram

Figure 1. Block diagram (Flexiwatt27)



1.2 Pins description

Figure 2. Pins connection diagrams

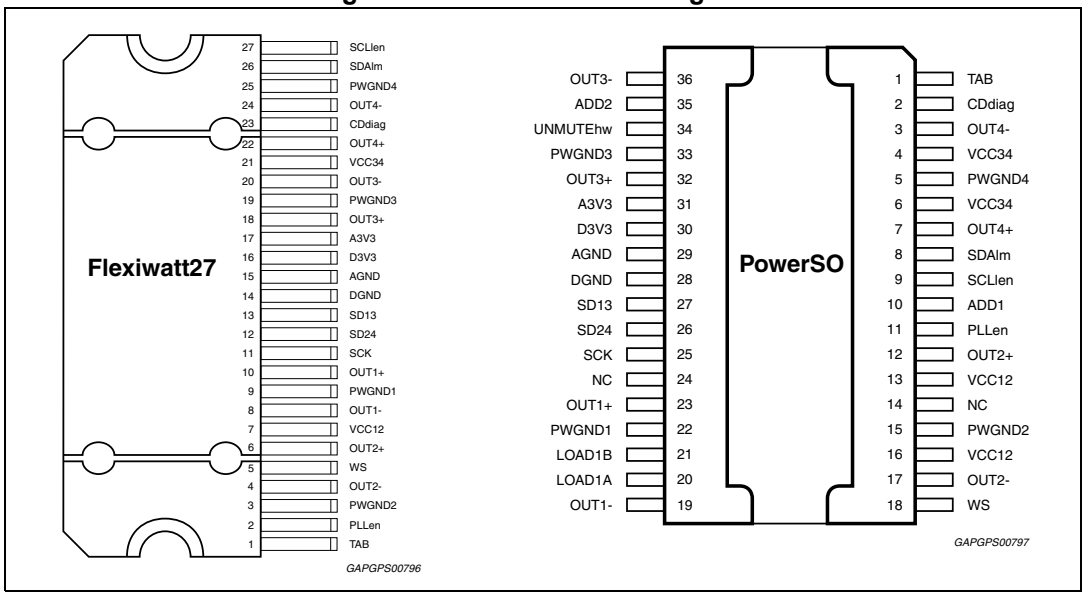


Table 2. Flexiwatt27 pins description

N°	Pin	Function	
1	TAB	TAB connection	Ground
2	PLLen	Pll loop filter / ENABLE	Input
3	PWGND2	Power ground channel 2	Power Ground
4	OUT 2-	Channel 2 (Left Rear) negative output	Power Output
5	WS	Word select (I2S bus)	Logic Input
6	OUT 2+	Channel 2 (Left Rear) positive output	Power Output
7	VCC12	Channel 1 and 2 positive supply	Battery
8	OUT 1-	Channel 1 (Left Front) negative output	Power Output
9	PWGND1	Power ground channel 1	Power Ground
10	OUT 1+	Channel 1 (Left Front) positive output	Power Output
11	SCK	Serial clock (I2S bus)	Logic Input
12	SD24	Serial data channels 2 and 4 (I2S bus)	Logic Input
13	SD13	Serial data channels 1 and 3 (I2S bus)	Logic Input
14	DGND	Digital ground	Signal Ground
15	AGND	Analog ground	Signal Ground
16	D3V3	Digital 3.3 V supply filter	Digital Regulator
17	A3V3	Analog 3.3 V supply filter	Analog Regulator
18	OUT3+	Channel 3 (right front) positive output	Power Output
19	PWGND3	Power ground channel 3	Power Ground
20	OUT3-	Channel 3 (right front) negative output	Power Output
21	VCC34	Channels 3 and 4 positive supply	Battery
22	OUT4+	Channel 4 (right rear) positive output	Power Output
23	CDdiag	Clip detector and diagnostic output: Overcurrent protection intervention Thermal warning POR Output DC offset Output short to VCC/GND	Open Drain Output
24	OUT4-	Channel 4 (right rear) negative output	Power Output
25	PWGND4	Power ground channel 4	Power Ground
26	SDAIm	I^2C data/legacy mode mute	Signal Input/Output
27	SCLIen	I^2C clock/enable legacy mode	Signal Input

Table 3. PowerSO36 pins description

N°	Pin	Function	
1	TAB	TAB connection	-
2	CDdiag	Clip detector and diagnostic output: Overcurrent protection intervention Thermal warning POR	Open Drain Output
3	OUT4-	Channel 4 (right rear) negative output	Power Output
4	VCC34	Channels 3 and 4 positive supply	Battery
5	PWGND4	Power ground channel 4	Power Ground
6	VCC34	Channels 3 and 4 positive supply	Battery
7	OUT4+	Channel 4 (right rear) positive output	Power Output
8	SDAIm	I^2C data/legacy mode mute	Signal Input/Output
9	SCLIen	I^2C clock/enable legacy mode	Signal Input
10	ADD1	I2C Address - First Pin	Logic Input
11	PLLen	Pll loop filter / ENABLE	Input
12	OUT 2+	Channel 2 (Left Rear) positive output	Power Output
13	VCC12	Channel 1 and 2 positive supply	Battery
14	NC	Not Connected	-
15	PWGND2	Power ground channel 2	Power Ground
16	VCC12	Channel 1 and 2 positive supply	Battery
17	OUT 2-	Channel 2 (Left Rear) negative output	Power Output
18	WS	Word select (I2S bus)	Logic Input
19	OUT 1-	Channel 1 (Left Front) negative output	Power Output
20	LOAD1A	Load Selection (channels 1 and 2)	Logic Input
21	LOAD1B	Load Selection (channels 3 and 4)	Logic Input
22	PWGND1	Power ground channel 1	Power Ground
23	OUT 1+	Channel 1 (Left Front) positive output	Power Output
24	NC	Not Connected	-
25	SCK	Serial clock (I2S bus)	Logic Input
26	SD24	Serial data channels 2 and 4 (I2S bus)	Logic Input
27	SD13	Serial data channels 1 and 3 (I2S bus)	Logic Input
28	DGND	Digital ground	Signal Ground
29	AGND	Analog ground	Signal Ground
30	D3V3	Digital 3.3 V supply filter	Digital Regulator
31	A3V3	Analog 3.3 V supply filter	Analog Regulator
32	OUT3+	Channel 3 (right front) positive output	Power Output
33	PWGND3	Power ground channel 3	Power Ground
34	UNMUTEhw	Unmute Hardware	Logic input
35	ADD2	I2C Address - Second Pin	Logic Input
36	OUT3-	Channel 3 (right front) negative output	Power Output

2 Application diagrams

Figure 3. I²C bus mode application diagram (TDA7802)

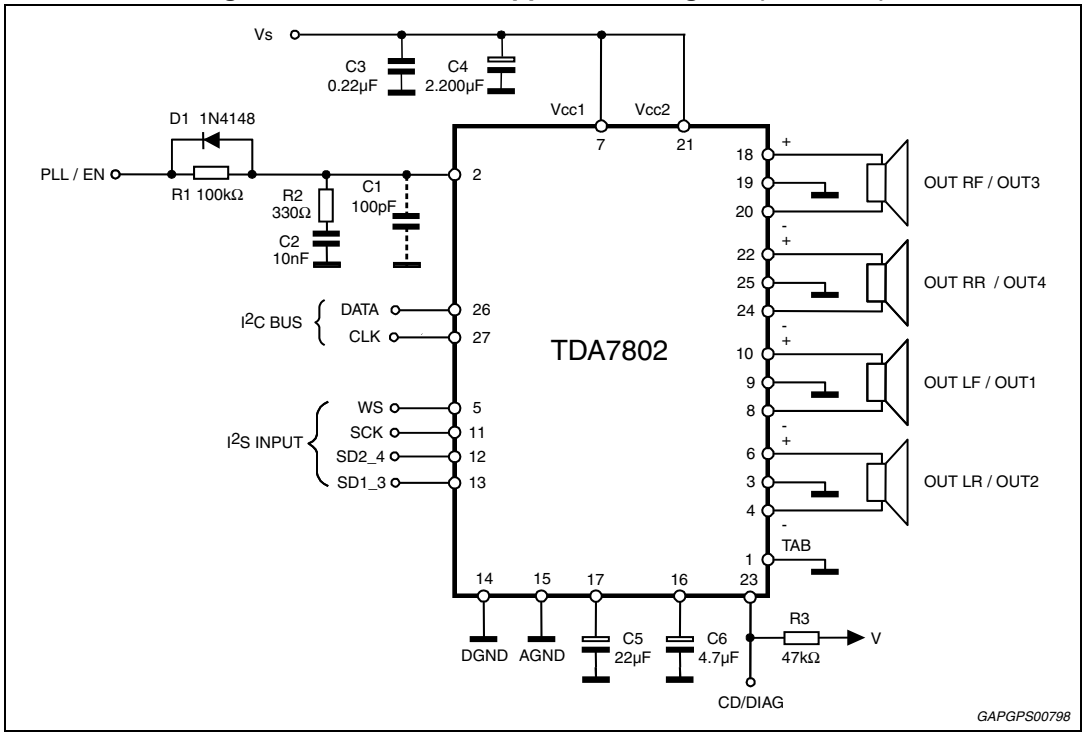


Figure 4. I²C bus mode application diagram (TDA7802PD)

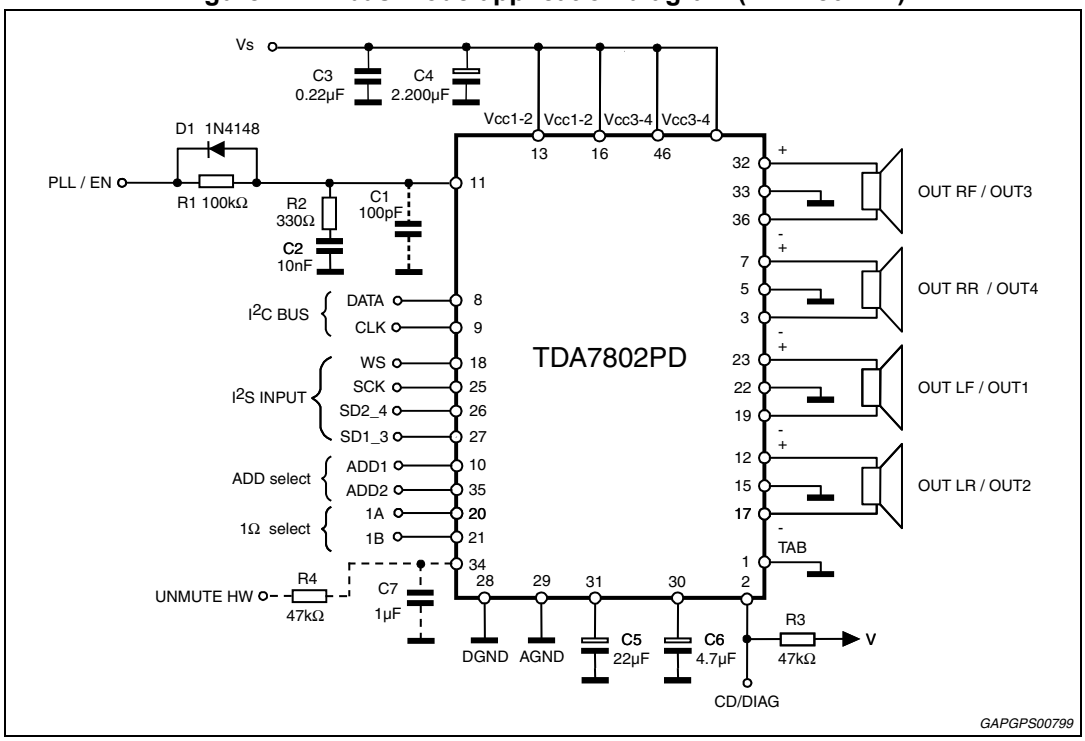


Figure 5. Legacy mode application diagram (TDA7802)

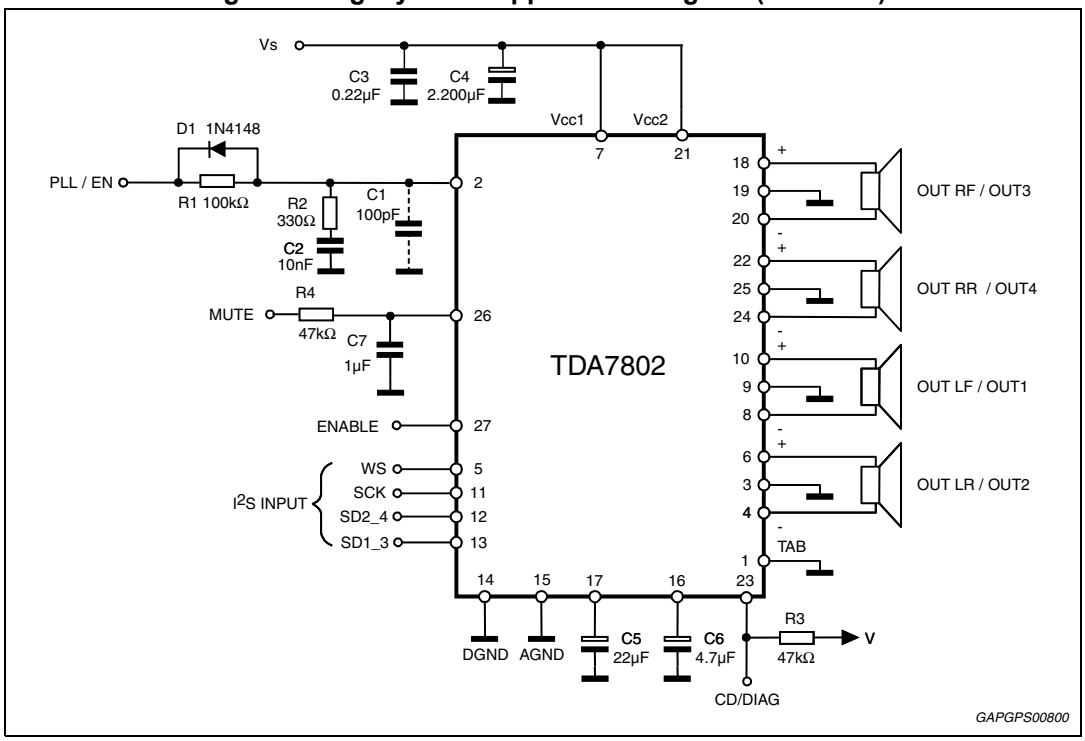
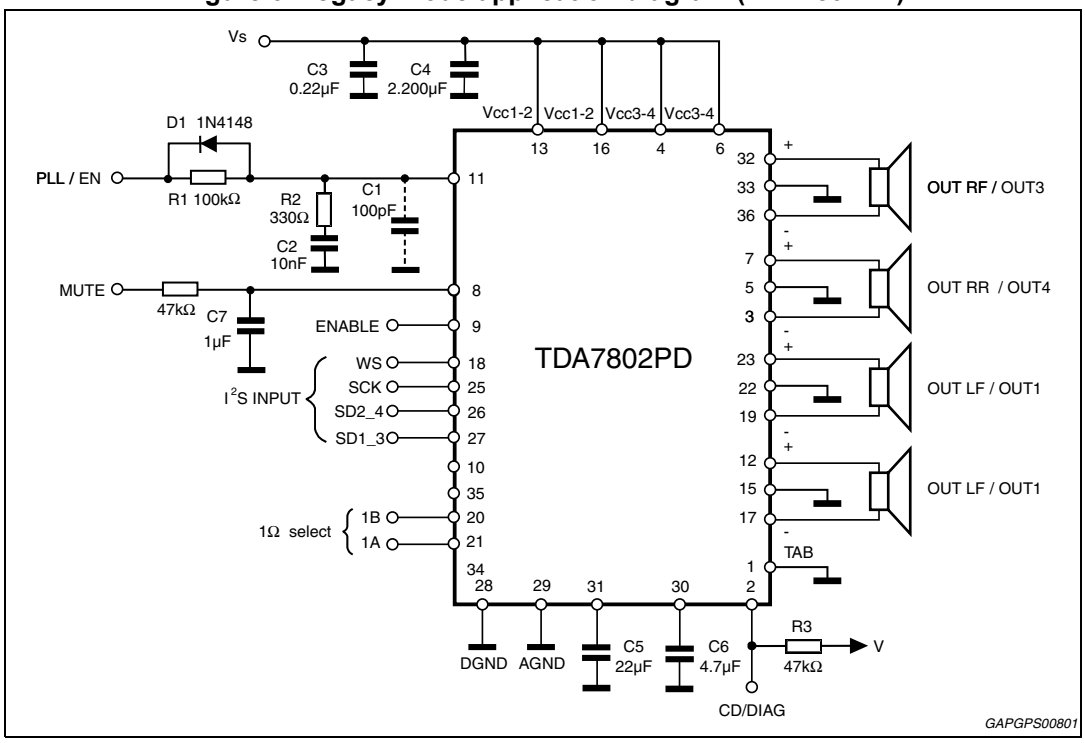


Figure 6. Legacy mode application diagram (TDA7802PD)



3 Electrical specification

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings(1)

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
V_{peak}	Transient supply voltage for t = 100 ms	-0.3 to 50	V
$V_{i2cdata}$	I^2C bus pins voltage/legacy mode mute	-0.3 to 5.5	V
V_{i2cClk}	I^2C bus pins voltage/enable legacy mode	-0.3 to Max (V_{CC}, 50V)	V
V_{i2s}	I^2S bus pins voltage	-0.3 to 3.6	V
V_{unmute}	Unmute hardware voltage (PSO36 only)	-0.3 to 3.6	V
V_{cd}	CD/Diag pin voltage	-0.3 to 20	V
V_{load12}	LOAD (Parallel mode) selection	-0.3 to 3.6	V
I_O	Output peak current (repetitive f > 10 Hz)	internally limited	A
P_{tot}	Power dissipation T_{case} = 70 °C	85	W
T_{stg}, T_j	Storage and junction temperature	–55 to 150	°C
T_{amb}	Operative temperature range(2)	-40 to 105	°C
C_{max}	Maximum capacitor vs. ground connected to the output	10	nF
ESD_{HBM}	ESD protection HBM (3)	2000	V
ESD_{CDM}	ESD protection CDM (3)	500	V

1. Absolute maximum rating for pin not specified in the table is 3.6 V.
2. A suitable heatsink/dissipation system should be used to keep T_j inside the specified limits.
3. Conforming to ESD standards.

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter		PowerSO36	Flexiwatt 27	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	Max	1	1	°C/W

3.3 Electrical characteristics

Referred to the test setup V_S = 14.4 V; R_L = 4 Ω; f = 1kHz; T_{amb} = 25 °C, SB-I mode, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage range	-	6		18	V
I_{SB}	Standby current	-	-	-	4	µA
I_d	Total quiescent drain current in amplifier mode	Enable on amplifier mode muted	160	235	310	mA
I_t	Total quiescent drain current in tristate mode	Enable on tristate mode	45	60	75	mA
I_{ovcur}	Over current protection	V_{CC} = 16 V, no signal	-	4.8	-	A
P_O	Output power	R_L = 4 Ω; max power	42	45	-	W
		THD = 10 %	26	29	-	W
		THD = 1 %	21	23	-	W
		R_L = 2 Ω; THD 10%	46	50	-	W
		R_L = 2 Ω; THD 1%	36	40	-	W
		R_L = 2 Ω; max power	73	77	-	W
THD_{SB}	Total harmonic distortion (Standard bridge)	P_O = 1 W to 10 W, f=1 kHz, G_{V1}	-	0.02	0.05	%
		P_O = 1 W to 10 W, f=10 kHz, G_{V1}	-	0.2	0.5	%
		R_L =100 Ω input=-10 dBFS, f = 1 kHz, $G_{V1,2,3,4}$	-	0.01	0.02	%
		R_L =1 Ω, f=1kHz, P = 24 W, G_{V1}	-	0.04	0.1	%
THD	Total harmonic distortion	P_O = 1 W to 10 W, f=1 kHz, G_{V1}	-	0.03	0.1	%
		R_L =1 Ω, f=1kHz, P = 24 W, G_{V1}	-	0.05	0.15	%
C_T	Cross talk	f = 1 kHz to 10 kHz	60	80	-	dB
G_{V1}	Voltage gain 1	Output voltage @ -10 dBFS	14.9	-	16.9	dB (V)
G_{V2}	Voltage gain 2		9.5	-	11.5	dB (V)
G_{V3}	Voltage gain 3		6.9	-	8.9	dB (V)
G_{V4}	Voltage gain 4		1.45	-	3.45	dB (V)
F_{SV1}	Full scale voltage G_{V1}	Output voltage @ 0 dBFS V_S = 18 V	12.7	-	-	Vrms
F_{SV2}	Full scale voltage G_{V2}	Output voltage @ 0 dBFS	6.7	-	8.4	Vrms
F_{SV3}	Full scale voltage G_{V3}	-	4.9	-	6.2	Vrms
F_{SV4}	Full scale voltage G_{V4}	-	2.65	-	3.35	Vrms
DG	Delta voltage gain 20 Hz – 20 kHz	P_o =1 W	-0.5	-	0.5	dB

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DR	Dynamic range $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw = 20 Hz to 20 kHz, un weighted	 105 100 100 98	 108 103 103 101	-	dB
E_{IN}	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw = 20 Hz to 20 kHz, un weighted	-	 30 30 21 21	 40 40 30 30	µV
SNR	Signal to noise ratio $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw = 20 Hz to 20 kHz, un weighted	 110 104 104 100	 113 107 107 103	-	dB
G_B	Gain balance	-	-1	-	4	dB
SVR	Supply voltage rejection	f = 1 kHz; V_r = 1 Vpk;	50	70	-	dB
A_M	Mute attenuation	-	80	-	-	dB
V_{OS}	Offset voltage	Mute and play	-50	-	50	mV
V_{AM}	Supply automute range	Above this voltage the device is in play	5.8	-	-	V
		Below this voltage the device is in mute	-	-	5	V
$V_{POWONRESET}$	Supply voltage of power-on reset	-	-	3.5	4.0	V
$V_{OVERVOLTAGE}$	Over voltage shut-down	-	18.5	-	22.5	V
V_{CDMOV}	CD/DIAG pin operative voltage	-	-	-	5	V
CD_{LK}	Clip det high leakage current	CD OFF	-	0	15	µA
CD_{SAT}	Clip det sat. voltage	CD on; I_{CD} = 1 mA	-	150	300	mV
$CD1_{THD}$	Clip det THD level 1 %	-	-	1	2	%
$CD2_{THD}$	Clip det THD level 5 %	-	3	5	7	%
$CD3_{THD}$	Clip det THD level 10 %	-	8	10	13	%

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{mute}	Mute and unmute commutation time	Programmable by I^2C bus register IB2(7:5) F_s = 44.1 kHz	-	1.45	-	ms
			-	6	-	
			-	12	-	
			-	24	-	
			-	48	-	
			-	93	-	
			-	186	-	
			-	370	-	
N_{GL}	Noise gating input level	Under this level the device is in mute	-	-102	-	dB
N_{GT}	Noise gating time	Fs = 44100	-	92	-	ms
E_{IN2}	Output noise voltage GV = GV1 GV = GV2 GV = GV3 GV = GV4	Bw = 20 Hz to 20 kHz, un weighted, noise gating off, No input signal	-	 56 53 40 30	-	µV
Turn on diagnostics speaker mode						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
P_{vs}	Short to V_s det. (above this limit, the output is considered in short circuit to V_S)	-	V_s - 1	-	-	V
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).	-	2	-	V_s - 2	V
Lsc	Shorted load det.	-	-	-	0.5	Ω
Lop	Normal load det.	-	1.5	-	25	Ω
Lnop	Open load det.	-	75	-	-	Ω
Turn-on diagnostic for 1 Ohm load configuration						
Lsc	Shorted load det.	-	-	-	0.25	Ω
Lop	Normal load det.	-	0.75	-	12.5	Ω
Lnop	Open load det.	-	37.5	-	-	Ω
Td	Max diagnostic time(1)	-	-	260	-	ms

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Rss	Soft short resistor	R_L=1.5 Ω and R_L=75 Ω for soft short to battery R_L=0.5 Ω and R_L=25 Ω for soft short to ground	500	-	-	Ω
Turn on diagnostics booster mode						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
Pvs	Short to V_s det. (above this limit, the output is considered in short circuit to V_s)	-	V_s - 1	-	-	V
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).	-	2	-	V_s - 2	V
Lsc	Shorted load det.	-	-	-	20	Ω
Lop	Normal load det.	-	0.06	-	1	kΩ
Lnop	Open load det.	-	3	-	-	kΩ
Rss	Soft Short Resistor	R_L= 60 Ω and R_L=1000 Ω	5.8(2)	-	-	kΩ
AC-diagnostic						
$I_{ACTRESH}$	AC diagnostic current threshold	IB4 – D4= ‘0’	250	375	500	mA
		IB4 – D4= ‘1’	125	187	250	mA
Permanent diagnostics						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	Power amplifier in Mute or Play, one or more short circuits protection activated	-	-	1	V
Pvs	Short to V_s det. (above this limit, the Output is considered in short circuit to V_s)	-	V_s - 1	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults)	-	2	-	V_s - 2	V
L_{SC}	Shorted load det.	1 Ohm	-	-	0.25	Ω
		Speaker mode	-	-	0.5	
		Booster mode	-	-	20	

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
L_{OP}	Normal load det.	1 Ohm	0.75	-	-	Ω
		Speaker	1.5	-	-	
		Booster	60	-	-	
V_O	Offset detection	Absolute value	1.5	-	2.5	V
T_{ph}	Thermal protection junction temperature	Gain attenuation of 60 dB	-	165	-	°C
T_{pl}		Gain attenuation of 0.5 dB	-	155	-	°C
T_{w1}	Thermal warning junction temperature	-	-	Tpl-10	-	°C
T_{w2}		-	-	Tpl-20	-	°C
T_{w3}		-	-	Tpl-35	-	°C
T_{w4}		-	-	Tpl-55	-	°C
Legacy mode						
$V_{LEGMUTEMOV}$	Legacy mode mute pin operative voltage	-	-	-	3.3	V
V_{LM_MUTE}	Legacy mode mute threshold	Gain attenuation of 80 dB	-	-	1.2	V
		Gain attenuation of 0.1 dB	2.6	-	-	V
$V_{LEGONMOV}$	Legacy mode ON pin operative voltage	V_{CC} = 14.4 V	-	-	14.4	V
V_{LM_ON}	Legacy mode threshold	Device in legacy mode	Vs-2	-	Vs	V
I^2C bus interface						
V_{I2CMOV}	I2C pin operative voltage	-	-	-	3.3	V
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	0.8	V
V_{IH}	Input high voltage	-	1.3	-	-	V
PII-filter /ENABLE pin						
V_{ILENB}	Input low voltage	-	-		1.5	V
V_{IHENB}	Input high voltage	-	2.3	-	-	V
I_{ILENB}	Logic ‘0’ output current	V_{IN} = 0.45 V	-	-	2	µA
I_{IHENB}	Logic ‘1’ input current	V_{IN} = 2.3 V (IB0 D4=0)	-	-	2	µA
I^2S pin						
V_{I2SMOV}	I2S pin operative voltage	-	-	-	3.3	V
V_{IL-I2S}	Input low voltage	-	-	-	0.8	V
V_{IH-I2S}	Input high voltage	-	1.3	-	-	V
I_{IH}	Input low current	@ V_I = 3.3 V	-	-	5	µA
I_{IL}	Input high current	@ V_I = 0 V	-	-	5	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Unmute hardware (pin 34)						
V_{HWMMOV}	HW mute pin operative voltage	-	-	-	3.3	V
V_{HW_UNMUTE}	Hardware unmute threshold (POSO36 only)	Gain attenuation of 80 dB	-	-	1.2	V
		Gain attenuation of 0.1 dB	2.6	-	-	V
I_{UNMUTE}	Input low current	absolute@ V_I = 3.3 V	-	-	5	µA
	Input high current	absolute@ V_I = 0 V	-	-	5	µA
Address and load selection pin (optional for PowerSO36 package only)						
$V_{LOADMOV}$	LOAD pins operative voltage	-	-	-	3.3	V
V_{LOAD}	Load 1 Ohm threshold	-	-	-	2	V
I_{LOAD}	Input LOAD current	absolute@ V_I = 3.3 V	-	-	50	µA
V_{ADD}	Add threshold	-	1	-	-	V
I_{ADD}	Input ADD current	absolute@ V_I = 0 V	-	-	50	µA

1. For the diagnostic timings information refer to the *Table 7*.
2. The values are the ones that guarantee the correct working of the diagnostic. Since the value is strongly dependable from the loudspeaker, we decided to target the values for the limits of open load and short load diagnostic.

3.4 Electrical characteristics typical curves

Figure 7. Quiescent current vs. supply voltage

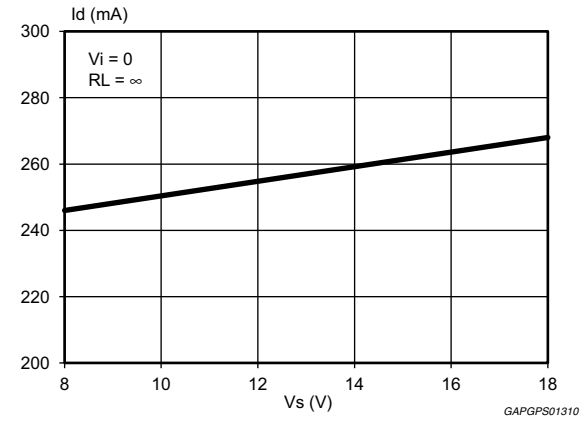


Figure 8. Output power vs. supply voltage (4 Ω)

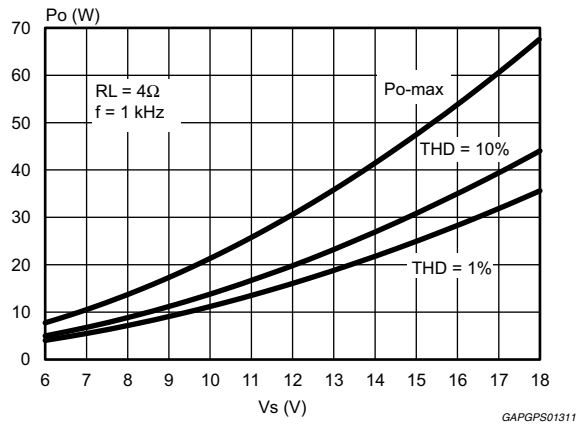


Figure 9. Output power vs. supply voltage (2 Ω)

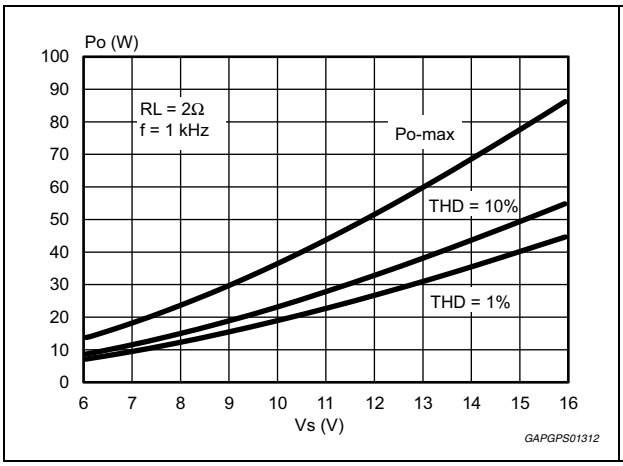


Figure 10. Distortion vs. output power (4 Ω, STD mode)

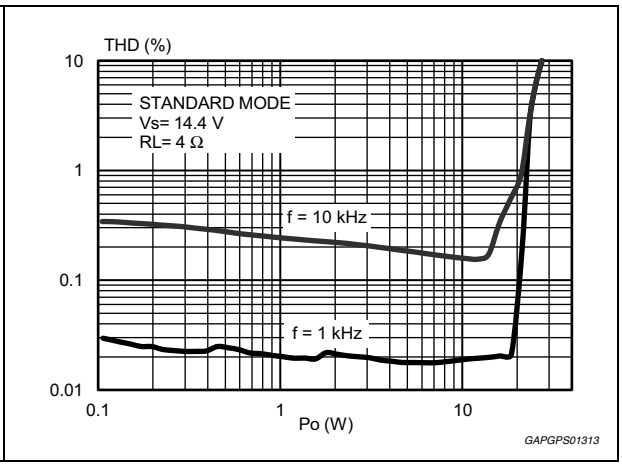


Figure 11. Distortion vs. output power (4 Ω, HI-EFF mode)

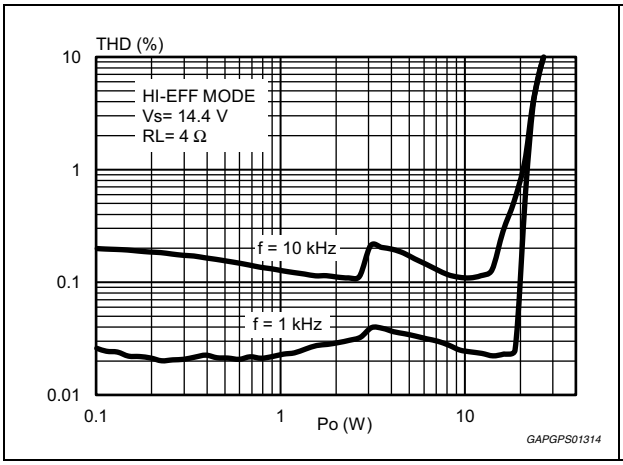


Figure 12. Distortion vs. output power (2 Ω, STD mode)

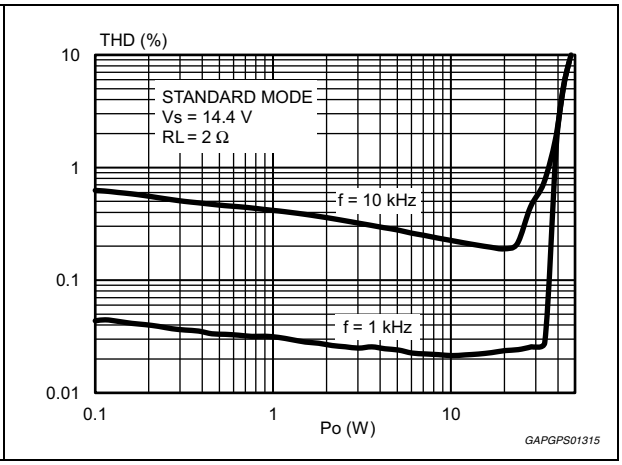


Figure 13. Distortion vs. output power (2 Ω, HI-EFF mode)

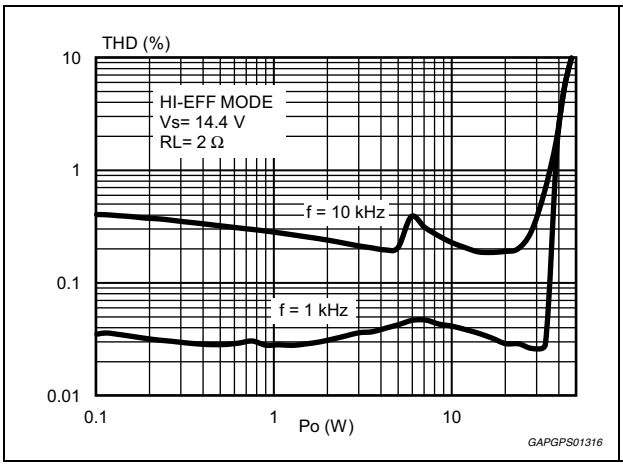


Figure 14. Distortion vs. frequency (4 Ω, STD mode)

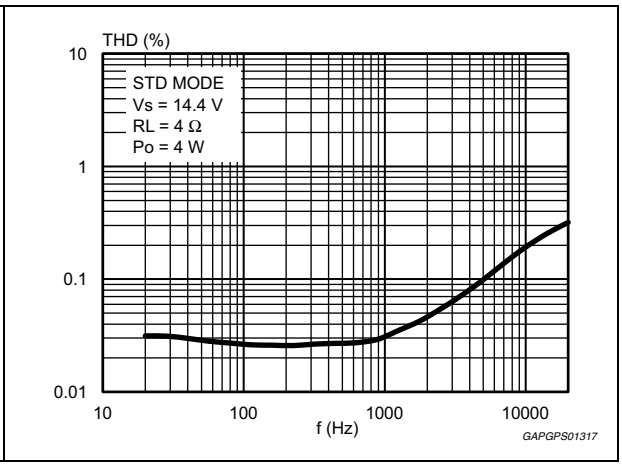


Figure 15. Distortion vs. frequency (2 Ω, STD mode)

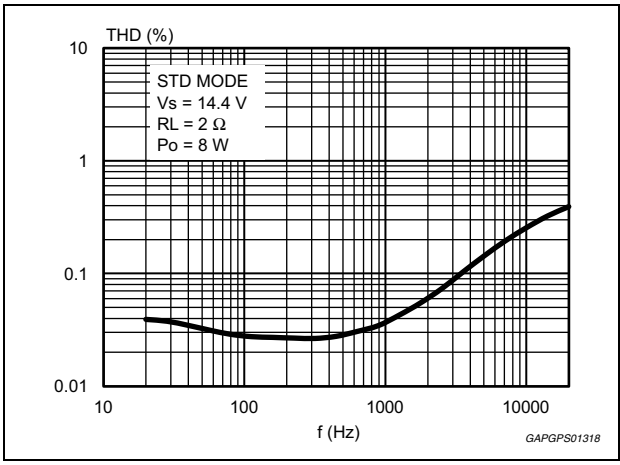


Figure 16. Distortion vs. output power (4 Ω, Vs = 6 V)

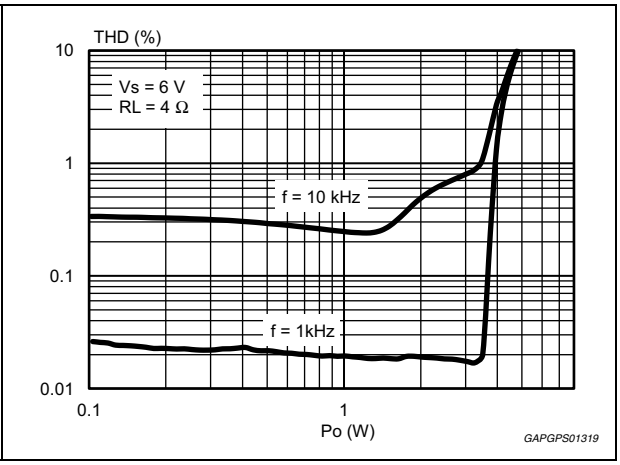


Figure 17. Distortion vs. output power (4 Ω, Vs = 6 V)

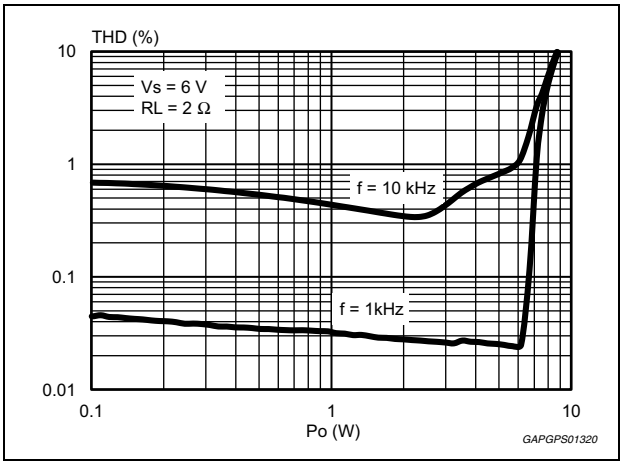


Figure 18. Vo vs. Vin (Gv1-2-3-4 settings)

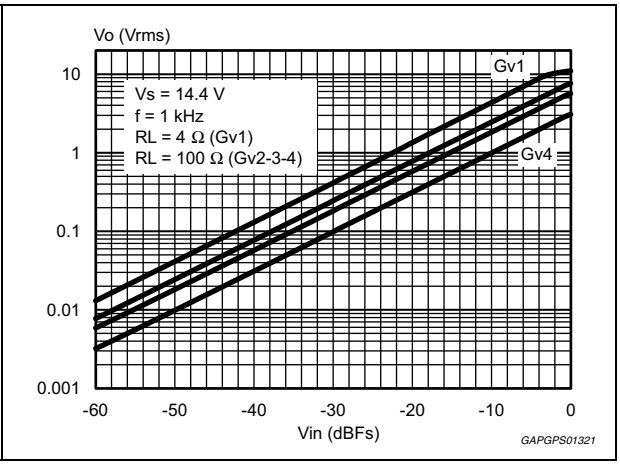


Figure 19. Vo vs. Vin (Gv1-2-3-4 settings + 6 dB dig. gain)

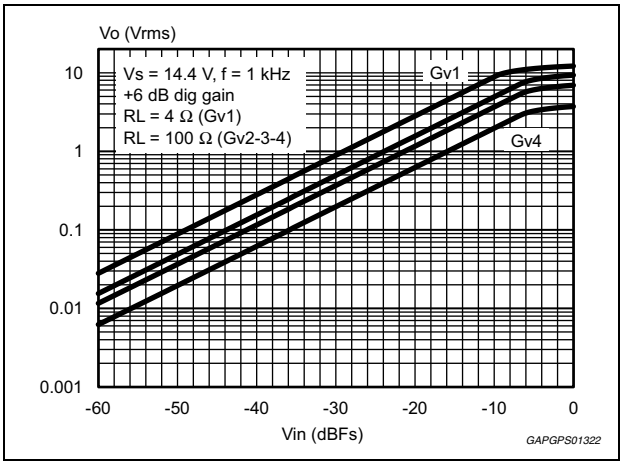


Figure 20. Distortion vs. output voltage (LD-Gv2)

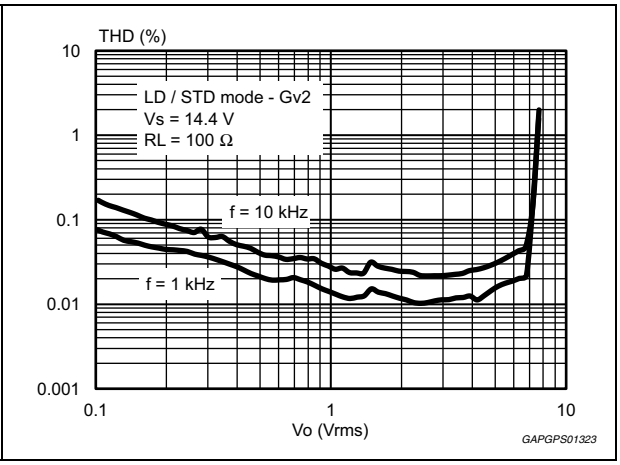


Figure 21. Distortion vs. output voltage (LD-Gv3)

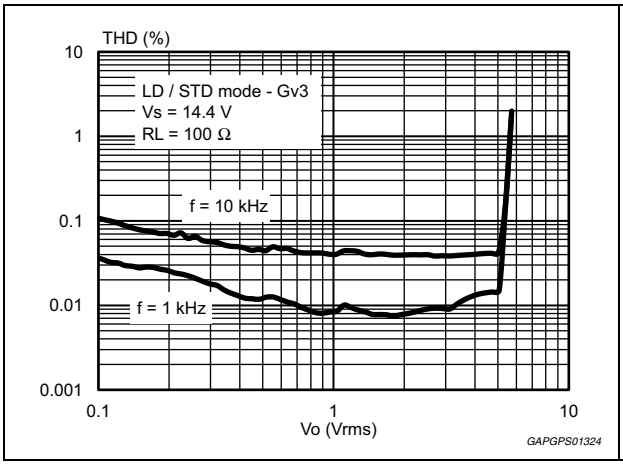


Figure 22. Distortion vs. output voltage (LD-Gv4)

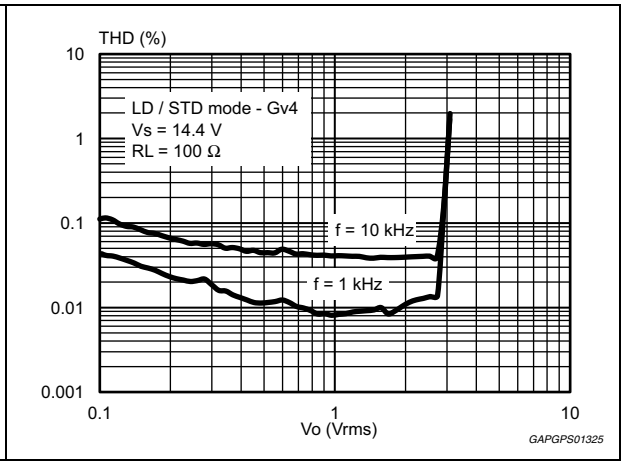


Figure 23. Output attenuation vs. Vs (normal & start-stop mode)

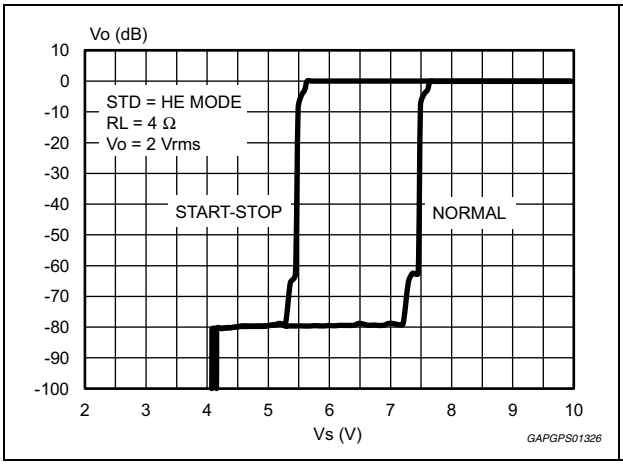


Figure 24. Crosstalk vs. frequency (STD mode)

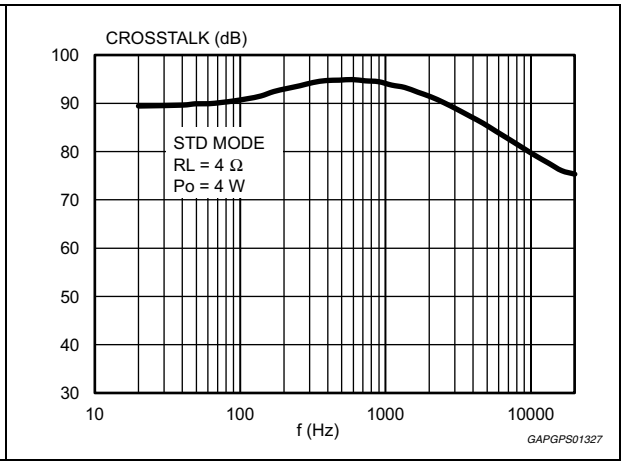


Figure 25. Crosstalk vs. frequency (HI-EFF mode)

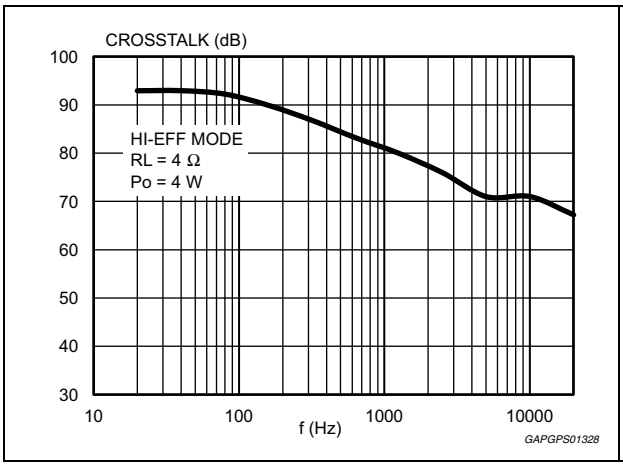


Figure 26. Supply voltage rejection vs. frequency

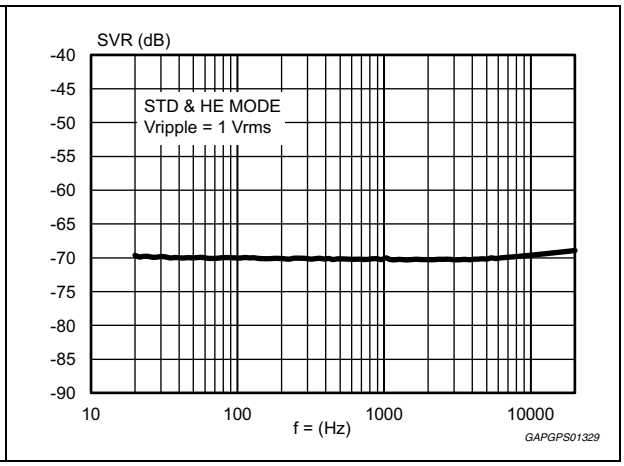


Figure 27. Total power dissipation & efficiency vs. Po (4 W, STD, Sine)

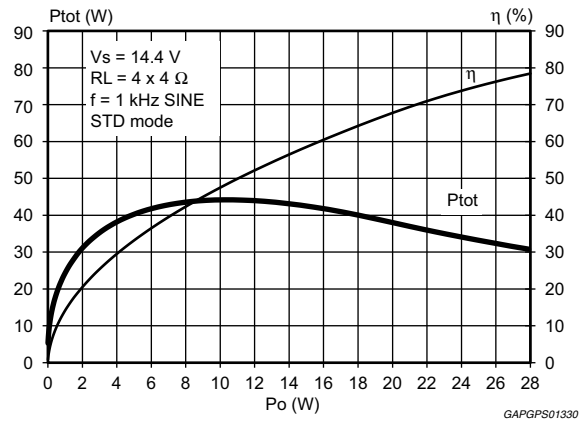


Figure 28. Total power dissipation & efficiency vs. Po (4 W, HE, Sine)

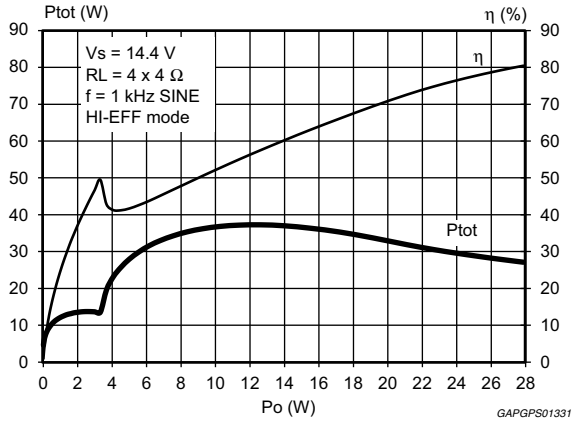


Figure 29. Total power dissipation & efficiency vs. Po (2 W, HE, Sine)

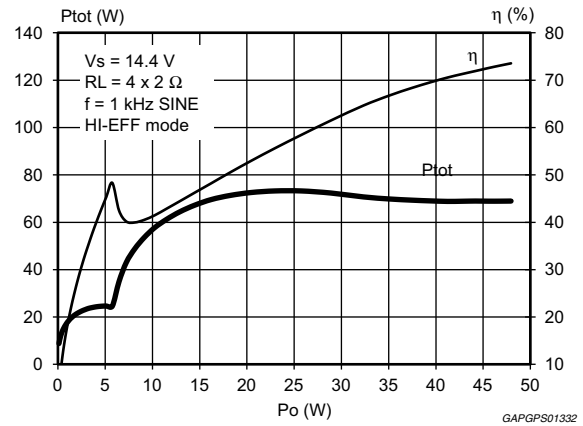


Figure 30. Power dissipation vs. average Po (audio program simulation, 4 Ω)

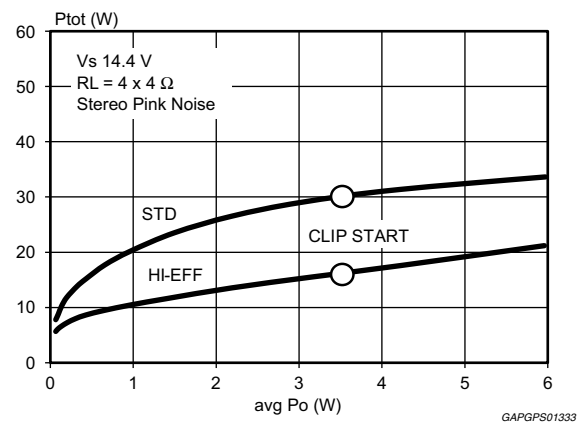


Figure 31. Power dissipation vs. average Po (audio program simulation, 2 Ω)

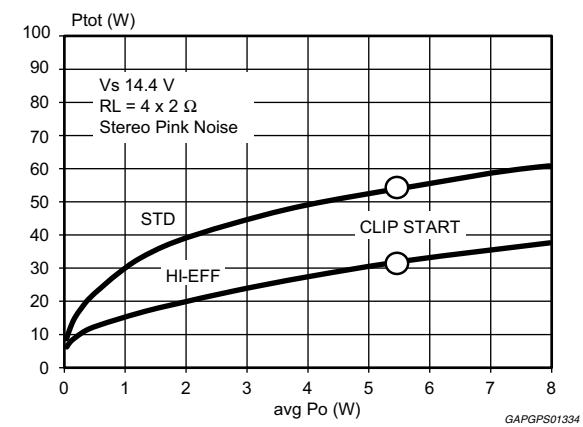
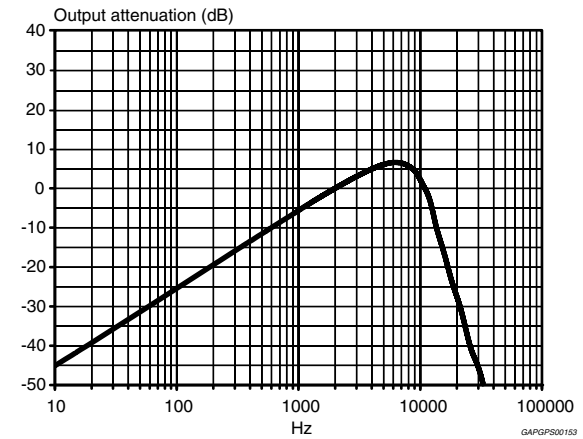


Figure 32. ITU R-ARM frequency response, weighting filter for transient pop



4 Operation mode

There are six main operation modes:

- Standby
- Low quiescent current
- Legacy
- I^2C amplifier
- Diagnostic
- Fault restart

The *Figure 33* in the next page shows state's diagram of TDA7802.

4.1 Standby

When the PLLen pin is below VILENB the amplifier is in standby mode and the current consumption is ISB.

4.2 Low quiescent current

When PLLen pin is above the VILENB and SCL is below VLM_ON (Legacy Mode threshold), only some internal circuitry is turned on, the "Short Circuit Protection" is on, the digital core is ready to work, the PLL is toggling.

Under these conditions, the amplifier is ready to receive instructions from the microcontroller or the legacy mode can be set.

4.3 Legacy

When PLLen pin is above the VILENB and the SCLlen pin is raised above VLM_ON, legacy mode is activated. The I^2C bus is not longer accessible, and the I^2C bytes will be set to default value. Pin SDAlm acts as hardware unmute pin in legacy mode.

4.4 I^2C amplifier

When PLLen pin is above the VILENB and the IB5 D0 = '1', the device is ready to play. This means that the final power stage are on and the output are raised to Vs/2 Volt. The consumption is ID when still muted. Please remember the amplifier is muted by default, and then mute disable instructions (IB2-D4, D3) need to be sent. An hardware unmute pin is available in PSO36 only (pin 34).

4.5 Diagnostic

A single channel can be in diagnostic mode when IB4-D0 is '1' and PLLen pin is above the VILENB. When the diagnostic bit is activated before the I^2C Amplifier Mode is active (IB5 D0 = '1'), the turn-on diagnostic is performed for all channels. Otherwise, when the bit is activated after the amplifier mode command, and an over current is detected, the run-time diagnostic will occur for the channel where the over current has been detected.

In both cases the output power stages are switched off and only part of them are kept on, in order either to detect the possible misconnections correctly or to make the amplifier restart in case of false detection. The I^2C registers data are updated and can be read (see *Section 7.2* and *7.3* for more details).

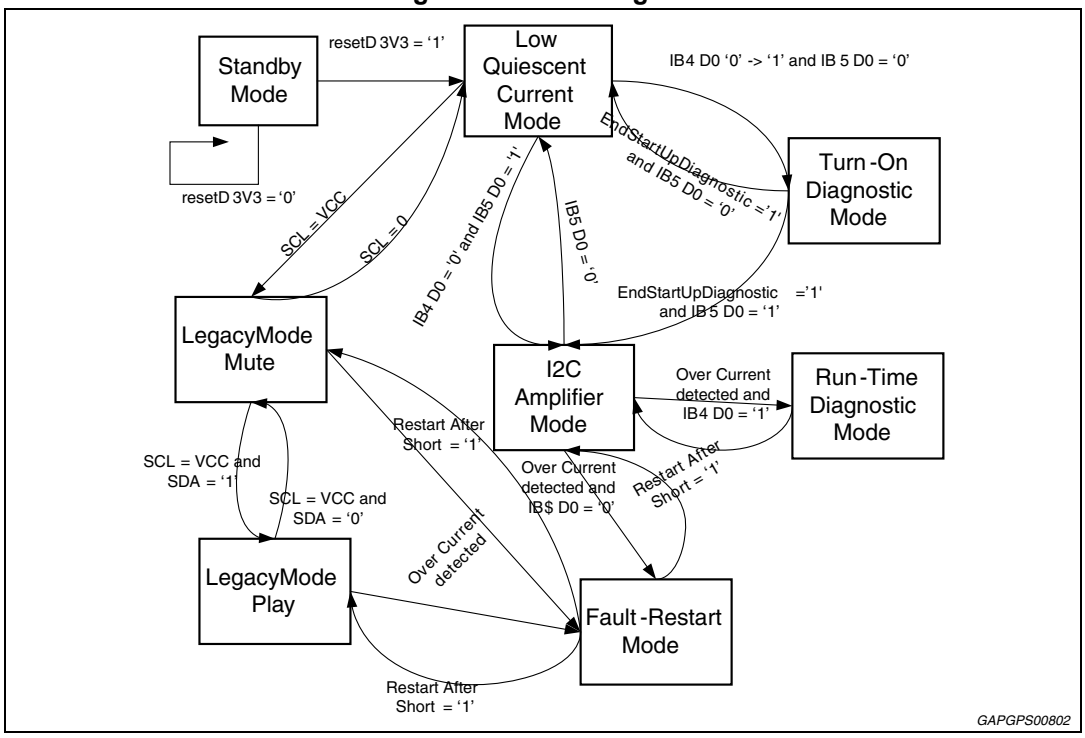
4.6 Fault restart

The amplifier can be in this state after an over current is detected while is in I^2C Amplifier mode (a) or in Legacy mode (b):

a) If IB4-D0 is '0' at the over current event, the amplifier's states will follow the sequence: I2C Amplifier Mode -> Fault Restart Mode. If IB4-D0 is '1' the states will follow this sequence: I2C Amplifier Mode -> Fault Restart Mode -> (if the fault is still present) Diagnostic Mode -> (if the fault is still present) Fault Restart Mode. In both cases, part of the output power is switched off according with IB4-D2/D1.

b) The amplifier state will change from Legacy Mode to Fault Restart Mode. Also in this case part of the output power will be switched off.

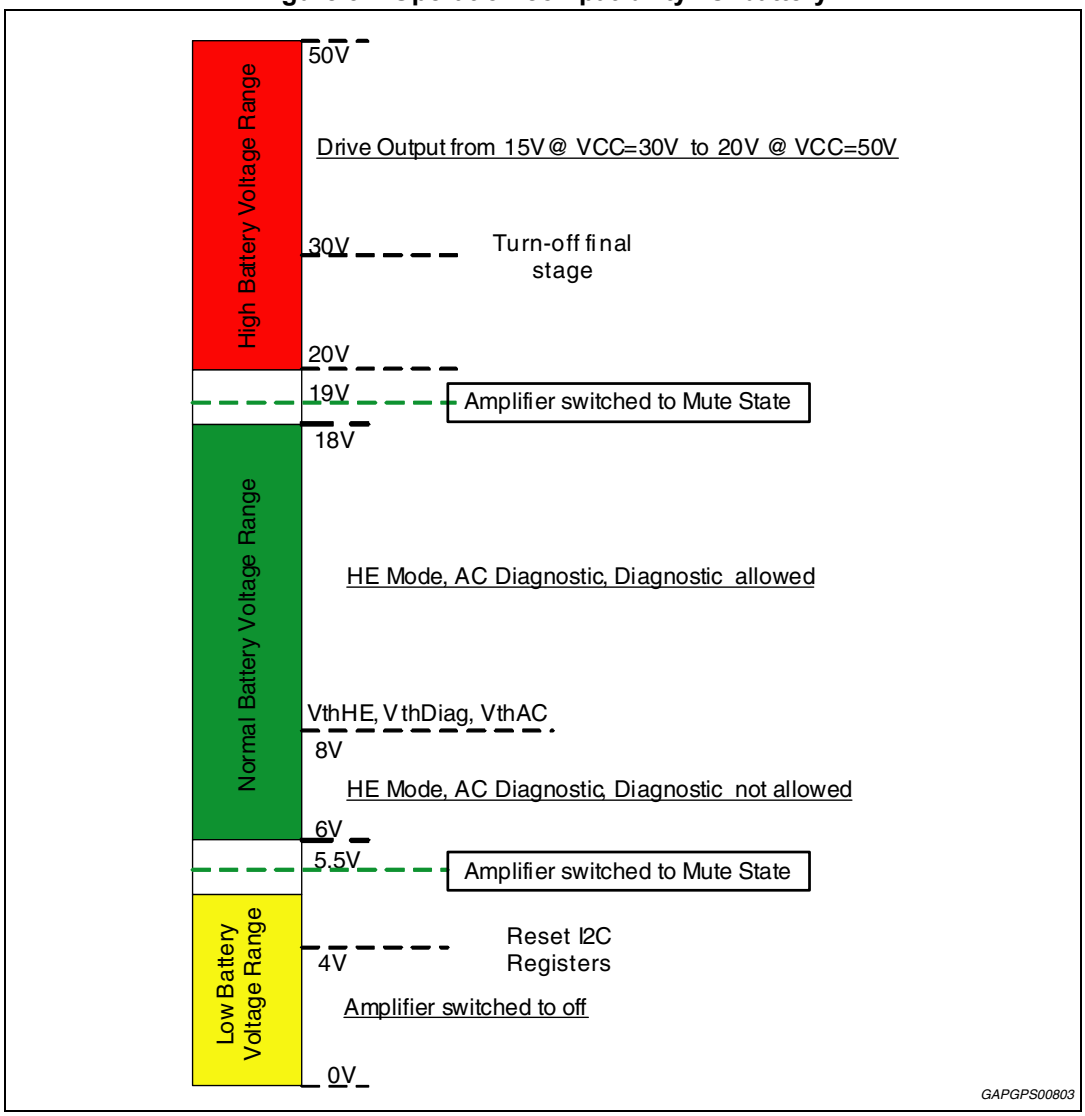
Figure 33. State diagram



5 Operation compatibility vs. battery

Here below the operation compatibility vs. the battery value is shown. For each battery voltage range, only a limited number of functions are available as it is shown below:

Figure 34. Operation compatibility vs. battery



6 "PLLen" pin description

The PLLen pin has the two shared functions:

- Enable
- PLL filter

PLLen pin works as ENABLE when it has the logic level "low": in this case the IC is in standby mode and the current consumption is the lowest possible (ISB).

The amplifier is waken-up once PLLen is raised to the logic level "high" and it goes in the low quiescent mode. The information that the transition from standby mode to low quiescent current mode happened is written in DB0 D7. This is possible because the power on reset of the digital part is triggered and the TDA7802 is able to receive any instructions.

At this point PLLen, unless it is externally pulled down below 1.75 V, works as PLL filter and then it is forced from the TDA7802 to have a precise value between 2 and 3 Volt. This value is the one that allows the VCO toggling at the system frequency, and it is reached in a time depending from the PLL loop filter (about 100-150 µs in the suggested configuration).

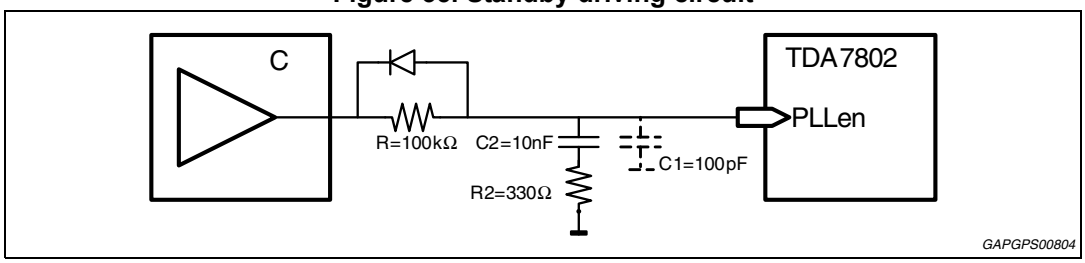
To avoid interfering with the PLL's functionality when IB3 D2 is set to '1', (therefore with I^2S of 50 bit), after DB0 D7 = "1" the output of the microcontroller or microprocessor that drives the PLLen pin must be set in tristate. This last information is also available on CDdiag until the TDA7802 moves into a different state (I^2C Amplifier mode or Legacy mode play).

During IC amplifier mode or legacy mode, it is possible to force the PLLen pin to low level. Before the device is back to the standby mode there is a fast-mute transition due to the PLL unlock (~ 2ms). The PLL will try to force the voltage of the pin PLLen by sourcing a current IILENB.

6.1 "PLLen" driving

The Figure 3 shows the applicative schematic to drive correctly the PLLen pin. TDA7802 is supposed be driven from a C or DSP.

Figure 35. Standby driving circuit



C2, C1 and R2 the external components of the PLL's loop filter; further filtering is internally integrated. The diode 1N4848 let to force the PLLen pin to logic level low and allows the TDA7802 to force the pin voltage level when it is in low quiescent current mode. During the transition amplifier/legacy mode -> standby mode, TDA7802 tries to force the voltage on PLLen pin by sourcing a current. The former current will forward bias the diode. The buffer input resistance has to be as small as the pin is carried below V_{ILENB}.

When I^2S with 50 bit is used, IB3-D2 set to '1', the C1 capacitor of 100 pF should be added. Otherwise it should not be connected.

7 Functional description

7.1 Voltage regulators timing

Pins D3V3 and A3V3 are respectively the digital and analog internal regulators. The D3V3 rises right after the PLLen pin is at the logical value "1" and its rising time depends from the filter capacitor; the value suggested for this filter is of min 4.7 µF.

The A3V3 rises after any command that moves the amplifier from low quiescent current mode; the rising time depends from the combined effect of the external capacitor on the pin and of an internal 2 ms ramp: if the capacitor value is 22 µF or lower, the internal ramp effect is dominant and the rising time will be about 2 ms. On other hand, when the capacitor has an higher value, the rise time will be higher as well. The suggested value for this capacitor is 22 µF (47 µF) at least.

7.2 Turn-on diagnostic description

The turn-on diagnostic is triggered on the rising edge of bit IB4 D0 when IB5 D0 is "0". This happens when the amplifier is in low quiescent current mode and the Legacy mode is not active. It is possible to run one or more turn-on diagnostic sequences according the following procedure:

1. wait the previous cycle is over
2. read the data bytes DB1,DB2,DB3 and DB4

Please note that all these instructions must be sent while the amplifier is still in low quiescent current (IB5 D0 = "0"), otherwise they won't be executed.

Turn-on diagnostic does not start if V_{CC} is below 8 V or one of the muting condition is present, (low battery mute, high voltage mute, PLL-unlock mute, thermal mute, hardware pin mute).

Note: The diagnostic enable bit (IB4 D0) must be set before the amplifier mode bit (IB5 D0).

DB1, DB2, DB3 must be read before DB4 (after DB4 is read the DB1-2-3-4 are reset).

The detected faults are here described:

Soft Short to GND: it detected the presence of a resistor (see *Table 6* in “Turn-on diagnostic” section) connected between an output and ground, whose effect could give a wrong open load or short across load diagnostic's result (causing an anomalous current consumption in some cases).

Soft Short to VS: it detects he presence of a resistor (see *Table 6* in “Turn-on diagnostic” section) connected between an output and battery, whose effect could give a wrong open load or short across load diagnostic's result (causing an anomalous current consumption in some cases).

Short to GND: it detects the hard connection between an output and ground. The value of the short is able to pull the output between 1.5 V and ground.

Short to VS: it detects the hard connection between an output and battery. The value of the short is able to pull the output between (battery - 1.5 V) and battery.

Short across the speaker: it detects the hard connection across the speaker that is below a certain value. This value guarantees that the IC is able to drive the lowest speaker written in this data sheet.

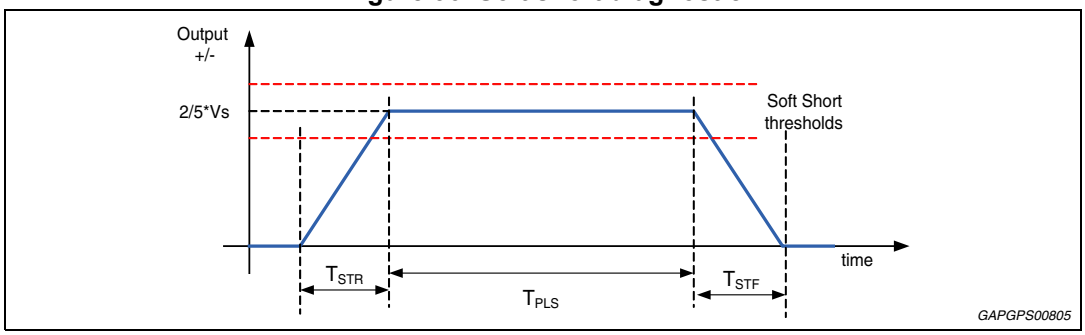
Open Load: it detects the missing of the speaker's connection.

The diagnostic's results are updated into the data bytes DB1, DB2, DB3 and DB4 (one for each channel) after the diagnostic is over.

The flow of the diagnostic includes some steps as described below.

- During the first part, the soft-short evaluation is performed. The outputs and an internal reference line are pulled up to a voltage of 2/5*Vbattery in a time TSTR and then compared for a time TPLS. During the plateau time, the comparator outputs are read from the digital part. The outputs are then pulled down to zero (see *Figure 36*). The A3V3 supply is 0V and the output stage is in tri-state during this phase.

Figure 36. Soft short diagnostic



- If a soft short is detected, the short to GND/VCC evaluation follows. Pin A3V3 goes up as the amplifier stage is turned on; the power and the outputs are risen up to 1/2*$V_{battery}$ and then compared to ($V_{battery}$ - 1.5 V) and 1.5 V for a time TPLS. At the end of the plateau (TPLS) output and A3V3 go back to 0V and the results obtained are written into the I^2C Bus registers once the diagnostic is over.

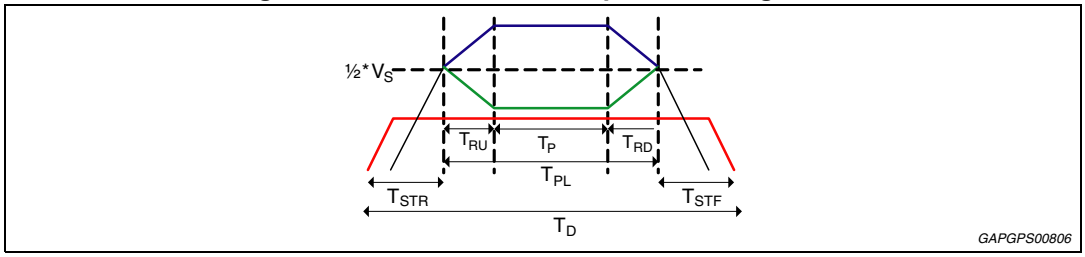
In case the short to VCC or GND is detected during this phase a '1' is written in DBx-D1/D0 (VCC/GND) but not in DBx-D6. In case the hard short is not detected a '1' is written all DBx-D1/D0 and DBx-D6.

The turn-on diagnostic is then completed and the amplifier is goes back to the low quiescent current mode.

- However, if a soft short is not detected, it means that no Short to VS/GND are present as well, and don't need to be checked. In this case, short across the speaker and the open load evaluation can be performed. Pin A3V3 goes up as the amplifier stage is turned on and the outputs are risen up to 1/2*$V_{battery}$. A first pulse for "Short load detection" is done: exploiting the presence of a D/A converter, a subsonic (inaudible) voltage pulse is digitally and internally generated and converted. The pulse amplitude increasing is stopped when the current flowing through the speaker $I_{speaker}$ is the same of a prefixed one I_{high} (high current) or because it reaches the maximum value permitted. Since the differential output voltage V_o is well known, it is possible to keep monitored the value of the connected speaker during the transition and plateau. If Ispeaker reaches high then, when V_o< V_{short} (short circuit threshold) the result is short load (DBx - D3 ='1'), otherwise it is normal load (DBx - D3 = '0'); when $I_{speaker}$ does not reach I_{high} the turn-on diagnostic is not completed yet because the result could be still normal or open load.
- This is called "Open load detection". If IB4 D1/D2 = 1 the power DMOS need to be changed again: the outputs are pulled down to zero, the DMOS are switched and then the outputs raised up to 1/2*$V_{battery}$ again. This sequence is done in order to avoid any pop noise during the power set. The procedure is the same of the previous case

afterwords or in case of IB4 (D1/D2) = 0. The pulse amplitude is stopped when the current flowing through the speaker $I_{speaker}$ is the same of prefixed one I_{low} (low current) or because it reaches the maximum value permitted. When $I_{speaker}$ reaches the value I_{low} and $V_o < V_{open}$ (open load threshold) it's mean that the speaker is a normal load (DBx-D2='0'). In all other case the result will be open load (DBx-D2='1') (see *Figure 37*).

Figure 37. Short circuit and open load diagnostic

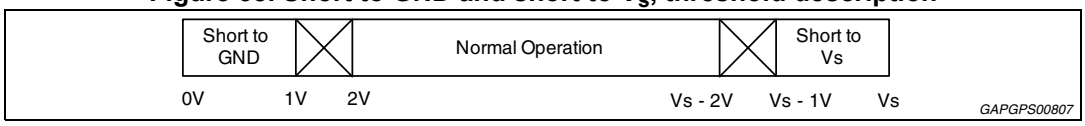


The whole diagnostic time depends from the number of pulses that are done. At least two pulses are done, but they could be three in case of open load. The values insert into the *Table 7*, are calculated basing on Fs = 48000 Hz.

In all the cases the fault is sent out to the registers only if it is stable throughout the whole plateau's period. If this does not happen any misconnection (Soft-short, Short to VCC/GND, Short Across or Open Load) are not reported. The faults for the turn-on diagnostic are written in DB (1, 2, 3, 4) (D1, D2, D3, D4) (a byte for each channel and a bit for each fault). They are consistent if DB0 D6 = "1". After a reading the data byte are reset.

The fault-detection thresholds for short to GND/ Vs remain unchanged independently from the gain setting. They are as in *Figure 38*.

Figure 38. Short to GND and short to V_S, threshold description



Concerning the short across the speaker / open speaker, the threshold changes from booster mode and speaker mode diagnostic setting, as load expected are pretty different (either normal speaker's impedance or high impedance). Speaker or booster mode are selectable from IB4 D2 for channels 1 and 3 and IB4 D1 for channel 2 and 4. The values in case of speaker mode are as in *Figure 39*. The same thresholds will change as in *Figure 40*, if booster mode diagnostic is selected.

Figure 39. Short across the speaker and open load threshold description, in speaker/amplifier mode

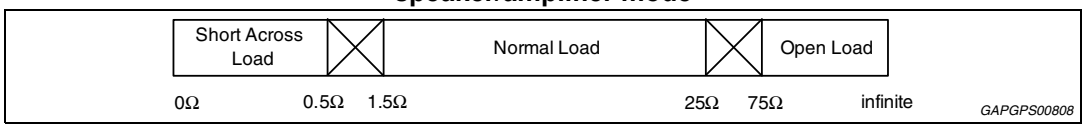


Figure 40. Short across the speaker and open load threshold description, booster/line driver mode

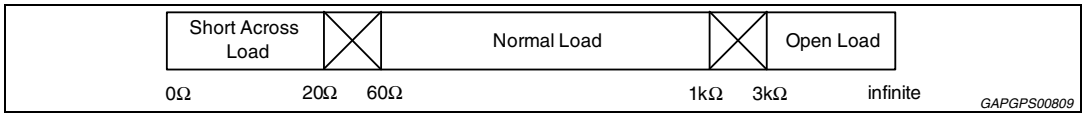


Table 7. Start-up pulse typical timings (F_s = 48 kHz)

Symbol	Parameter	Min	Typ	Max	Unit	Note
T_{STR}	Time to rise the outputs from 0V to a certain battery's percentage	-	10 (+ 10)	-	ms	When A3V3 goes up, the number in the bracket has to be added
T_{STF}	Time to rise the outputs from a certain battery's percentage to 0V	-	10 (+ 10)	-	ms	When A3V3 goes down, the number in the bracket has to be added
T_{PLS}	Plateau time for soft-short and short to VCC/GND diagnostic	-	80	-	ms	This time does not depend from the load and is not stretchable setting bits IB1-D6/D5
T_P	Plateau time for short circuit or open load diagnostic detection phase	-	80 (1)	-	ms	T_P = 86 ms · X when 140 ms - 2 ·T_{RU} > 80 ms
						T_P = (140 ms - 2·T_{RU}) · X when 140 ms - 2 ·T_{RU} < 80 ms
T_{PL}	Pulse time for short circuit or open load diagnostic detection phase	-	120	122.4(2)	ms	T_P = (2·T_{RU} + T_P) · X
X	Multiplier factor in case of diagnostic active	-	1,2,4,8	-	-	IB1-D6/D5 settings
T_{RU}=T_{RD}	Ramp-up and ramp-down diagnostic pulse's time	-	14 (3)	-	ms	2 ohm case
		-	20 (3)	-	ms	4 ohm case
T_{SS}	Soft-short diagnostic time	-	100	-	ms	Output rising time + Output falling time + plateau time (no A3V3)
T_{HS}	Short to VCC and GND diagnostic time	-	120	-	ms	A3V3 rising and falling time (10 ms x2) + Output rising and falling time + plateau time
T_D	Short load and open load diagnostic time	-	148	-	ms	2 ohm case (X=1)
		-	160	-	ms	4 ohm case (X=1)
T_{tot}	Total diagnostic time	-	260	-	ms	4 ohm load and no faults (T_{tot} = T_{SS} + T_D)
		-	220	-	ms	Hard or soft short to supplies (T_{tot} = T_{SS} + T_{HS})
		-	420	-	ms	Open load (X = 1, IB4 (D1/D2) = 0) T_{tot} = T_{SS} + T_{D1} + T_{D2}
I_{high}	Test current for the short load pulse	-	200 40	-	mA	For speaker mode For booster mode
I_{low}	Test current for the open load pulse	-	40 2	-	mA	For speaker mode For booster mode

1. For typical loudspeaker of 2 and 4 ohm.
2. These numbers are obtained from simulations.
3. Typical values for 4 Ω and 2 Ω and zero offset. These numbers depend on the loudspeaker and also from the intrinsic offset of the amplifier. For 2 Ω loudspeaker, -30 mV offset and Fs = 48 kHz T_{RU} = 21.2 ms; for 4 Ω and same surrounding conditions T_{RU} = 22.1 ms. Under these conditions T_{PL} = 122.4 ms for 2 Ω and 124.4 for 4 Ω. For higher values the number are not reported here.

When the amplifier is biased and the IB4 D0 ="1", the permanent diagnostic is enabled. The turn-on diagnostic state is held until an over current event is triggered. When this happens, a new diagnostic cycle can start.

7.3 Permanent diagnostic

The detectable faults are (see table 5 for definitions):

- Short to GND
- Short to Vs
- Short across the speaker

Then following additional features are also provided:

- Output offset detection
- AC diagnostic

When an over current occurs, TDA7802 has two different cycles that could react with:

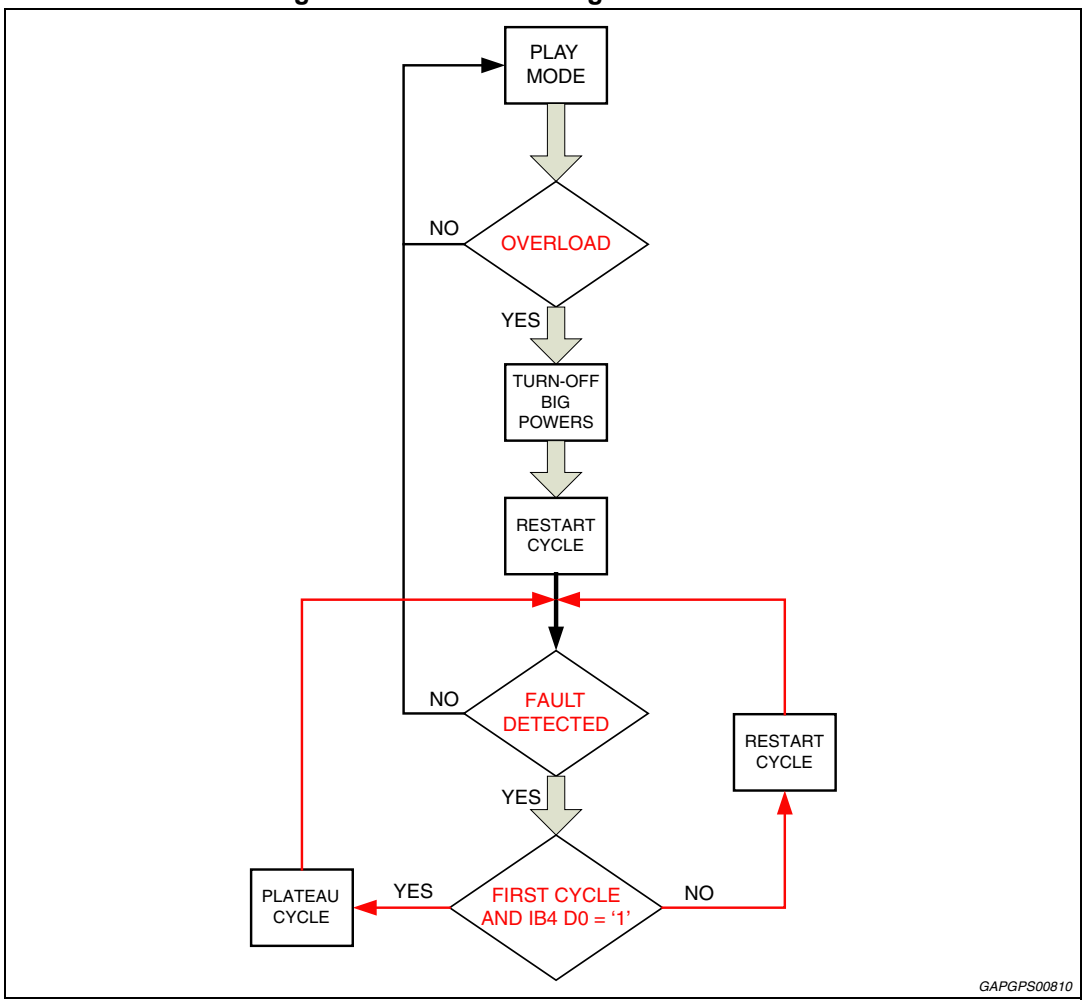
- Restart cycle: it is a 2 ms pulse. During this period a check of the output is performed.
- Plateau cycle: it is an 80 ms cycle. During this period a check of the outputs is performed and the results of diagnostic analysis are written into the I^2C bus.

TDA7802 has two different operating behaviors when an over current is detected:

- Restart mode, (IB4 D0 = "0"). The diagnostic is not enabled. Each audio channel operates independently from each other. If any of the above mentioned faults occurs, only the channel(s) where the fault happened is shut down. The diagnostic performs restart cycles every 2 ms until the fault condition is present. The amplifier restarts in play only once the overload is removed.
- Diagnostic mode, (IB4 D0 = "1"). It is enabled via I^2C and self activated if an output overload occurs to the speaker outputs. Once activated, the diagnostic procedure develops as below:
  - The diagnostic performs one restart cycle in order to avoid momentary re-circulation spikes which could give erroneous results. If a normal state (no overloads) is detected, the channel returns back active.
  - Instead, if after the restart cycle, the overload is still detected, then the diagnostic performs a plateau cycle.
  - After the plateau cycle, a restart cycle is going to be performed every 2 ms until the fault condition is not removed. The data acquired from the plateau cycle are stored and can be read from the microprocessor. If the fault condition persists, a new plateau cycle can programmed from I^2C simply by reading. This ensures continuous diagnostic throughout the car-radio operating time.

For a more immediate understanding, the permanent diagnostic's flowchart is as in *Figure 41*.

Figure 41. Permanent diagnostic flow-chart



When a plateau cycle is done during the permanent diagnostic the bit D5 of byte connected to the channel where the overload occurred is set to "1". If all the bits related to the diagnostic are "0", it means that the fault has been removed or has not been detected or it occurred an over current on a loudspeaker with a very high inductance and it took more than 2 ms to get the current reduced.

A plateau cycle can be recalled by mean of a reading procedure of bytes DB1/2/3/4 when the amplifier is performing the restart cycle. As for the turn-on diagnostic, when DB4 is read DB1/2/3/4 are reset, therefore the incremental reading is suggested in order to not miss any data.

Please note that if the over-current cause was removed before the reading the plateau cycle cannot restart.

7.4 AC diagnostic

The goal of this feature is to detect accidental disconnection of tweeters in 2-way speaker and, more in general, the presence of capacitive (AC) coupled load. This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) tends to increase towards high frequencies if the tweeter gets disconnected. This happens

because the remaining speaker (woofer) would be out of its operating frequency's range (high impedance).

To determine the load impedance, a sine wave tone of a suitable frequency should be provided to the output pins and the AC diagnostic is able to determine if a the tweeter is connected or not. The tweeter is not connected if for four consecutive sine waves the current threshold on the load is not crossed.

AC diagnostic is managed by I^2C commands. When IB4 D3 ="1", the AC diagnostic is enabled; IB4 D4 is used to choose the current level threshold that is compared during the test.

The results of the AC diagnostic test are stored in DB5 D3..6. It is written "1" if the tweeter for that channel is present.

The AC diagnostic is able to give the correct results only if the input signal Vout < Vs -4V. User knows that this condition is verified by reading "0" in DB5 D7. When DB5 D7 = "0", it mean that the test's signal was too high.

7.5 Output DC offset detection

Any DC output offset detection exceeding ± Vo are signalled out. This inconvenient might occur as a consequence of improper dc input signal. The offset detection is done at the end of the digital chain by a low pass digital filter. The offset detection is permanent, and then it works also in play mode. Results can be read in DB1, DB2, DB3 and DB4-D5.These bits are continuously refreshed.

7.6 Double faults

Faults can occur simultaneously. When this happens, faults are read out in according with the priority table (*Table 8*).

Please note that a "short to GND" and a "short to Vs" can be simultaneously read only when an open load is present; however it would mean three faults at the same time, which is not covered by TDA7802.

Table 8. Double faults priority

-	Soft short to GND(1)	Soft short to Vs(1)	Short to GND	Short to Vs	Short across load	Open load(1)
Soft short to GND	Soft Short to GND	/	Short to GND	/	Soft Short to GND	Soft Short to GND
Soft short to Vs	/	Soft Short to Vs	/	Short to Vs	Soft Short to Vs	Soft Short to Vs
Short to GND	Short to GND	/	Short to GND	/	Short to GND	Short to GND
Short to Vs	/	Short to Vs	/	Short to Vs	Short to Vs	Short to Vs
Short across load	/	/	/	/	Short across load	N.A.
Open load	/	/	/	/	/	Open Load

1. Open load, soft short to GND and soft short to Vs are only available for the turn-on diagnostic; in fact the permanent diagnostic can be triggered from an over current even, and no one of these event can be cause of an over current.

7.7 Legacy mode

In case of application without I^2C bus, the TDA7802 can be turned on in legacy mode.

In order to put the device in legacy mode is enough to tie the pin SCLlen to Vs. The amplifier is still turned-on by the pin PLLen and then it goes straight from low quiescent current mode to amplifier mode. The mute-play condition is managed from the pin SDAlm: the user can decide to either use or don't use this pin:

- When it is used, the unmute will occur only after SDAlm is raised above the higher VLM_MUTE threshold and it is performed internally by a digital ramp (note: the internal digital ramp is by default set to the fastest play/mute transition). The hardware unmute can be received only after the filter is configured and ready to go in play mode (note: “ready to go in play mode” means that the outputs have reached Vcc/2 level and the RAM is cleaned), otherwise it is ignored. When SDAlm is pulled below the lower VLM_MUTE threshold, the amplifier goes in mute mode. A RC of about 2 ms is suggested for this pin, especially when it is used for mute the amplifier before PLLen is pulled down to zero.
- SDAlm must be set at 3.3V (5V). The unmute is performed internally by a digital ramp, after the filter is configured. Instead, the mute is done after PLLen is pulled down to zero, because the PLL's lock lost. The PLL unlock muting has a time constant of about 2 ms.

The I^2C instruction bytes are set to a default value, and some of the selectable features are no longer available.

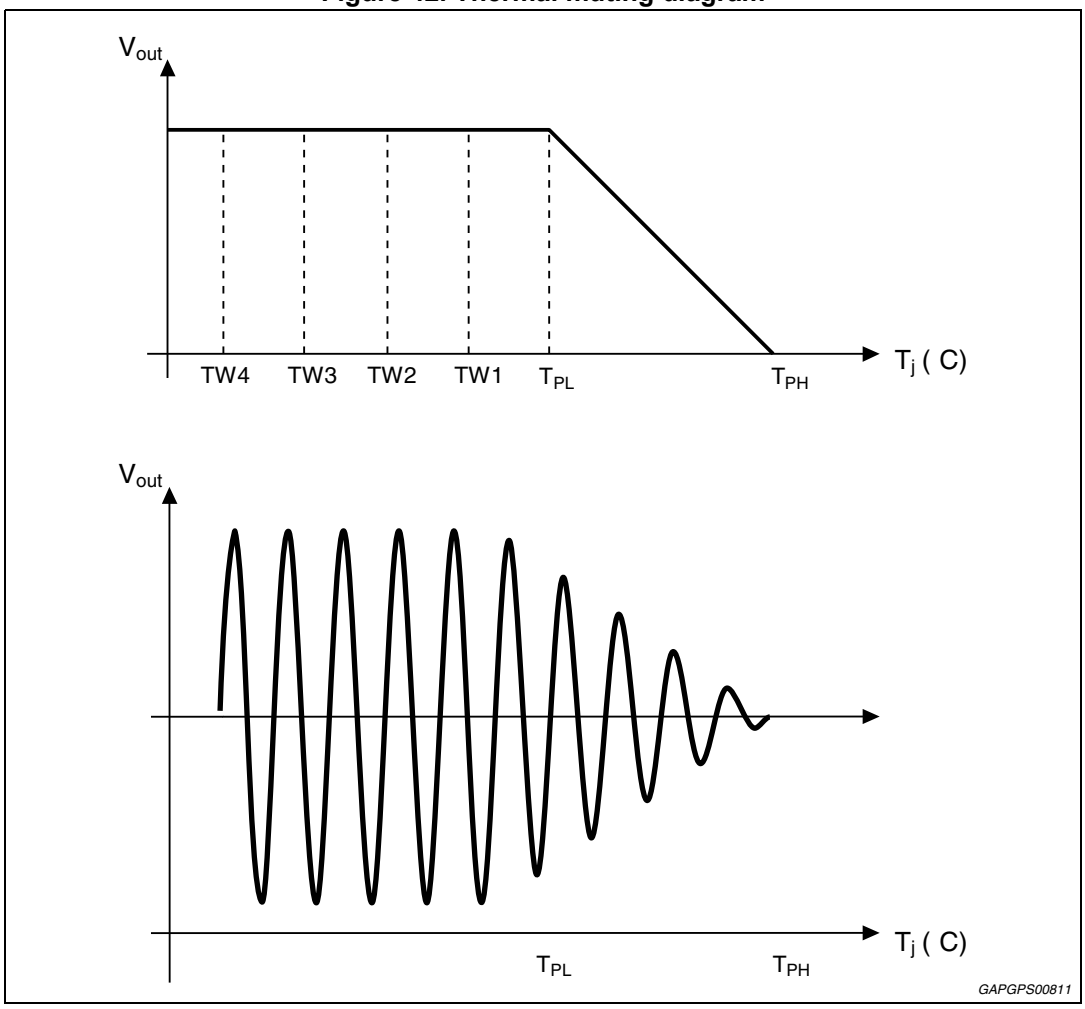
The default is set to “0” for all bits, except IB2 (D4/D3) = 11. This choice is needed to set the amplifier in “play mode”.

7.8 Thermal protection

The TDA7802 has four thermal warning (Tw1, Tw2, Tw3, Tw4) which are stored in I^2C data bytes. Only one of the thermal warnings can be sent to the pin CDdiag and it is selectable via I^2C bus.

A temperature dependent mute function is implemented in order to protect the junction from the over temperature and prevent the IC from sound quality degradation. Over the temperature Tpl the device is gradually carried in mute. When the temperature is Tpl the output signal is attenuated of 0.5 dB, while at the Tph the attenuation is of 60 dB. The distortion is kept low throughout the whole muting transition. The thermal protection's behaviour is shown in *Figure 42*.

Figure 42. Thermal muting diagram



7.9 Mute management

The transition Mute → Play can happen once the device is in amplifier mode and IB2-D3/D4 ="1" or after has been put in mute for one of the causes listed in Table 8.It is done by mean of a digital ramp whose the time constant is programmable by IB2 D7, D6 and D5 bits. The digital un-mute works in this way: all the D2A converter's elements, which at the beginning are off, are progressively turned on until they reach the steady value that is present at the input of the converter.

The transition Play → Mute occurs when certain conditions are verified and it can be Digital or Analog. An over view of all the events that might happen are reported in the *Table 9*.

Table 9. Transition play to mute strategy

Cause of transition Play → Mute	When it happens	Analog	Digital
I^2C instruction	When bit IB2 D4,D3 = “0” (Mute command)	No	Yes Timing for transition are fixed by IB2 D7, D6, D5
Hardware mute in legacy mode	SDAlm is pulled below the mute threshold	Yes	Disabled
Low battery mute	When there is a battery dip and the Vs goes below the auto mute threshold (selectable by IB2 D1)	Yes	IB2-D2 = 0: Yes IB2-D2 = 1: Disable If digital mute is enabled, timing for transition are fixed by IB2 D7-D6-D5
High battery mute	When Vs ramp up above 19V	Yes	No
PLL un-lock	The PLL lock detector goes down for some reason	Yes	Not possible because in case of un-lock, digital core is reset so not working
Thermal mute	When Tw1 is “1”	Yes	Disabled
Tristate command	No	Yes	Timing for transition are fixed by IB2-D7, D6, D5

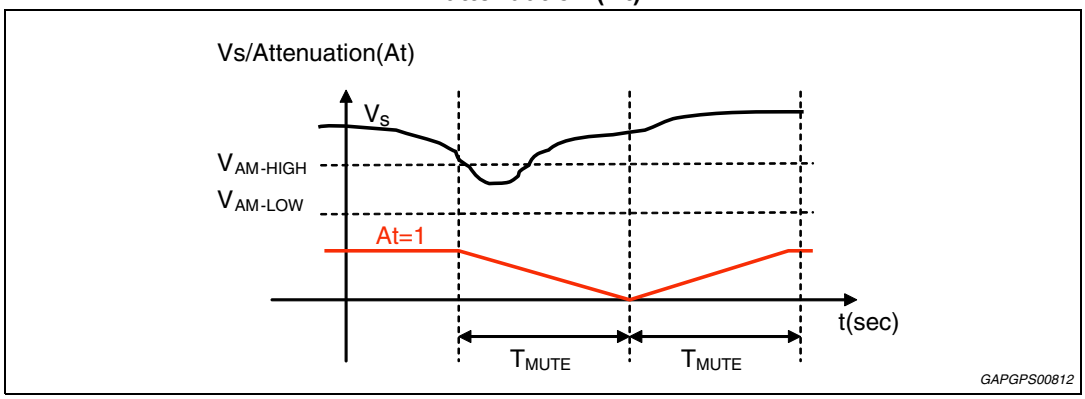
7.9.1 Auto-mute threshold

The device in play mode is put in mute when the supply voltage gets below the V_{AM} threshold.

The muting strategy for this kind of event is reported in *Figure 43*. Both analog and digital mute start when the supply voltage is below V_{AM_HIGH}. The digital mute transition lasts a period T_{MUTE}. The analog mute attenuation is proportional to Vs; when Vs is at V_{AM_LOW} the mute attenuation is A_M.

Note that, once it is engaged, the digital mute procedure is carried up the A_M attenuation. It is not possible to stop it and move the device to play mode in advance. The concept of this procedure is to avoid that fast oscillation on Vs can generate fast oscillation on the output.

Figure 43. Low voltage mute attenuation, supply voltage variation (Vs); result digital attenuation (At)



When the battery goes below the auto-mute low threshold, it is possible to disable the digital muting if IB2 D2 ="1". In this case the mute will be only analog.

The digital mute is also disabled during the turn-on diagnostic.

7.10 SB-I Improved high efficiency principle

The TDA7802 has an improved high efficiency that minimizes the power dissipated through the heat sink thanks to the musical signal characteristic. All bridges are connected to a common bar by mean of four power switches. When an input signal goes under a threshold that depends on the Vs level, the switch will short the corresponding output to the common bar in such a way that it can exchange current with the other channel. The dissipation reduction can be up to 50% compared to standard AB class.

The TDA7802 sets the high efficiency mode by default, but it can be changed though the bits IB0 D3, D2, D1 and D0.

7.11 1 Ohm load driving configurations

The TDA7802 has the possibility to drive 1 ohm loads. The functionality is possible since the two output powers gates (master and slave) are shorted together and only one of the two drivers is effectively working (the master). At the same time the outputs are shorted on the application in such a way to minimize the resistive path.

The pins 20 and 21 are dedicated for this function, as it follows:

Pin 21 & pin 20:

"00" 2 ohm for all channels

"01" (ch1 and ch2): 1 ohm, (ch3 and ch4): 2 ohm

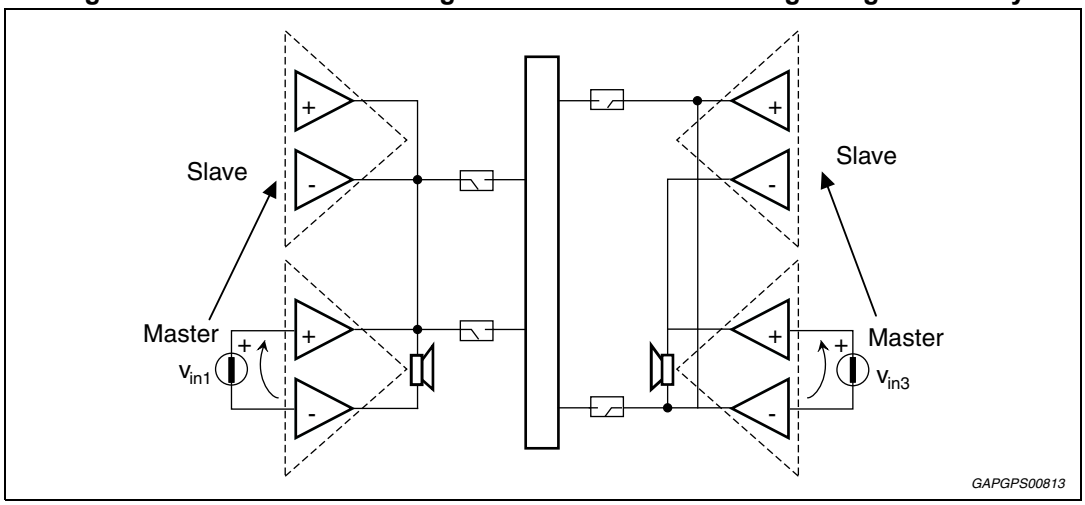
"10" (ch1 and ch2): 2 ohm, (ch3 and ch4): 1 ohm;

"11" all channels are set to 1 ohm.

The master channels are channel 1 (when ch1 and ch2 are configured to 1 ohm), and channel 3 (when ch3 and ch4 are configured to 1 ohm).

The TDA7802 is able to work in high efficiency mode also when two channels are configured in 1 ohm (see*Figure 44*).

Figure 44. Two channels configured to 1 Ohm and working in high efficiency



7.12 Power on reset threshold

When the PLLen is low of the supply voltage value does not guarantee the integrity of I^2C registers (Vs = 4V), the TDA7802 is put in low quiescent current and the bytes are initialized. This event is signalled writing "0" on DB0 D7 bit.

8 I²S and TDM bus interface

The audio input port is a three/four-wire synchronous serial interface that can operate only as Slave. Pins SD13 and SD24 are the serial data inputs. The audio data format accepted from TDA7802 is the I²S standard.

Input data can also be sent in time division multiplexed (TDM). Pins SCK (bit clock) and WS (frame select) complete the I²S interface.

Important note on I2S-clock: when I2S-clk is lost during amplifier operation a protection circuit acts and puts the amplifier in a safe condition: amplifier short circuit protections are guaranteed, dump protection is guaranteed, signal is muted and outputs bias is under control.

For avoiding other side effects user should put the amplifier in standby moving PLL/en pin to 0 V.

8.1 I²S and TDM input data frame format

The audio data word length for each channel may be up to 24 bit. Either for I2S or TDM mode, the frame for each channel can be 25 bit or 32 bit. The selection of the frame's length is done via I²C: when IB3 D2 = "0", the I²S interface expects to receive 32 samples for each channel; while when IB3 D2 ="1", the I²S interface expects only 25 samples.

The following table summarizes the frequencies configurations.

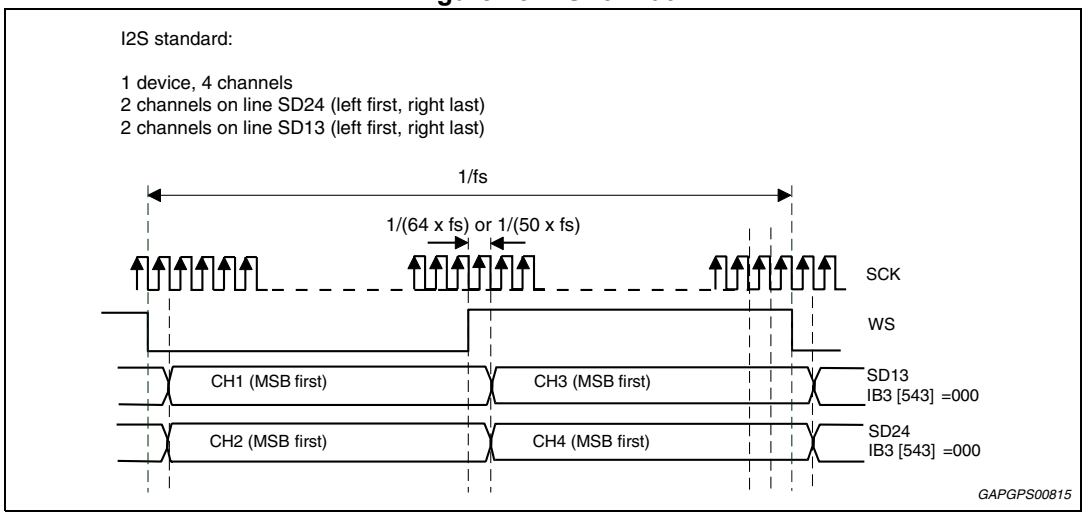
Table 10. System input frequencies

Frequency sampling (Fs)	System clock frequency (f_{SCK}), (MHz)			Channel frame length (bit)
	I²S standard	TDM 4ch	TDM 8ch/16ch)	
44.1 (kHz)	2.8224	5.6448	11.2896	32
	2.205	4.41	8.82	25
48 (kHz)	3.072	6.144	12.288	32
	2.4	4.8	9.6	25
96 (kHz	6.144	12.288	24.576	32
	4.8	9.6	19.2	25
192 (kHz	12.288	24.576	49.152	32
	9.6	19.2	38.4	25

8.2 I²S input data format

The TDA7802 accepts I²S standard interface format as in *Figure 45* and the I²C bit configuration is IB3 [D5,D4,D3] = "000".

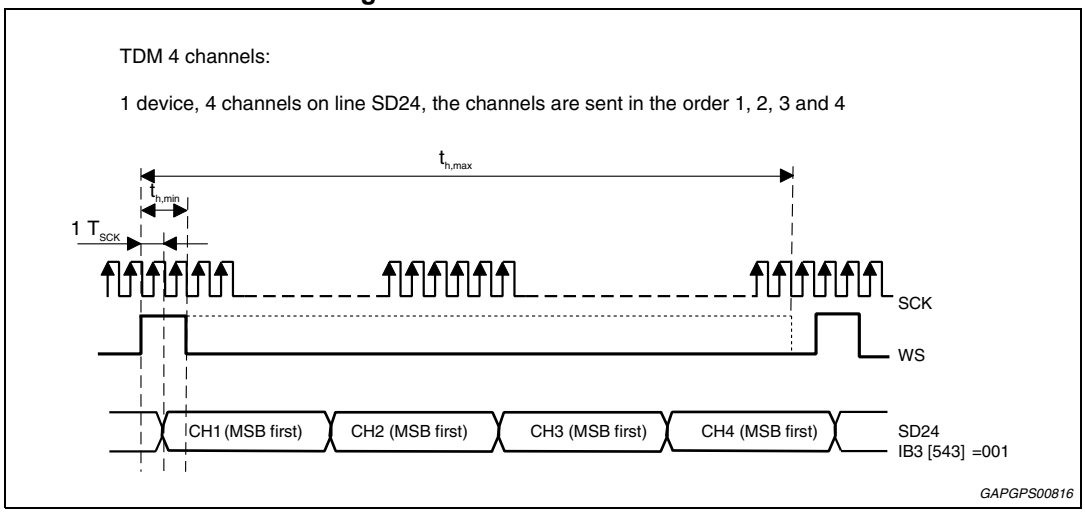
Figure 45. I²S format



8.3 TDM input data format

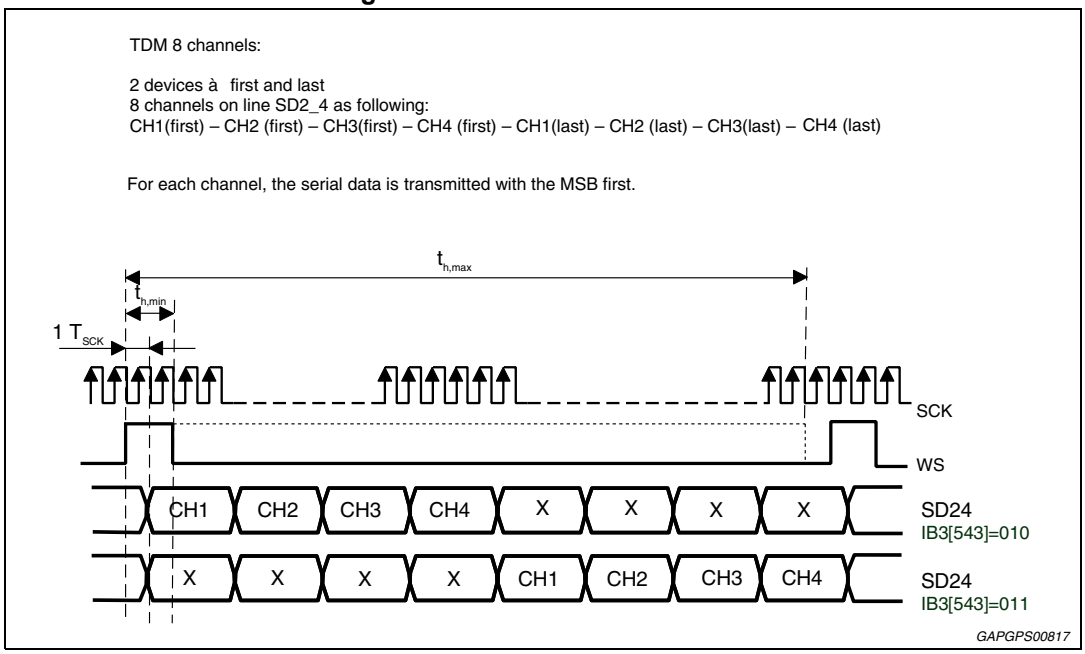
TDM 4-channel is allowed for TDA7802 and it is as in *Figure 46*. All the channels are sent on the audio data line SD24. The channel's order is 1, 2, 3 and 4. The I²C bit configuration is IB3 [D5, D4, D3] = "001".

Figure 46. TDM 4-channel format



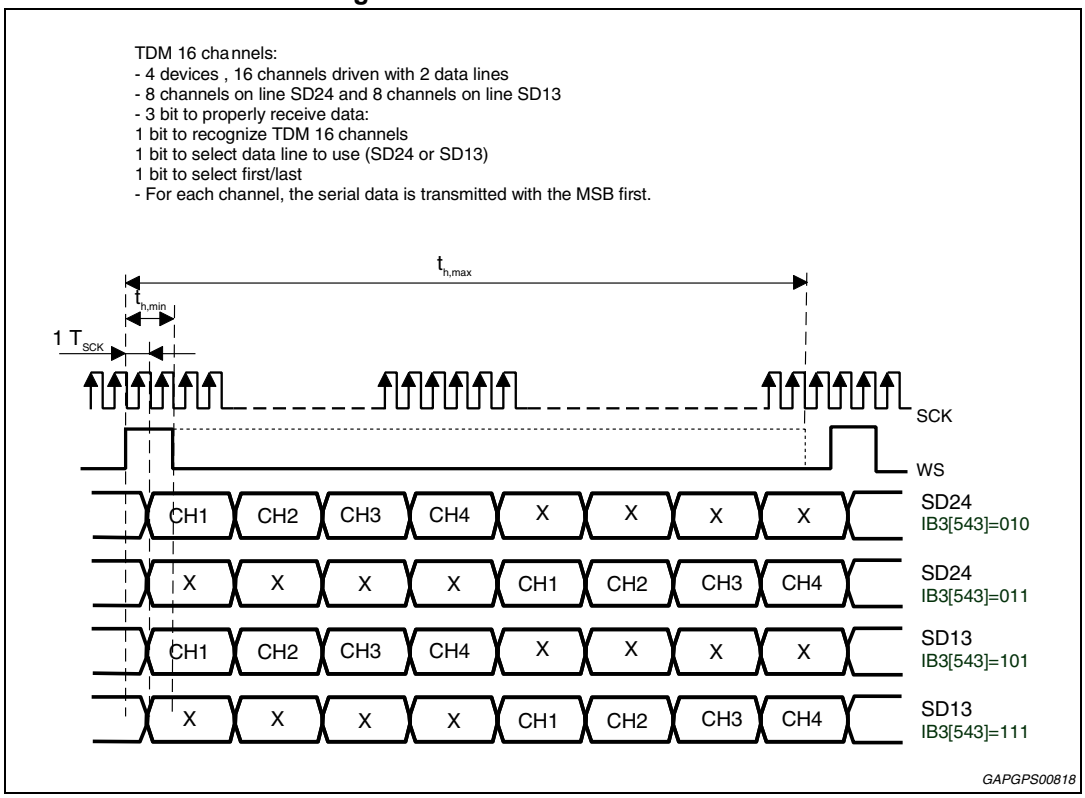
TDM 8-channel is also allowed and two devices (device 1 and device 2) can be driven by using just one serial data line SD24. There are two selectable options
When IB3 [D5,D4,D3] = "010" device 1 is first sent; when IB3 [D5,D4,D3] = "011" device 2 is first sent. In *Figure 47* TDM 8-channel format is showed.

Figure 47. TDM 8-channel format



The TDM 8 channel is expansible to TDM 16 channel (*Figure 48*) where both SD24 and SD13 data lines are used. All the configurations are selectable via I²C.

Figure 48. TDM 16-channel format



8.4 Timings requirements

Figure 49. Audio interface timing

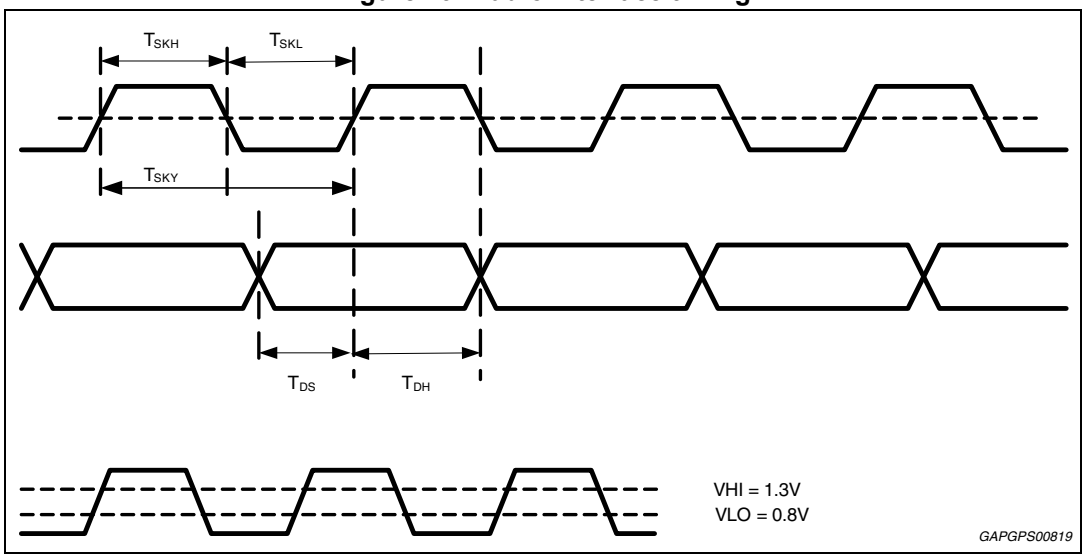


Table 11. I²S interface timing

Symbol	Parameter	note	min	max	unit
Fsck0	SCK (bit clock) frequency	-	-	49.152	MHz
-	SCK (bit clock) frequency tolerance	-	0.9Fsck0	1.1Fsck0	MHz
Tsck	SCK period	-	20	-	ns
-	SCK duty cycle	-	40	60	%
Tsckh	SCK high time	-	6	-	ns
Tsckl	SCK low time	-	6	-	ns
-	SCK transition time	-	-	4	ns
-	WS (word select) frequency	-	-	192	KHz
Twsh	WS high time	I2S standard	25 or 32 Tsck (duty cycle=50%)		ns
Twsh	WS high time	TDM 4-channel	1 Tsck	127 Tsck	ns
Twsh	WS high time	TDM 8-16-channel	1 Tsck	255 Tsck	ns
Tws	WS setup time	-	5	-	ns
Twh	WS hold time	-	6	-	ns
Tds	SD13 SD24 (data inputs) setup time before SCK rising edge	-	5	-	ns
Tdh	SD13 SD24 (data inputs) hold time after SCK rising edge	-	6	-	ns

For TDM mode:

- WS changes at SCK falling edge, on clock period before the MSB is transmitted
- WS does not need to be symmetrical. It need to stay high for at least 2 SCK period clock. The maximum duration is:
  - T_{h_max} = 127 T_{SCK} in TDM 4-channel
  - T_{h_max} = 255 T_{SCK} in TDM 8-channel and TDM 16-channel
- The other timings are like in *Table 11*.

8.5 Group delay

The group delay is due to the FIR filter of first interpolator and it is T_{delay} = 32/Fs.

9 I²C bus interface

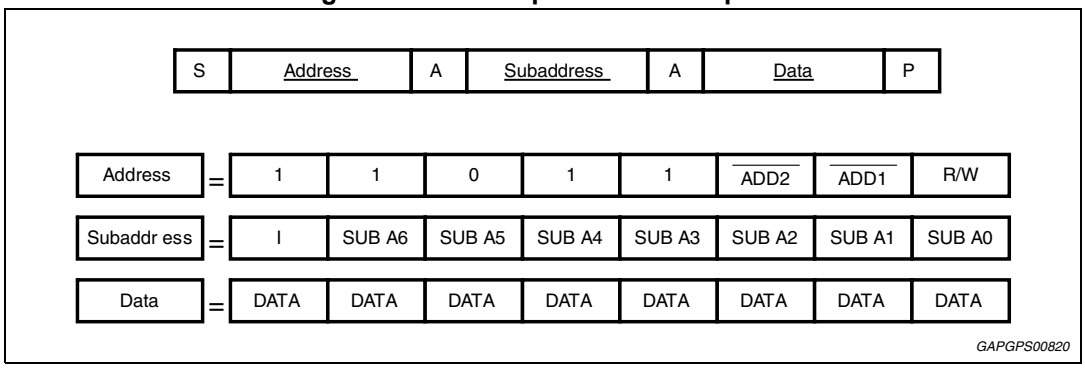
Data transmission from microprocessor to the TDA7802 and viceversa takes place through the 2 wires I2C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

When I²C bus is active, the user can select the IC's operating mode. He can perform the diagnostic cycle whose the results are stored into the data byte, and read the instruction and data bytes back.

The protocol used for the bus is depicted in *Figure 50* and comprises:

- a start condition (S)
- a chip Address byte (the LSB bit determines read/write transmission)
- a Subaddress byte
- a sequence of Data (N-bytes + acknowledge)
- a stop condition (P)

Figure 50. I²C bus protocol description



Description:

- S = Start
- R/W = '0' => Receive-Mode (Chip could be programmed by uP)
- I = Auto increment; when 1, the address is automatically incremented for each byte transferred
- A = Acknowledge
- P = Stop
- MAX CLOCK SPEED 400kbit/sec

There are four I²C addresses (for PowerSO36 package): 1101100, 1101101, 1101110, 1101111.

For Flexiwatt package only the 1101100 is available (if no bonding options are considered).

9.1 Writing procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the register to be written is addressed by the subaddress SUB A. Only this register is written by the DATA byte following the subaddress byte.
2. with increment: the I bit is set to 1 and the first register to be written is the one addressed by subaddress SUB A. Then all the registers from SUB A up to stop bit or the reaching of last register are written.

9.2 Reading procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the only register to be read is addressed by the subaddress sent in the previous write procedure.
2. with increment: the I bit is set to 1 and the first register to be read is the one addressed by subaddress sent in the previous write procedure. Then all the registers from this subaddress up to stop bit or the reaching of last register are read.

9.3 Data validity

The data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

9.4 Start and stop conditions

A start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

9.5 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

9.6 Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The receiver** the acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

* **Transmitter**

= master (µP) when it writes an address or instruction byte to the TDA7802
= slave (TDA7802) when the µP reads a data byte from TDA7802

** **Receiver**

= slave (TDA7802) when the µP writes an address or instruction byte to the TDA7802
= master (µP) when it reads a data byte from TDA7802

9.7 I²C bus timings

This paragraph describes more in detail the I2C bus protocol used and its timings. Figure 21 and Table 12 include the timing that need to be respected in order to correctly write into/ read from the I²C registers.

Figure 51. I²C bus interface timing

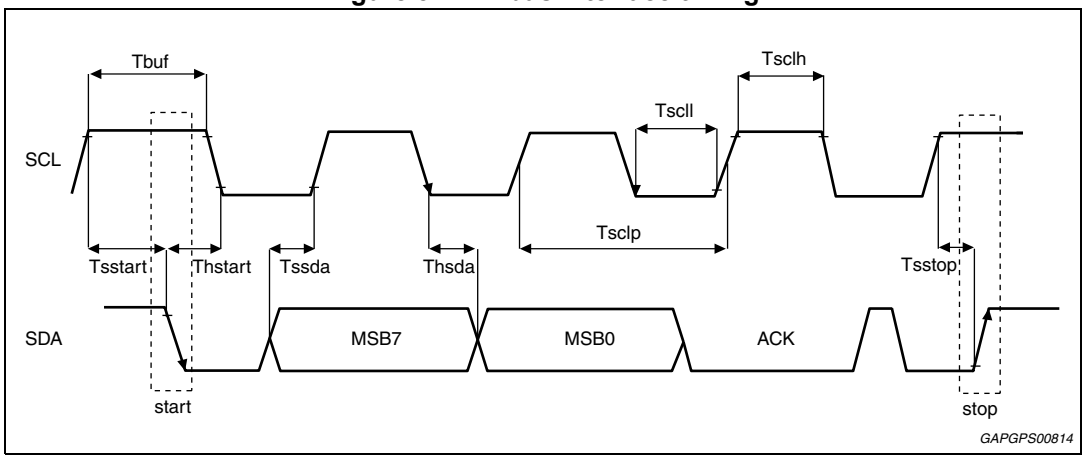


Table 12. I²C bus interface timing

Symbol	Parameter	Min	Max	Unit
Fscl	SCL (clock line) frequency	-	400	kHz
Tscl	SCL period	2500	-	ns
Tsclh	SCL high time	0.6	-	µs
Tscll	SCL low time	1.3	-	µs
Tsstart	Setup time for start condition	0.6	-	µs
Thstart	Hold time for start condition	0.6	-	µs
Tsstop	Setup time for stop condition	0.6	-	µs
Tbuf	Bus free time between a stop and a start condition	1.3	-	µs
Tssda	Setup time for data line	100	-	ns
Thsda	Hold time for data line(1)	500	-	ns
Tf	Fall time for SCL and SDA	-	300	ns

10 I²C registers

10.1 Instruction byte

10.1.1 IB0 - Subaddress "I0000000h" - default = "00000000"

Table 13. IB0 - Subaddress "I0000000h" - default = "00000000"

Bit	Instruction decoding bit
D7	**Channel 4 Tristate Mode** 0: off 1: on
D6	**Channel 3 Tristate Mode** 0: off 1 on
D5	**Channel 2 Tristate Mode** 0: off 1: on
D4	**Channel 1 Tristate Mode** 0: off 1: on
D3	**Channel 4 Amplifier Mode** 0: High Efficiency Mode 1: Standard Class AB Mode
D2	**Channel 3 Amplifier Mode** 0: High Efficiency Mode 1: Standard Class AB Mode
D1	**Channel 2 Amplifier Mode** 0: High Efficiency Mode 1: Standard Class AB Mode
D0	**Channel 1 Amplifier Mode** 0: High Efficiency Mode 1: Standard Class AB Mode

10.1.2 IB1 - Subaddress "I0000001h" - default = "00000000"

Table 14. IB1 - Subaddress "I0000001h" - default = "00000000"

Bit	Instruction decoding bit
D7	**Impedance efficiency optimizer (rear channels)** 0: Efficiency optimized for 2 ohm 1: Efficiency optimized for 4 ohm
D6 **D5**	**Long diagnostic configuration timing** D6 D5 timing configuration 0 0 default 0 1 stretched x 2 1 0 stretched x 4 1 1 stretched x 8
D4 **D3**	**Gain Channel 1 & 3** D4 D3 Gain 0 0 GV1 0 1 GV2 1 0 GV3 1 1 GV4
D2 **D1**	**Gain Channel 2 & 4** D2 D1 Gain 0 0 GV1 0 1 GV2 1 0 GV3 1 1 GV4
D0	**Digital Gain Increase** 0: No digital gain increase 1: +6dB digital gain increase

10.1.3 IB2 - Subaddress "I0000010h" - default = "00000000"

Table 15. IB2 - Subaddress "I0000010h" - default = "00000000"

Bit	Instruction decoding bit
D7	**Mute Time Setting** D7 D6 D5 mute timing(Fs=44.1kHz) 0 0 0 1.45 ms 0 0 1 5.8 ms 0 1 0 11.6 ms 0 1 1 23.2 ms 1 0 0 46.4 ms 1 0 1 92.8 ms 1 1 0 185.6 ms 1 1 1 371.2 ms
D6	
D5	
D4	**Mute 1&3** 0: Channels 1&3 Muted 1: Channels 1&3 un-Muted
D3	**Mute 2&4** 0: Channels 2&4 Muted 1: Channels 2&4 un-Muted
D2	**Digital mute enabling** 0: digital mute enable 1: digital mute disable
D1	**Automute threshold** 0: 5.3V (guaranteed play down to 6V) 1: 7.3V (guaranteed play down to 8V)
D0	**Impedance efficiency optimizer (front channels)** 0: Efficiency optimized for 2 ohm 1: Efficiency optimized for 4 ohm

10.1.4 IB3 - Subaddress "I0000011h" - default = "00000000"

Table 16. IB3 - Subaddress "I0000011h" - default = "00000000"

Bit	Instruction decoding bit
D7	**Sample frequency range** (1) D7 D6 Sample frequency 0 0 44.1 kHz 0 1 48 kHz 1 0 96 kHz 1 1 192 kHz
D6	
D5	**Digital Input Format** (1) D5 D4 D3 0 0 0 I2S standard 0 0 1 TDM – 4ch 0 1 0 TDM – 8ch (SD2_4 input, device 1) 0 1 1 TDM – 8ch (SD2_4 input device 2) 1 0 0 TDM – 16ch (SD2_4 input - device 1) 1 0 1 TDM – 16ch (SD2_4 input - device 2) 1 1 0 TDM – 16ch (SD1_3 input - device 3) 1 1 1 TDM – 16ch (SD1_3 input - device 4)
D4	
D3	
D2	**I2S Frame Period length** (1) 0: 64 bits (Fs=44.1kHz, 48kHz,96kHz,192kHz) 1: 50 bits (Fs=48kHz,96kHz,192kHz)
D1	**PLL Clock Dither enable/disable** (1) 0: disable 1: enable
D0	**High pass filter enable/disable** (1) 0: disable 1: enable

1. Byte IB3 settings can be changed only if the amplifier is in low quiescent current state, otherwise the command is ignored.

10.1.5 IB4 - Subaddress "I0000100h - default = "00000000"

Table 17. IB4 - Subaddress "I0000100h - default = "00000000"

Bit	Instruction decoding bit
D7	**Noise Gating Function enable/disable** 0: enable 1: disable
D6	**Short Fault information on CDdiag pin** **0: yes** 1: no
D5	**Offset information on CDdiag pin** 0: yes (if IB3 < 0 >='1') 1: no
D4	**AC diagnostic current threshold** 0: high 1: low
D3	**AC Diagnostic Enable/Disable** 0: disable 1: enable
D2	**Channel 1&3 Diagnostic Mode** 0: Speaker mode 1: Booster mode
D1	**Channel 2&4 Diagnostic Mode** 0: Speaker mode 1: Booster mode
D0	**Diagnostic Mode Enable/Disable** 0: disable 1: enable

10.1.6 IB5 - Subaddress "I0000101h" - default = "00000000"

Table 18. IB5 - Subaddress "I0000101h" - default = "00000000"

Bit	Instruction decoding bit
D7 D6 D5	**Temperature warning information on CDdiag pin** D7 D6 D5 Temperature 0 0 0 TW1 0 0 1 TW2 0 1 0 TW3 0 1 1 TW4 1 x x no thermal warning information on diag pin
D4 D3	**Clipping detection level for front channels** D4 D3 0 0 2% for all channel 1 and 3 0 1 5% for all channel 1 and 3 1 0 10% for all channel 1 and 3 1 1 no clipping for channel 1 and 3
D2 D1	**Clipping detection level for rear channels** D2 D1 0 0 2% for all channel 2 and 4 0 1 5% for all channel 2 and 4 1 0 10% for all channel 2 and 4 1 1 no clipping for channel 2 and 4
D0	**Amplifier on/off** 0: off 1: on

10.2 Data byte

10.2.1 DB0 - Subaddress: "I0010000h"

Table 19. DB0 - Subaddress: "I0010000h"

Bit	Instruction decoding bit
D7	**Power on reset (POR)** 0: the start-up phase to move from ‘standby’ state to ‘low quiescent current’ state is running 1: the device is ‘out of standby’.
D6	**Start-up Diagnostic status** 0: Turn-on Diag. cycle not activated or not terminated 1: Turn-on Diag. cycle terminated
D5	**TW1** 0: TW1 threshold not trespassed 1: TW1 threshold trespassed
D4	**TW2** 0: TW2 threshold not trespassed 1: TW2 threshold trespassed
D3	**TW3** 0: TW3 threshold not trespassed 1: TW3 threshold trespassed
D2	**TW4** 0: TW4 threshold not trespassed 1: TW4 threshold trespassed
D1	**Channel 2 & 4 in mute/play** 0: Channel 2 & 4 in play 1: Channel 2 & 4 in mute
D0	**Channel 1 & 3 in mute/play** 0: Channel 1 & 3 in play 1: Channel 1 & 3 in mute

10.2.2 DB1 - Subaddress: "I0010001h"

Table 20. DB1 - Subaddress: "I0010001h"

Bit	Instruction decoding bit
D7	**Diagnostic Data Valid** 0: diagnostic data valid 1: diagnostic data not valid
D6	**Channel 1 Soft Short present** 0: No Soft short 1: Soft Short (only during turn-on diagnostic)
D5	**Channel 1 offset detection** 0: No output offset 1: Output offset detected
D4	**Channel 1 Permanent Diagnostic status** 0: Permanent diagnostic cycle not activated or not terminated 1: Permanent diagnostic cycle terminated
D3	**Channel 1 Normal/Short Load** 0: Normal load 1: Short load
D2	**Channel 1 Open load** 0: No open load 1: Open load detection (only during turn-on diagnostic)
D1	**Channel 1 Short to VCC** 0: No Hard short to Vcc 1: Hard short to Vcc
D0	**Channel 1 Short to GND** 0: No short to GND 1: Short to GND

10.2.3 DB2 - Subaddress: "I0010010h"

Table 21. DB2 - Subaddress: "I0010010h"

Bit	Instruction decoding bit
D7	**Reserved**
D6	**Channel 2 Soft Short present** 0: No Soft short 1: Soft Short (only during turn-on diagnostic)
D5	**Channel 2 offset detection** 0: No output offset 1: Output offset detected
D4	**Channel 2 Permanent Diagnostic status** 0: Permanent diagnostic cycle not activated or not terminated 1: Permanent diagnostic cycle terminated
D3	**Channel 2 Normal/Short Load** 0: Normal load 1: Short load
D2	**Channel 2 Open load** 0: No open load 1: Open load detection (only during turn-on diagnostic)
D1	**Channel 2 Short to VCC** 0: No Hard short to Vcc 1: Hard short to Vcc
D0	**Channel 2 Short to GND** 0: No short to GND 1: Short to GND

10.2.4 DB3 - Subaddress: "I0010011h"

Table 22. DB3 - Subaddress: "I0010011h"

Bit	Instruction decoding bit
D7	**Reserved**
D6	**Channel 3 Soft Short present** 0: No Soft short 1: Soft Short (only during turn-on diagnostic)
D5	**Channel 3 offset detection** 0: No output offset 1: Output offset detected
D4	**Channel 3 Permanent Diagnostic status** 0: Permanent diagnostic cycle not activated or not terminated 1: Permanent diagnostic cycle terminated
D3	**Channel 3 Normal/Short Load** 0: Normal load 1: Short load
D2	**Channel 3 Open load** 0: No open load 1: Open load detection (only during turn-on diagnostic)
D1	**Channel 3 Short to VCC** 0: No Hard short to Vcc 1: Hard short to Vcc
D0	**Channel 3 Short to GND** 0: No short to GND 1: Short to GND

10.2.5 DB4 - Subaddress: "I0010100h"

Table 23. DB4 - Subaddress: "I0010100h"

Bit	Instruction decoding bit
D7	**Not used**
D6	**Channel 4 Soft Short present** 0: No Soft short 1: Soft Short (only during turn-on diagnostic)
D5	**Channel 4 offset detection** 0: No output offset 1: Output offset detected
D4	**Channel 4 Permanent Diagnostic status** 0: Permanent diagnostic cycle not activated or not terminated 1: Permanent diagnostic cycle terminated
D3	**Channel 4 Normal/Short Load** 0: Normal load 1: Short load
D2	**Channel 4 Open load** 0: No open load 1: Open load detection (only during turn-on diagnostic)
D1	**Channel 4 Short to VCC** 0: No Hard short to Vcc 1: Hard short to Vcc
D0	**Channel 4 Short to GND** 0: No short to GND 1: Short to GND

10.2.6 DB5 - Subaddress: "I0010101h"

Table 24. DB5 - Subaddress: "I0010101h"

Bit	Instruction decoding bit
D7	0: Signal ok 1: Signal too high
D6	**Channel 4 tweether detection** 0: Ch4 tweeter not present 1: Ch4 tweeter present
D5	**Channel 3 tweether detection** 0: Ch3 tweeter not present 1: Ch3 tweeter present
D4	**Channel 2 tweether detection** 0: Ch2 tweeter not present 1: Ch2 tweeter present
D3	**Channel 1 tweether detection** 0: Ch1 tweeter not present 1: Ch1 tweeter present
D2	**Front channel clip detection** 0: No clipping on front channel 1: Clipping on front channel
D1	**Rear channel clip detection** 0: No clipping on rear channel 1: Clipping on rear channel
D0	**PLL lock detector** 0: PLL not locked 1: PLL locked

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

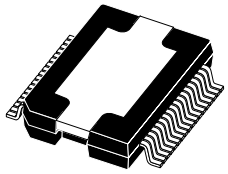
ECOPACK® is an ST trademark.

Figure 52. PowerSO36 (slug up) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.270	-	3.410	0.1287	-	0.1343
A2	3.100	-	3.180	0.1220	-	0.1252
A4	0.800	-	1.000	0.0315	-	0.0394
A5	-	0.200	-	-	0.0079	-
a1	0.030	-	-0.040	0.0012	-	-0.0016
b	0.220	-	0.380	0.0087	-	0.0150
c	0.230	-	0.320	0.0091	-	0.0126
D	15.800	-	16.000	0.6220	-	0.6299
D1	9.400	-	9.800	0.3701	-	0.3858
D2	-	1.000	-	-	0.0394	-
E	13.900	-	14.500	0.5472	-	0.5709
E1	10.900	-	11.100	0.4291	-	0.4370
E2	-	-	2.900	-	-	0.1142
E3	5.800	-	6.200	0.2283	-	0.2441
E4	2.900	-	3.200	0.1142	-	0.1260
e	-	0.650	-	-	0.0256	-
e3	-	11.050	-	-	0.4350	-
G	0	-	0.075	0	-	0.0031
H	15.500	-	15.900	0.6102	-	0.6260
h	-	-	1.100	-	-	0.0433
L	0.800	-	1.100	0.0315	-	0.0433
N	-	-	10°	-	-	10°
s	-	-	8°	-	-	8°

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006").
(2) No intrusion allowed inwards the leads.

OUTLINE AND MECHANICAL DATA



PowerSO36 (SLUG UP)

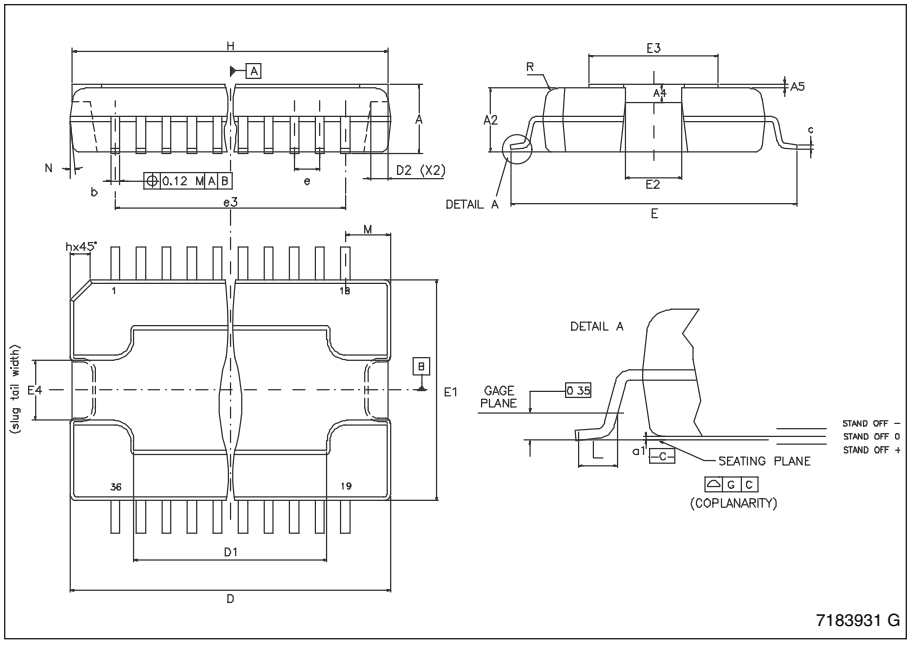
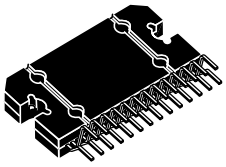


Figure 53. Flexiwatt27 (vertical) mechanical data and package dimensions

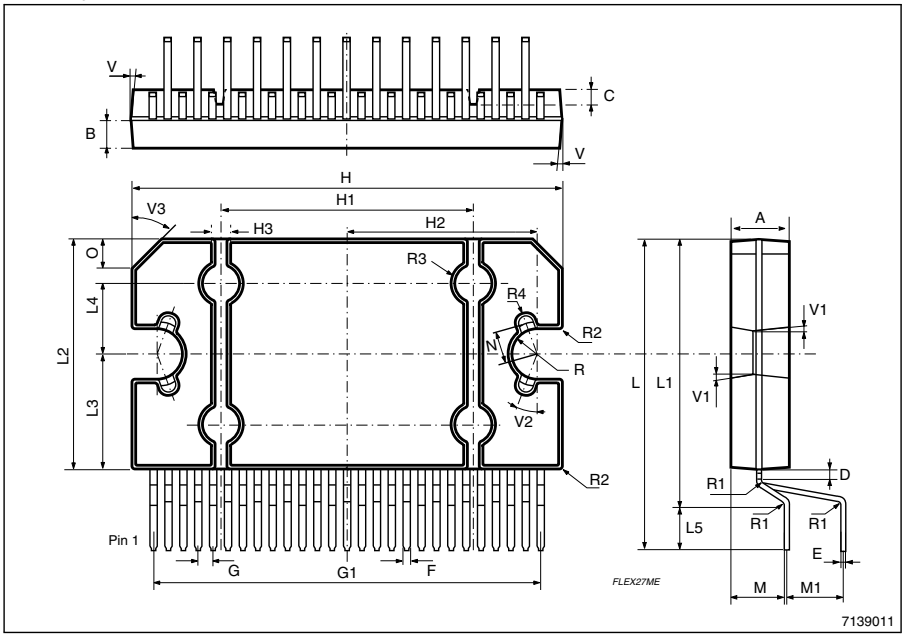
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	25.75	26.00	26.25	1.014	1.023	1.033
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt27 (vertical)



Appendix A I²C registers setting

This chapter includes some suggestions of how the I²C registers should be programmed.

A.1 Standard turn-on

- STANDBY OFF + MUTE PLAY TRANSITION (pop free transition)

  PLLen PIN '0' TO '1' (ABOVE VILENB) +

  WAIT 10 ms (PLL locking) +

  I2C WRITE D8 80 00 00 18 00 00 01 (auto increment active + default setting + unmute + amplifier on).
- STANDBY OFF + TURN-ON DIAGNOSTIC + MUTE PLAY TRANSITION (mute -> play done whatever is the diagnostic result)

  PLLen PIN '0' TO '1' +

  WAIT 10 ms +

  I2C WRITE D8 80 00 00 18 00 01 01 (default setting + unmute + diagnostic + amplifier on) + WAIT 500 ms +

  I2C READ D9 10
- In case you want to read diagnostic result first and then set the play the sequence becomes:

  PLLen PIN '0' TO '1' (ABOVE VILENB) + WAIT 10 ms (PLL locking) +

  I2C WRITE D8 80 00 00 18 00 01 00 (default setting + unmute + diagnostic) +

  WAIT 500 ms +

  I2C READ D9 10 +

  WAIT READING TIME +

  I2C WRITE D8 80 00 00 18 00 01 01.

  When this sequence is sent as above, an additional diagnostic cycle will start after the reading and then the amplifier starts to play. In order to avoid a second diagnostic pulse it is important to set IB4 D0 = '0'. Here below the writing procedure suggested:

  PLLen PIN '0' TO '1' +

  WAIT 10 ms +

  I2C WRITE D8 80 00 00 18 00 01 00 (default setting + unmute + diagnostic) +

  WAIT 50 ms +

  I2C WRITE D8 80 00 00 18 00 00 00 (default setting + unmute + diagnostic disable) +

  WAIT 450 ms +

  I2C READ D9 10 +

  WAIT READING TIME +

  I2C WRITE D8 80 00 00 18 00 01 01.

IMPORTANT every time a reading procedure is done, make sure DB0 = C0. This means the turn-on diagnostic is completed and the results valid.

A.2 Long diagnostic turn-on

The diagnostic pulse's duration can be programmed by bits IB1 D6 and IB1 D5. Let's consider the "x2" case in this section; all the other options are easily extendable with the help in the table 5. Please remember the "x2" factor has effect just on the short load pulse (See *Section 7.2*).

- STANDBY OFF + TURN-ON DIAGNOSTIC + MUTE PLAY TRANSITION (mute -> play done whatever is the diagnostic result)

PLLen PIN '0' TO '1' +

WAIT 10 ms +

I2C WRITE D8 80 00 20 18 00 01 01 (default setting + long diagnostic x2 + unmute + diagnostic + amplifier on) +

WAIT 500 ms +

I2C READ D9 10 +

Case 4 Ohm loudspeaker or 2 Ohm (and not misconnections)

The diagnostic has been completed and the results are valid. Not further reading procedures are needed.

Case 4 Ohm loudspeaker or 2 Ohm (and open load on at least 1 channel)

The diagnostic is likely not finished (check the byte DB0)

WAIT 200 ms +

I2C READ D9 10

Note that the reading might happen when the amplifier has already started to play. This does not change the effectiveness of the action; after the reading the data bytes are reset.

- In case you want to read diagnostic result first and then set the play the sequence becomes:

PLLen PIN '0' TO '1' +

WAIT 10 ms +

I2C WRITE D8 80 00 20 18 00 01 00 (default setting + long diagnostic x2 + unmute + diagnostic + amplifier on) +

WAIT 500 ms +

I2C READ D9 10 +

WAIT READING TIME +

If DB0 = C0

I2C WRITE D8 80 (auto increment active) 00 20 18 00 01 01.

If DB0 = 80 (DB0 D6 = '0')

WAIT 200 ms +

I2C READ D9 10 (UNTIL DB0 = C0) +

I2C WRITE D8 80 (auto increment active) 00 20 18 00 01 01

A.3 Legacy mode turn-on

- STANDBY OFF + MUTE PLAY TRANSITION

PLLen PIN '0' TO '1' +

WAIT 100 ms +

SDALM PIN '0' to '1' (LEGACY UNMUTE)

A.4 Legacy mode turn-off

- PLAY MUTE TRANSITION STANDBY ON

SDALM PIN '1' to '0' (LEGACY MUTE)

WAIT 100 ms (It depends from the RC time constant in the application)

PLLen PIN '1' TO '0' (STANDBY ON)

A.5 Battery crank setting

When the battery goes below 4V the I2C settings are not longer guaranteed. In order to reset the amplifier it is important to follow the below sequence:

WAIT UNTIL DB0-D7 = '1'

I2C WRITE D8 03 XX (PLL SETTING IF DIFFERENT FROM DEFAULT)

WAIT 500 µs (PLL LOCKING)

I2C WRITE D8 80 00 00 18 00 00 01 (unmute + amplifier on)

Note that this sequence it's very important when the CODEC is set different from the I2S standard format and Fs = 48 kHz.

Revision history

Table 25. Document revision history

Date	Revision	Changes
10-May-2013	1	Initial release.

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