



STF6N65K3, STFI6N65K3, STU6N65K3

N-channel 650 V, 1.1 Ω typ., 5.4 A SuperMESH3™ Power MOSFET in TO-220FP, I²PAKFP, IPAK

Datasheet — production data

Features

Order codes	V _{DSS}	R _{DS(on)} max.	I _D	P _{tot}
STF6N65K3	650 V	< 1.3 Ω	5.4 A	30 W
STFI6N65K3				110 W
STU6N65K3				

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These SuperMESH3™ Power MOSFETs are the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

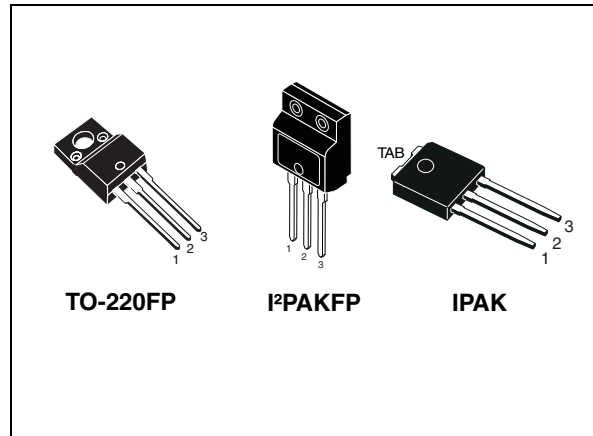


Figure 1. Internal schematic diagram

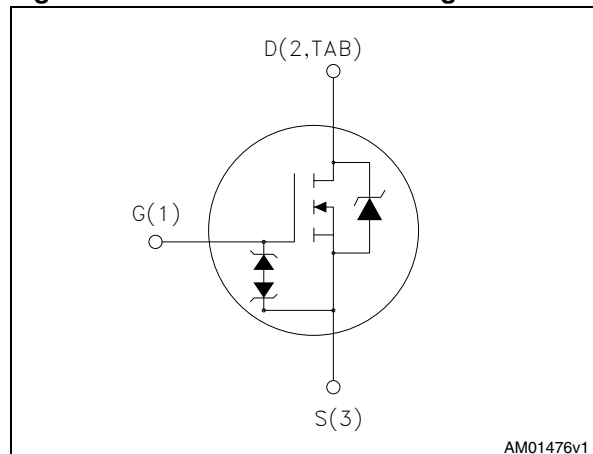


Table 1. Device summary

Order codes	Marking	Package	Packaging
STF6N65K3	6N65K3	TO-220FP	Tube
STFI6N65K3		I ² PAKFP	
STU6N65K3		IPAK	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		TO-220FP	I ² PAKFP	I ² PAK	
V _{DS}	Drain-source voltage	650			V
V _{GS}	Gate- source voltage	± 30			V
I _D	Drain current (continuous) at T _C = 25 °C	5.4 ⁽¹⁾	5.4		A
I _D	Drain current (continuous) at T _C = 100 °C	3 ⁽¹⁾	3		A
I _{DM} ⁽²⁾	Drain current (pulsed)	21.6 ⁽¹⁾	21.6		A
P _{TOT}	Total dissipation at T _C = 25 °C	30	110		W
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j max)	5.4			A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	100			mJ
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	2.5			kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	12			V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500			V
T _{stg}	Storage temperature	-55 to 150			°C
T _j	Max. operating junction temperature	150			°C

- Limited by package
- Pulse width limited by safe operating area
- I_{SD} ≤ 5.4 A, di/dt ≤ 400 A/μs, V_{DD} = 80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220FP	I ² PAKFP	I ² PAK	
R _{thj-case}	Thermal resistance junction-case max	4.17	1.14		°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	62.5	100		°C/W

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}$			0.8 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 9	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.7\text{ A}$		1.1	1.3	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	880	-	pF
C_{oss}	Output capacitance			65		pF
C_{rss}	Reverse transfer capacitance			12		pF
$C_{o(tr)}^{(1)}$	Eq. capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }520\text{ V}$	-	43	-	pF
$C_{o(er)}^{(2)}$	Eq. capacitance energy related			27		pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 500\text{ V}$, $I_D = 5.4\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 18)	-	33	-	nC
Q_{gs}	Gate-source charge			4		nC
Q_{gd}	Gate-drain charge			21		nC

- $C_{oss\text{ eq}}$: time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
- $C_{oss\text{ eq}}$: energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$, $I_D = 2.7 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 17)		14		ns	
t_r	Rise time			10		ns	
$t_{d(off)}$	Turn-off-delay time				44		ns
t_f	Fall time				24		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				5.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				21.6	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5.4 \text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 22)		285		ns
Q_{rr}	Reverse recovery charge			5100		nC
I_{RRM}	Reverse recovery current				14	A
t_{rr}	Reverse recovery time	$I_{SD} = 5.4 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 22)		330		ns
Q_{rr}	Reverse recovery charge			2500		nC
I_{RRM}	Reverse recovery current				15.5	A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0$ (open drain)	30		-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220FP and I²PAKFP

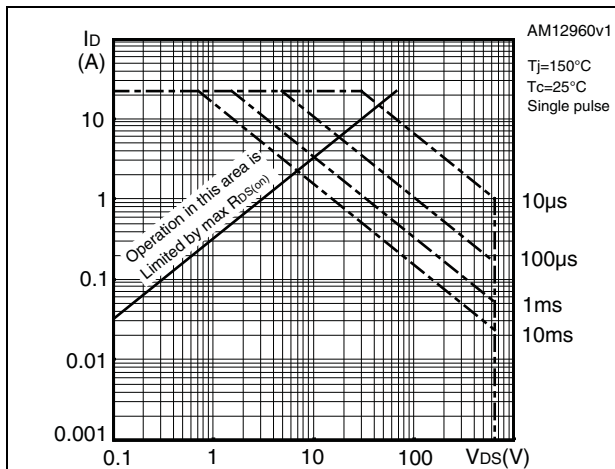


Figure 3. Thermal impedance for TO-220FP and I²PAKFP

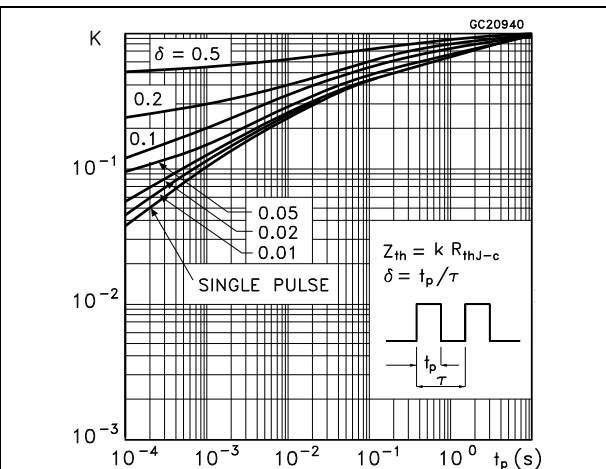


Figure 4. Safe operating area for IPAK

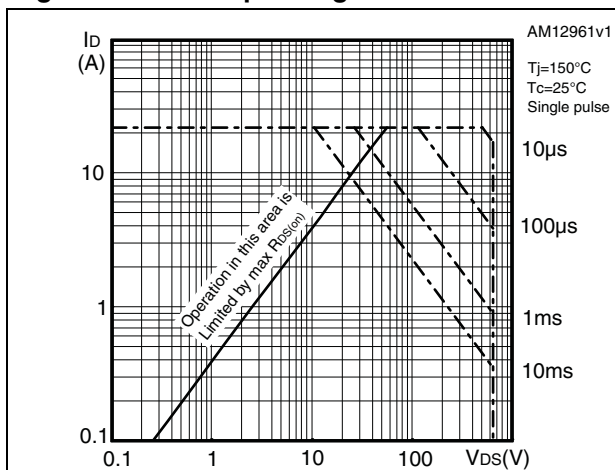


Figure 5. Thermal impedance for IPAK

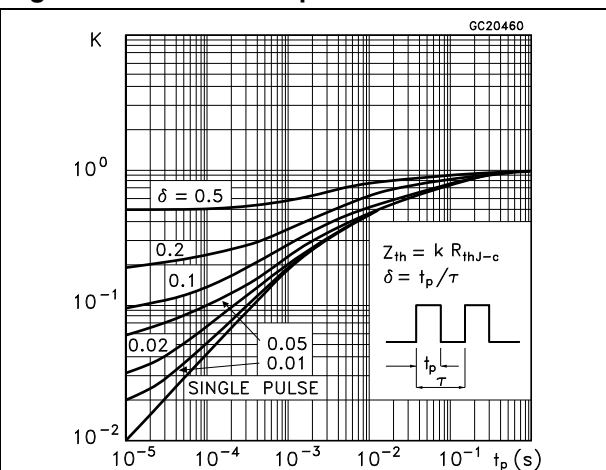


Figure 6. Output characteristics

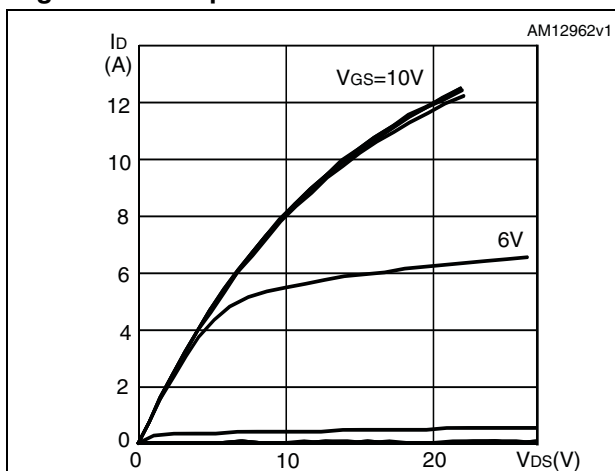


Figure 7. Transfer characteristics

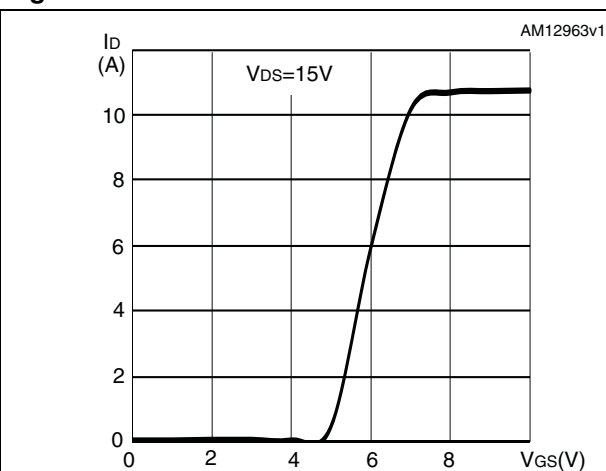


Figure 8. Gate charge vs gate-source voltage **Figure 9. Static drain-source on-resistance**

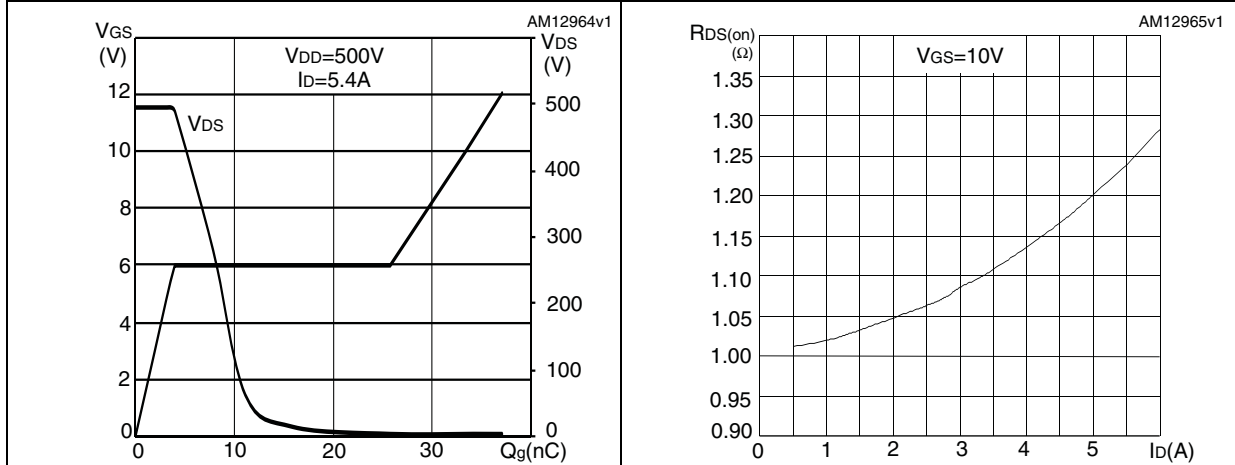


Figure 10. Capacitance variations **Figure 11. Output capacitance stored energy**

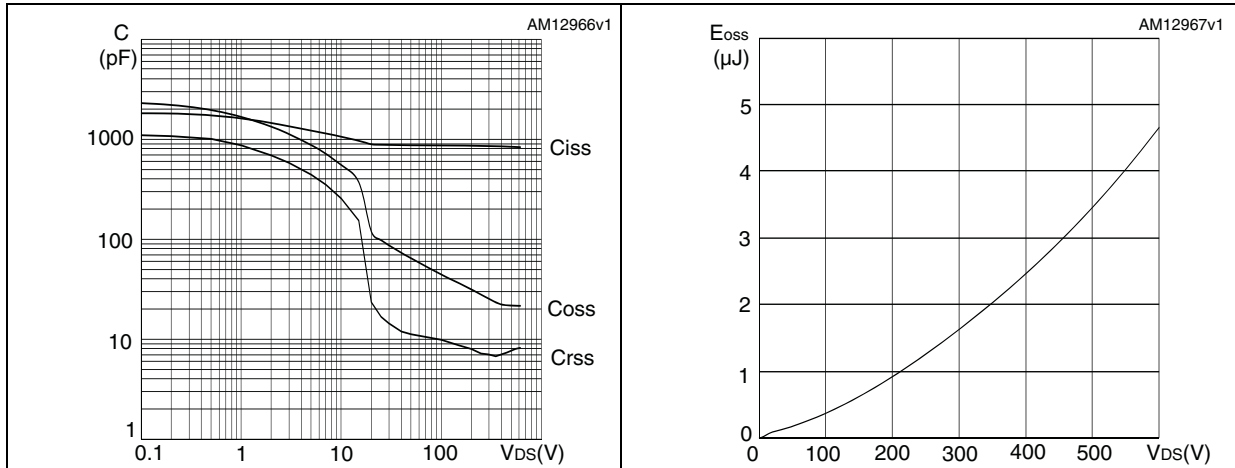


Figure 12. Normalized gate threshold voltage vs temperature **Figure 13. Normalized on-resistance vs temperature**

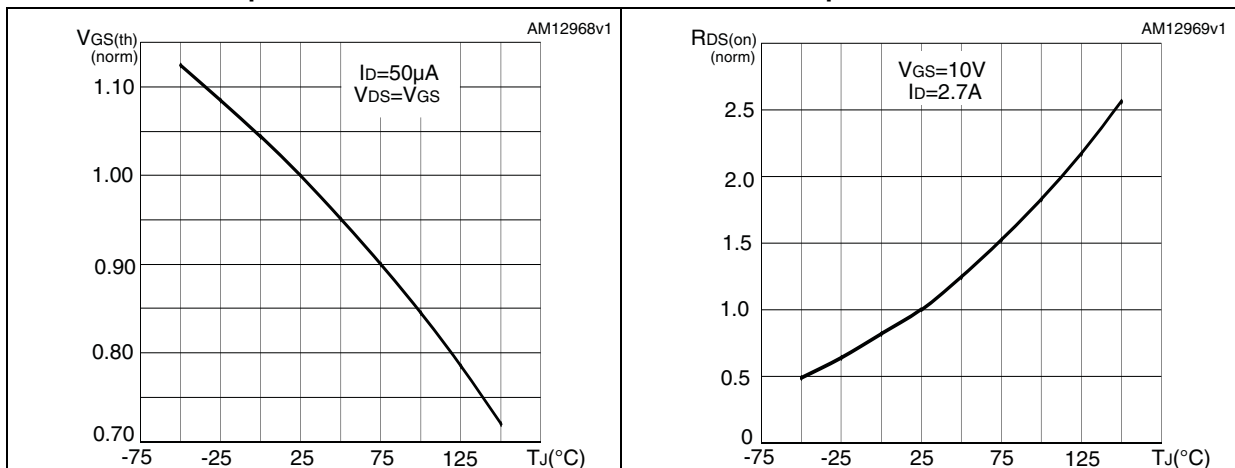


Figure 14. Normalized BV_{DSS} vs temperature

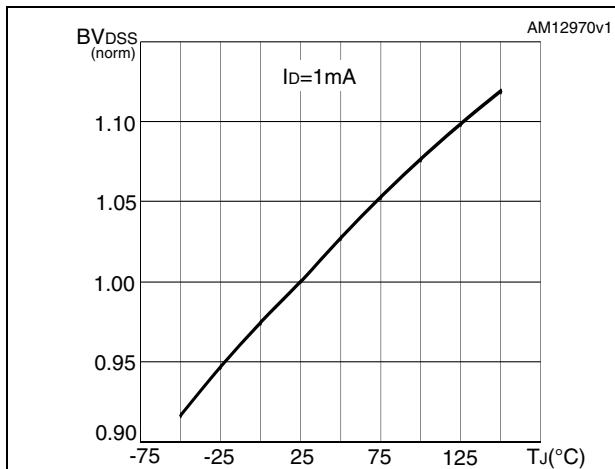


Figure 15. Source-drain diode forward characteristics

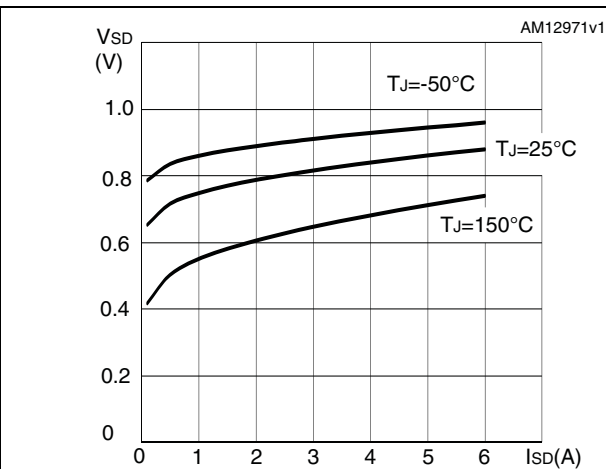
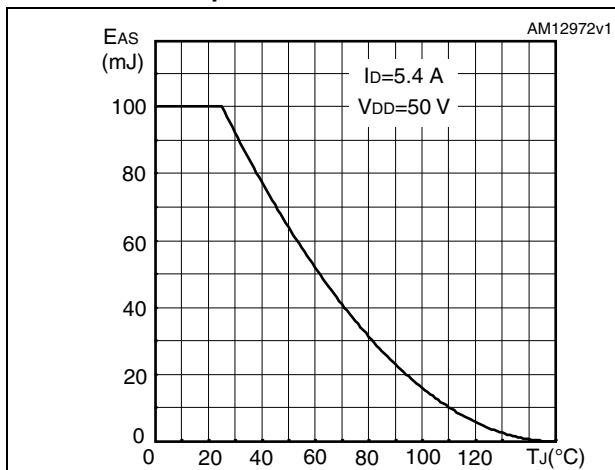


Figure 16. Maximum avalanche energy vs temperature



3 Test circuits

Figure 17. Switching times test circuit for resistive load



AM01468v1

Figure 18. Gate charge test circuit



AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times



AM01470v1

Figure 20. Unclamped inductive load test circuit



AM01471v1

Figure 21. Unclamped inductive waveform



AM01472v1

Figure 22. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing

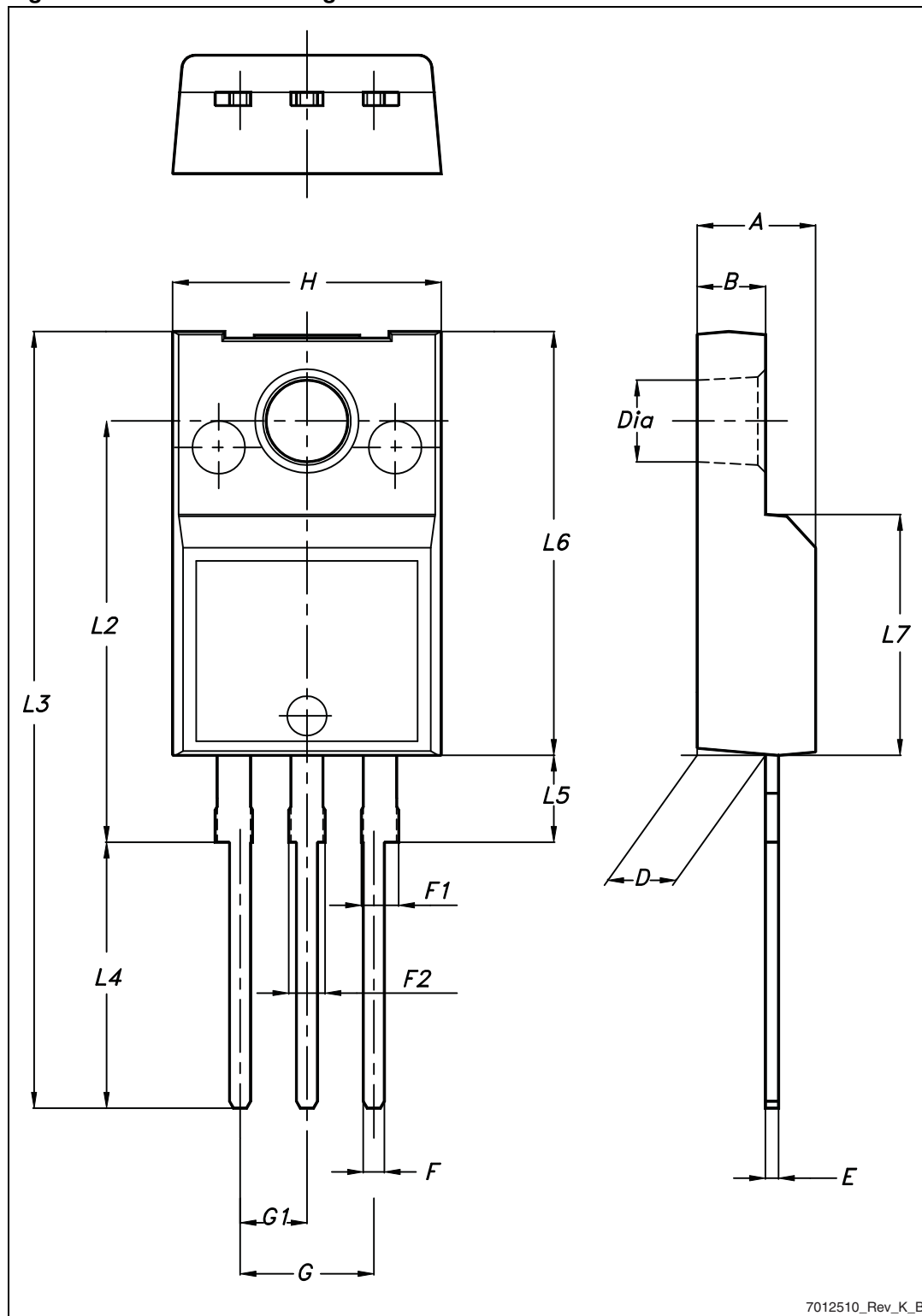


Table 10. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

Figure 24. I²PAKFP (TO-281) drawing

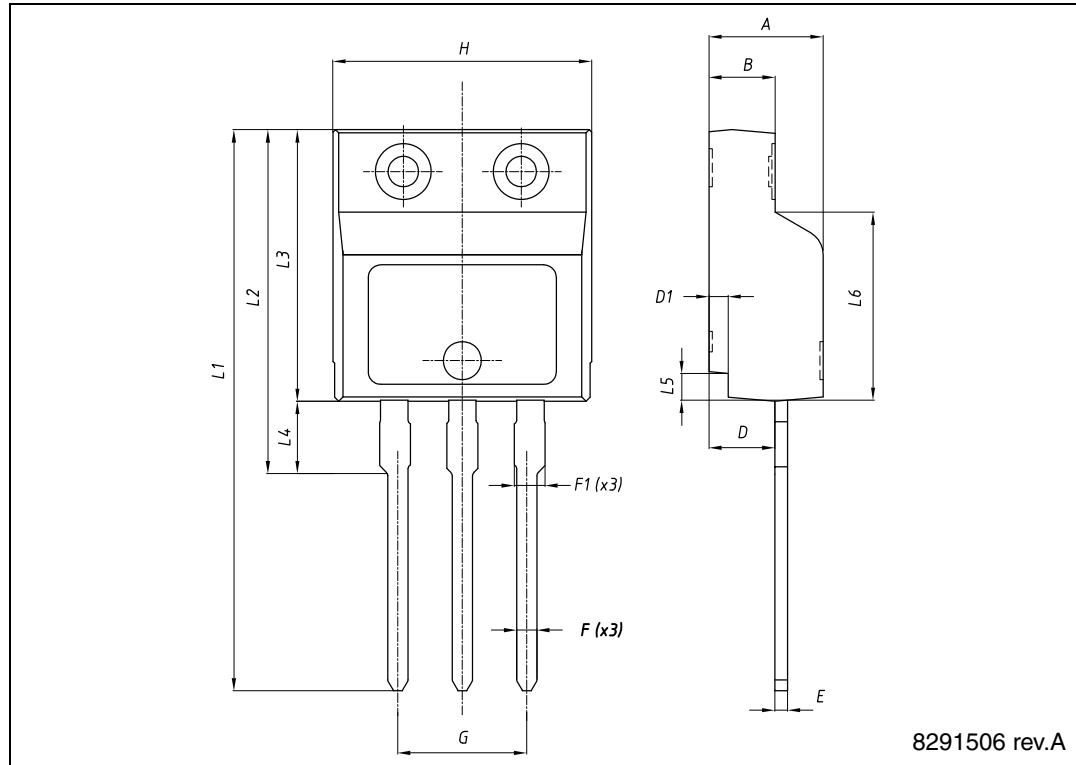
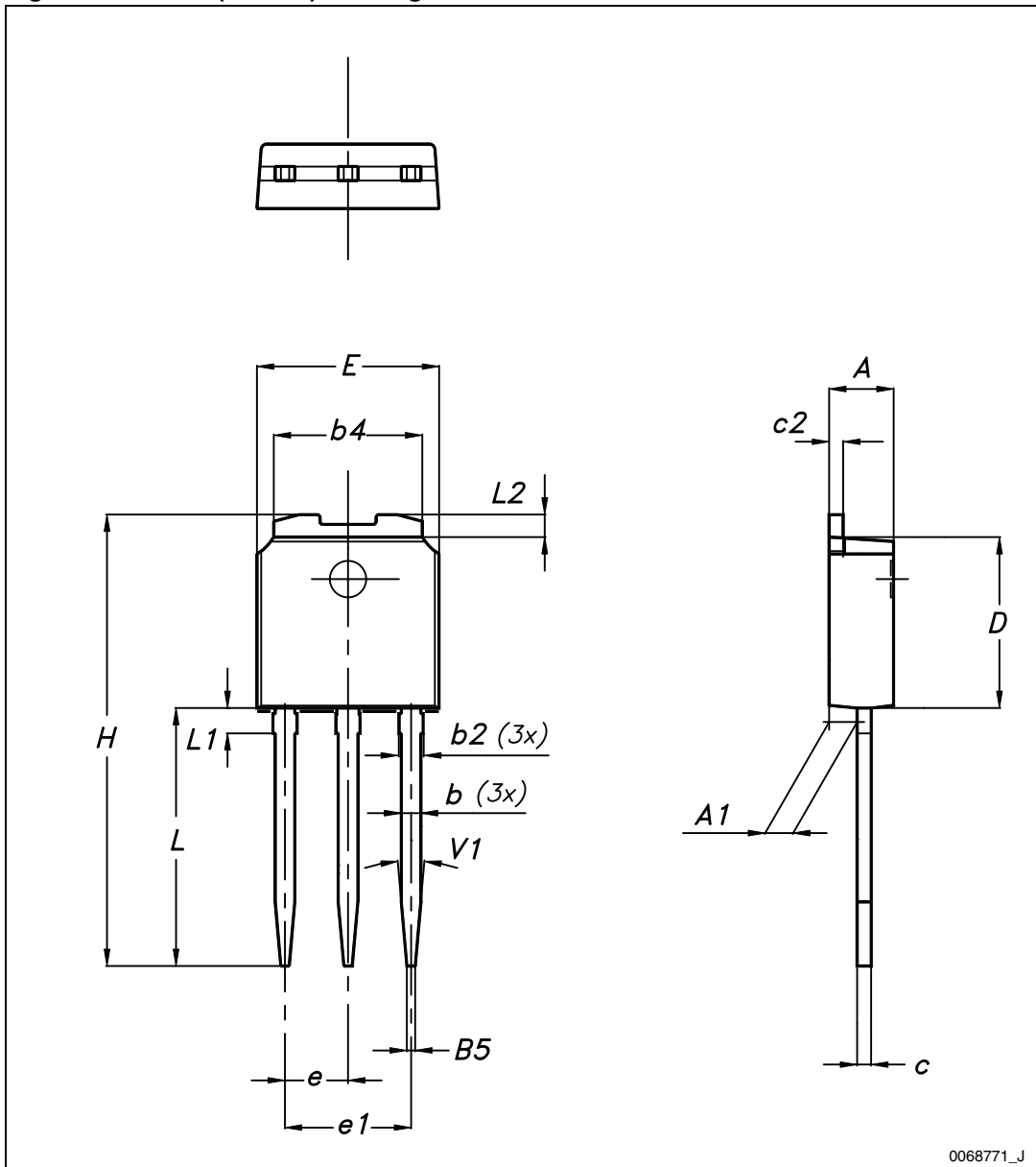


Table 11. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10 °	

Figure 25. IPAK (TO-251) drawing



0068771_J

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
05-Apr-2011	1	First release
07-Nov-2012	2	Added new part numbers: STF16N65K3 in I ² PAKFP package and STU6N65K3 in IPAK packages. Section 2.1: Electrical characteristics (curves) has been updated. Minor text changes.

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