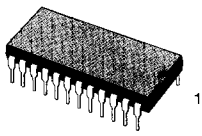
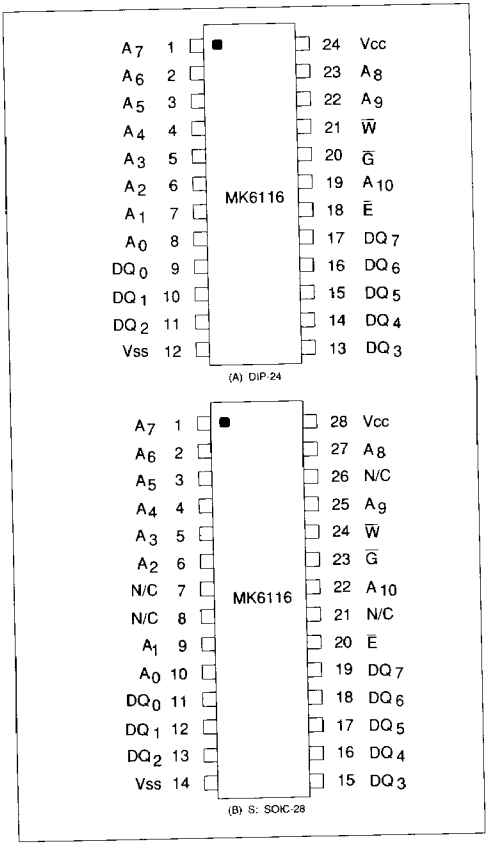
MK6116, MKI6116, MK6116L, MKI6116L (N/S) - 15/20/25
2 K X 8 CMOS STATIC RAM

- BYTEWYDE™ 2K x 8 CMOS STATIC RAM.
- +5 VOLT ONLY WRITE/READ.
- 24-PIN 600 MIL PLASTIC DIP, JEDEC PINOUT 28-PIN 330 MIL SOIC.
- EQUAL WRITE AND READ CYCLE TIMES.
- HIGH PERFORMANCE WITH LOW CMOS STANDBY POWER.



B
DIP 24
(Plastic Package)

PIN CONNECTION



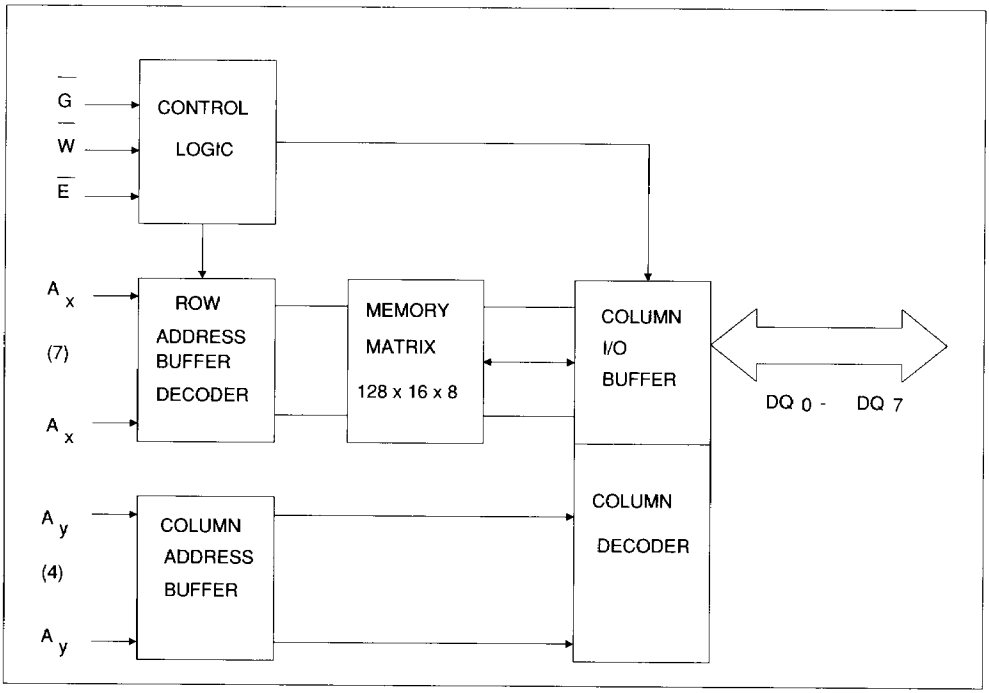
DESCRIPTION

The MK6116 is a 16,384-bit CMOS Static RAM, organized as 2K x 8 usingSGS-THOMSON Microelectronics' advanced HCMOS process technology. This device is directly compatible with the popular 24-pin, three-wire handshake, 16K static CMOS RAM. All inputs and outputs are TTL compatible using a single 5V supply. The MK6116 provides full static operation, requiring no clocks or refresh operations, and has equal access and cycle times. Additionally, whenever $\overline{E}$ (Chip Enable) goes high, the device will maintain a reduced power standby mode until $\overline{E}$ again goes active low. (Refer to the MK6116Truth Table.)

PIN NAMES

A_0 -A_{10}	ADDRESS INPUTS
DQ_0 - DQ_7	DATA I/O
$\overline{E}$	CHIP ENABLE
$\overline{G}$	OUTPUT ENABLE
$\overline{W}$	WRITE ENABLE
V_{CC}, V_{SS}	+5V, GND

FIGURE 1 : BLOCK DIAGRAM



MK6116 TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
V_{IH}	X	X	deselect	Hight Z	Standby
V_{IL}	X	V_{IL}	Write	D_{IN}	Active
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	V_{IH}	Read	Hight Z	Active

READ MODE

The MK6116 is in the read mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_0-A_{10}) defines which one of 2048 bytes of data is to be accessed.

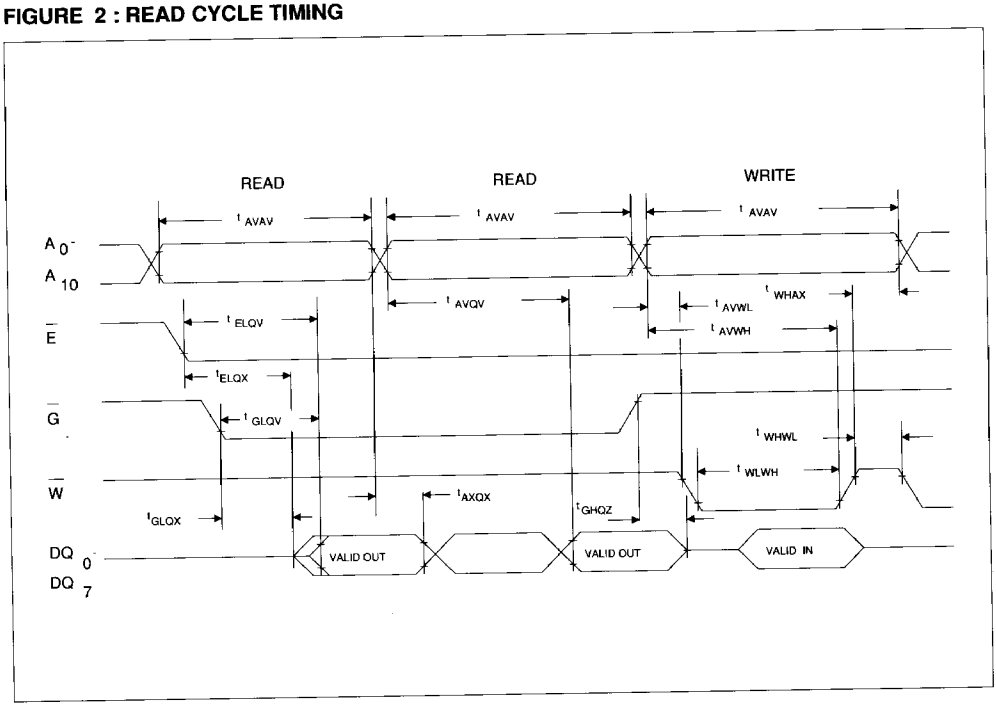
Valid data will be available at the eight Data Outputs Drivers (DQ_0-DQ_7) within t_{AVQV} after the last address input signal is stable, provided that the $\overline{E}$ and $\overline{G}$ (Out-put Enable) access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{ELQV} or t_{GLQV}) rather than address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ input signals. Data Out may be indeterminate between t_{AXQX} and t_{AVQV}, but data will always be valid at t_{AVQV}.

AC ELECTRICAL CHARACTERISTIICS (READ CYCLE)

{0°C ≤ TA ≤ +70°C (MK6116/L), -40°C ≤ TA ≤ + 105°C (MKI6116/L), VCC= 5.0 +/ - 10%}

ALT. SYMBOL	STD. SYMBOL	PARAMETER	MK6116 - 15 MKI6116 -15 MK6116L-15 MKI6116L-15		MK6116 - 20 MKI6116 -20 MK6116L-20 MKI6116L-20		MK6116 - 25 MKI6116 -25 MKL6116-25			
			MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	t_{AVAV}	Read Cycle Time	150		200		250		ns	
t_{AA}	t_{AVQV}	Address Access Time		150		200		250	ns	1
t_{CEA}	t_{ELQV}	ChipEnable Access Time		150		200		250	ns	1
t_{CEZ}	t_{EHQZ}	Chip Enable Data OffTime		35		40		50	ns	
t_{OEA}	t_{GLQV}	Output Enable Access Time		75		80		90	ns	1
t_{OEZ}	t_{GLQV}	Output Enable Data Off Time		35		40		50	ns	
t_{OEL}	t_{GLQX}	Out put Enable to Q Low-Z	15		15		15		ns	
t_{CEL}	t_{ELQX}	Chip Enable to Q Low-Z	15		15		15		ns	
t_{OH}	t_{AXQX}	Output Hold from Address	15		15		15		ns	1

FIGURE 2 : READ CYCLE TIMING



WRITE MODE

The MK6116 is in the Write Mode of operation whenever $\overline{W}$ and $\overline{E}$ are active low (G is a don't care as noted in the Truth Table). The latter occurring falling edge of either $\overline{W}$ or $\overline{E}$ will determine the start of the write cycle. Therefore, address setup time and write or chip enable pulse width are referenced to the latter occurring edge of $\overline{W}$ or $\overline{E}$. The write cycle can be terminated by either earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{W}$ must return to the high logic state for a minimum write recovery time designated as t_{WHWL} between write cycles. Addresses must remain valid for t_{WHAX} at the termination of the write cycle. The same principles apply for an $\overline{E}$ controlled write cycle.

If the output bus has been enabled ($\overline{E}$ and $\overline{G}$ active low), then $\overline{W}$ will disable the outputs within t_{WLQZ} from its falling edge; however, care must be taken to avoid a potential bus contention. Data-In must be valid t_{DVWH} or t_{DVEH} prior to the earlier rising

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

{0°C ≤ T_A ≤ +70°C (MK6116/L), -40°C≤ T_A ≤ +105°C (MKI6116/L), V_{CC}=5.0 ± 10%}

ALT. SYMBOL	SDT. SYMBOL	PARAMETER	MK6116 - 15 MKI6116 -15 MK6116L-15 MKI6116L-15		MK6116 - 20 MKI6116 -20 MK6116L-20 MKI6116L -20		MK6116 - 25 MKI6116 -25 MKL6116-25			
			MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WC}	t_{AVAV}	Write Cycle Time	150		200		250		ns	
t_{AS}	t_{AVWL}	Address Setup Time $\overline{W}$ Low	0		0		0		ns	
t_{AS}	t_{AVEL}	Address Setup Time $\overline{E}$ Low	0		0		0		ns	
t_{CEW}	t_{ELEH}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	t_{AVWH}	Address Valid to End of Write	120		140		180		ns	
t_{AW}	t_{AVEH}	Address Valid to End of Write	120		140		180		ns	
t_{WEW}	t_{WLWH}	Write Pulse Width	90		120		160		ns	
t_{AH}	t_{WHAX}	$\overline{W}$ Hight to address Change	10		10		10		ns	
t_{AH}	t_{EHAX}	$\overline{E}$ Hight to address Change	10		10		10		ns	
t_{WR}	t_{WHWL}	$\overline{W}$ Hight to $\overline{W}$ Low Next Cycle	10		10		10		ns	
t_{WEZ}	t_{WLQZ}	$\overline{W}$ Data Off Time		50		60		80	ns	
t_{CEZ}	t_{EHQZ}	$\overline{E}$ Data Off Time		50		60		80	ns	
t_{DS}	t_{DVWH}	Data Setup Time to $\overline{W}$ Hight	40		60		100		ns	
t_{DS}	t_{DVEH}	Data Setup Time to $\overline{E}$ Hight	40		60		100		ns	
t_{DH}	t_{WHDX}	Data Hold Time $\overline{W}$ High	0		0		0		ns	
t_{DH}	t_{EHDX}	Data Hold Time $\overline{E}$ High	0		0		0		ns	

FIGURE 3 : WRITE CYCLE TIMING

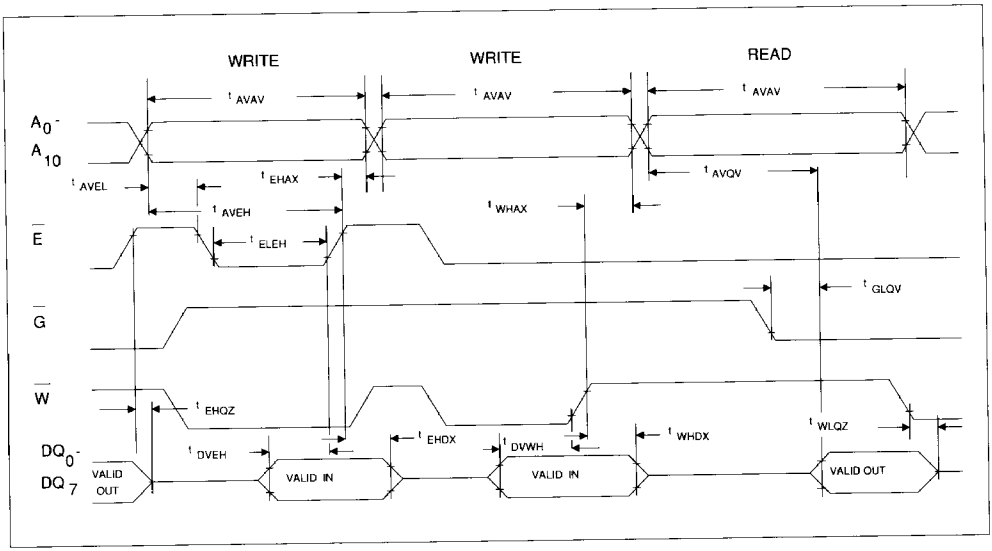
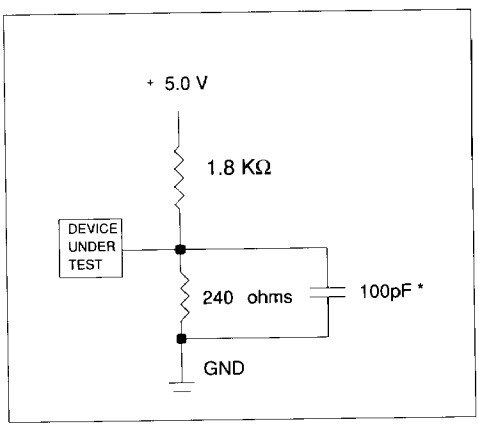


FIGURE 4 : OUTPUT LOAD DIAGRAM



*Notes: Including scope and JIG

AC TEST CONDITION

Input Levels: . . . . . 0.6 V to 2.4 V

Transition Times: . . . . . 5 ns

Input and Output Timing
Reference Levels: . . . . . 0.8V or 2.2 V

ABOLUTE MAXIMUM RATINGS *

PARAMETER	VALUES	UNITS
Voltage on any Pin Relative tro Ground	-0.3 to +7.0	V
Operating Temperature (MK6116L)	0 to +7	°C
Operatting Temperature (MKI6116/L)	-40 to +150	°C
Storage Temperature	-55 to +150	°C
Power Dissipation	1	W
Output Current	† 20	mA

* This is a stress rating only and functional operation of the device at these or any conditions above those indicazted in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliabiliy.

† Output current absolute maximun rating is specified for one output at a time, not to exceed a duration of a1 second.

RECOMMENDED DC OPERATING CONDITIONS

{0°C ≤ T_A ≤ +70°C (MK6116/L), -40°C ≤ T_A ≤ +150°C (MKI6116/L), V_{CC}=5.0 +/- 10%}

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.5.	V	4
V_{SS}	Supply Voltage	0	0	V	4
V_{IH}	Logic 1 All Inputs	2.2	V_{cc} +0.3	V	4
V_{IL}	Logic 1 All Inputs	-0.3	0.8	V	4,5

DC ELECTRICAL CHARACTERISTICS

{0°C ≤ TA ≤ +70°C (MK6116/L), -40°C ≤ T_A ≤ +150°C (MKI6116/L), V_{CC}=5.0 +/- 10%}

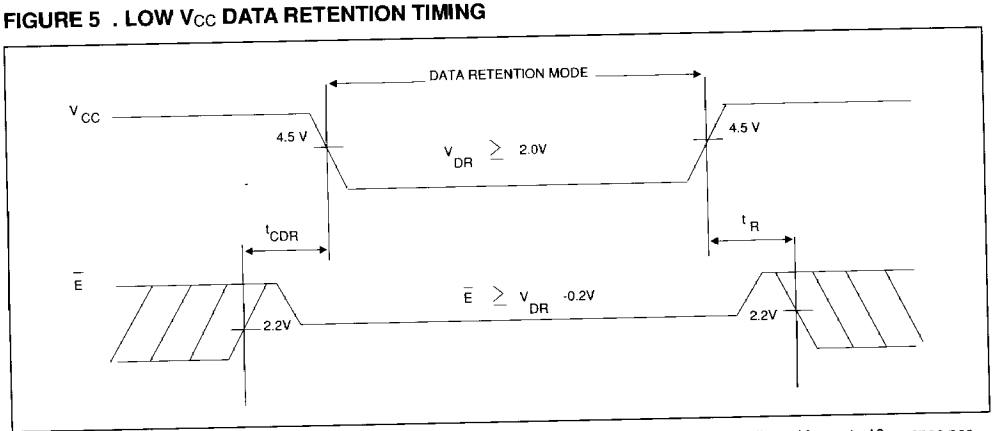
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	Average V_{CC} Power Supply Current ,		70	mA	6
	MK6116, MKI6116				
	MK6116L, MKI6116L		70	mA	
I_{SB1}	TTL Standby Current ($\overline{E}$ = V_{IH})		3	mA	
I_{SB2}	CMOS Standby Current ($\overline{E}$ ≥ V_{CC}-0.2 V)		1	mA	
	MK6116, MKI6116				
	MK6116L			µA	
	MKI6116L		10	µA	
I_{LI}	Input Leakage Current	-1	+1	µA	7
I_{LO}	Output Leakage Current	-5	+5	µA	7
V_{OH}	Output Logic 1 Voltage (I_{OH} = -1.0 mA)	2.4		V	
V_{OL}	Output Logic 2 Voltage (I_{OH} = 2.1 mA)		0.4	V	

LOW V_{CC} Data RETENTION CHARACTERISTICS (MK6116L, MKI6116L)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{DR}	V_{CC} Data retention	2.0	V_{CC} (max)		
$I_{CC}DR$	Data Retention Power Supply Current		1	µA	8
	MK6116L				
	MKI6116L		3	µA	
t_{CDR}	Chip Deselection to Data Retention Time	0		ns	
t_R	Operation Recovery Time	t_{AVAV}*			

* tAVAV = Read Cycle Time

FIGURE 5 . LOW V_{CC} DATA RETENTION TIMING



NOTES:

1 . Measured with load as shown in Figure 4.

2 . Effective capacitance calculated from the equation:
C= IΔt/ΔV, with ΔV = 3 volts and power supply at nominal level

3 . Output is deselected.

4 . All voltages referenced to GND.

5 . Negative spikes of -1.0 volts allowed for up to 10 ns once per cycle.

6 . ICC1 measured with output open.

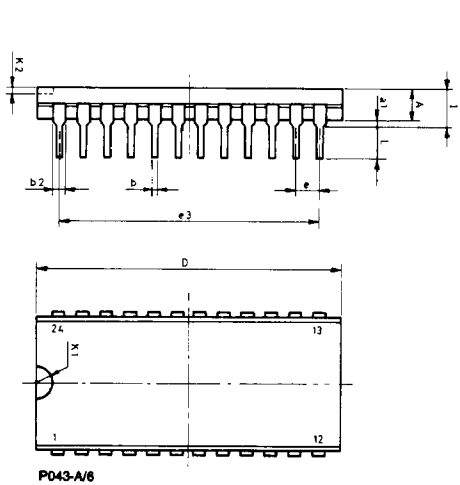
7 . Measured with GND ≤ V ≤ V_{CC} and outputs deselected.

8 . V_{CC} = 2.0 Volts.

CAPACITANCE (TA = 25°C)

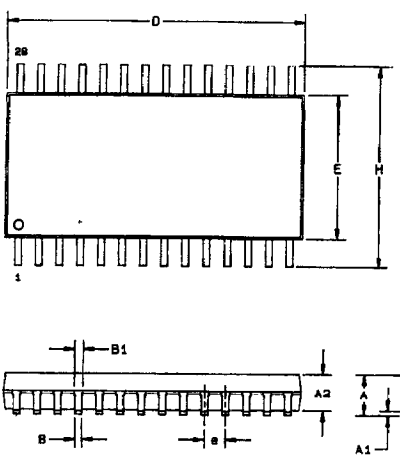
SYMBOL	PARAMETER	MAX	UNITS	NOTES
C_I	Capacitance on all pins (except DQ)	7.0	P^F	2
C_{DQ}	Capacitance on DQ pins	10.0	P^F	2, 3

FIGURE 6 . 24-PIN PLASTIC DIP (N)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A						
a1		0.63			0.024	
B		0.45			0.017	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
C						
D			32.20			1.267
E	15.20		16.68	0.598		0.656
e		2.54			0.100	
e3		27.94			1.100	
e4						
F			14.10			0.555
I	4.45		0.175			
L	3.30		0.129			
K1						
K2						

FIGURE 7 . 28-PIN SOIC (S)



Dim.	Inches	
	Min.	Max.
A		.120
A1	.002	.014
A2	.092	.106
B	.014	.020
B1	.014	.024
C	.006	.0125
D	.697	.728
E	.324	.350
e	.050 Basic	
H	.453	.500
L	.016	.050
α	0°	8°

ORDERING INFORMATION

PART N0.	ACCESS TIME	CYCLE TIME	PACKAGE TYPE	TEMPERATURE
MK6116 (N/S)-15	150 ns	150 ns	Plastic DIP/SOIC	0°C to 70°C
MK6116 (N)-20	200 ns	200 ns	Plastic DIP	0°C to 70°C
MK6116 (N) -25	250 ns	250 ns	Plastic DIP	0°C to 70°C
MKI6116 (N/S) -15	150 ns	150 ns	Plastic DIP/SOIC	-40°C to 105°C
MKI6116 (N) -20	200 ns	200 ns	Plastic DIP	-40°C to 105°C
MKI6116 (N) - 25	250 ns	250 ns	Plastic DIP	-40°C to 105°C
MK6116 L(N/S) -15	150 ns	150 ns	Plastic DIP/SOIC	0°C to 70°C
MK6116 L(N) - 20	200 ns	200 ns	Plastic DIP	0°C to 70°C
MK6116 L(N) - 25	250 ns	250 ns	Plastic DIP	0°C to 70°C
MKI6116 L(N/S) - 15	150 ns	150 ns	Plastic DIP/SOIC	-40°C to 105°C
MKI6116L (N) - 20	200 ns	200 ns	Plastic DIP	-40°C to 105°C

MK _____ Commercial Temperature Range (0°C to +70°C)

MKI _____ Industrial Temperature Range (-40°C to +85°C)

6116 _____ Device Family and Identification Number

L _____ Low Power

N _____ Plastic Dip Package

S _____ SOIC Package

15/20/25 _____ Speed Grade

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