



# STD20NF06L

## N-CHANNEL 60V - 0.032 Ω - 24A DPAK/IPAK STripFET™ II POWER MOSFET

Table 1: General Features

TYPE	V <sub>DSS</sub>	R <sub>D(on)</sub>	I <sub>D</sub>
STD20NF06L	60 V	< 0.040 Ω	24 A
STD20NF06L-1	60 V	< 0.040 Ω	24 A

- TYPICAL R<sub>D(on)</sub> = 0.032 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- POWER TOOLS
- AUTOMOTIVE ENVIRONMENT

Figure 1: Package

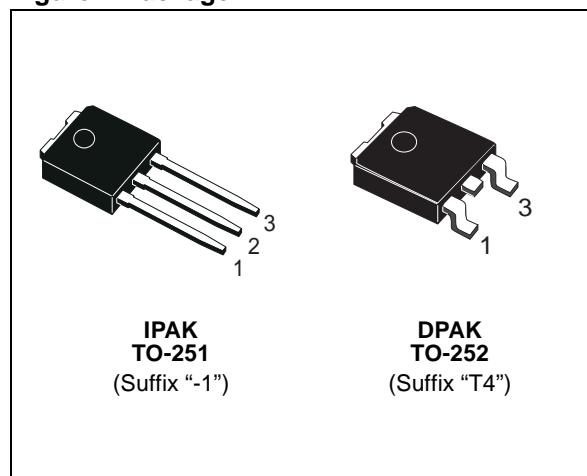


Figure 2: Internal Schematic Diagram

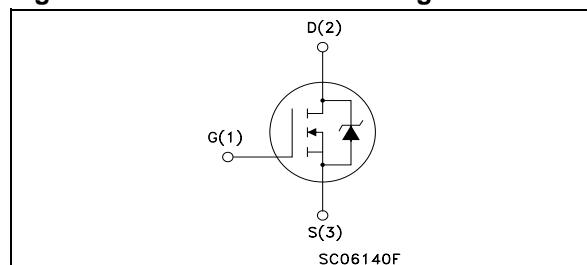


Table 2: Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD20NF06L	D20NF06L	TO-252	TAPE & REEL
STD20NF06L-1	D20NF06L	TO-251	TUBE

Table 3: ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	60	V
V <sub>GS</sub>	Gate-source Voltage	± 18	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	24	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	17	A
I <sub>DM(•)</sub>	Drain Current (pulsed)	96	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	60	W
	Derating Factor	0.4	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	10	V/ns
E <sub>AS</sub> (2)	Single Pulse Avalanche Energy	225	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

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**Table 4: THERMAL DATA**

R <sub>thj-case</sub> R <sub>thj-pcb</sub> T <sub>j</sub>	Thermal Resistance Junction-case (*) Thermal Resistance Junction-PCB Maximum Lead Temperature For Soldering Purpose (1.6 mm from case, for 10 sec)	Max Max	2.5 50 275	°C/W °C/W °C
-----------------------------------------------------------------	-------------------------------------------------------------------------------------------------------------------------------------------------------------	------------	------------------	--------------------

(\*) When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz of Cu

## ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

**Table 5: OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 18 V			±100	nA

**Table 6: ON (\*)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 12 A V <sub>GS</sub> = 5 V I <sub>D</sub> = 12 A		0.032	0.040 0.050	Ω Ω

**Table 7: DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 25 V I <sub>D</sub> = 12 A		20		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V f = 1 MHz V <sub>GS</sub> = 0		660 170 70		pF pF pF

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### ELECTRICAL CHARACTERISTICS (continued)

**Table 8: SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30 \text{ V}$ $I_D = 10 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 5 \text{ V}$ (Resistive Load, Figure 17)		11 50		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 30 \text{ V}$ $I_D = 20 \text{ A}$ $V_{GS} = 10 \text{ V}$		13 3.5 8		nC nC nC

**Table 9: SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30 \text{ V}$ $I_D = 10 \text{ A}$ $R_G = 4.7 \Omega$ , $V_{GS} = 5 \text{ V}$ (Resistive Load, Figure 17)		20 12		ns ns

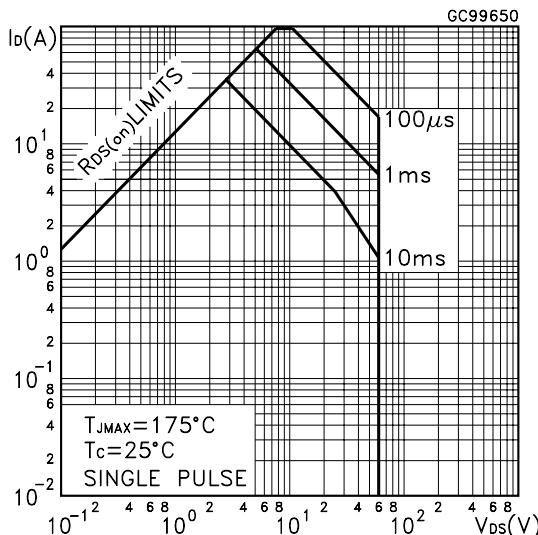
**Table 10: SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				24 96	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 20 \text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 20 \text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 19)		56 108 4		ns nC A

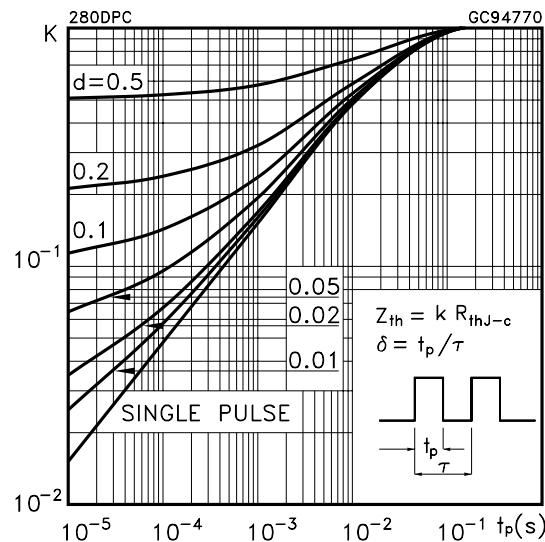
(\*)Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.

**Figure 3: Safe Operating Area**

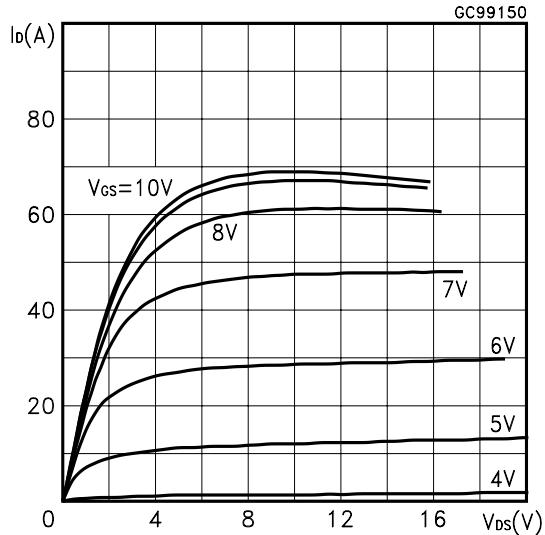


**Figure 4: Thermal Impedance**

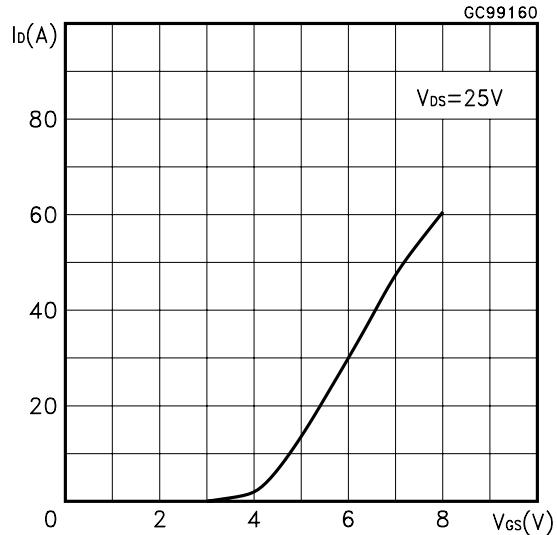


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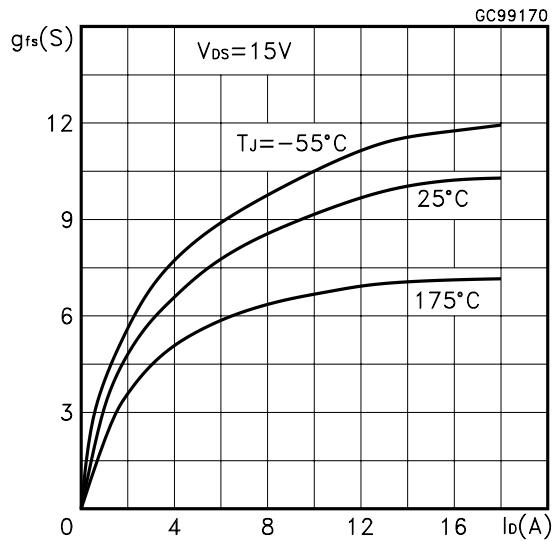
**Figure 5:** Output Characteristics



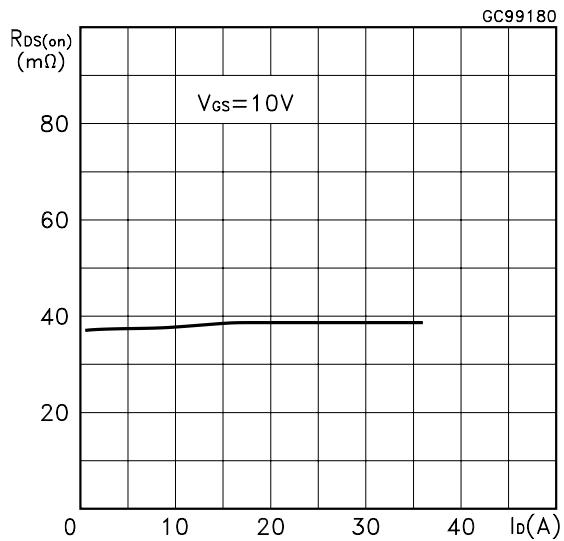
**Figure 6:** Transfer Characteristics



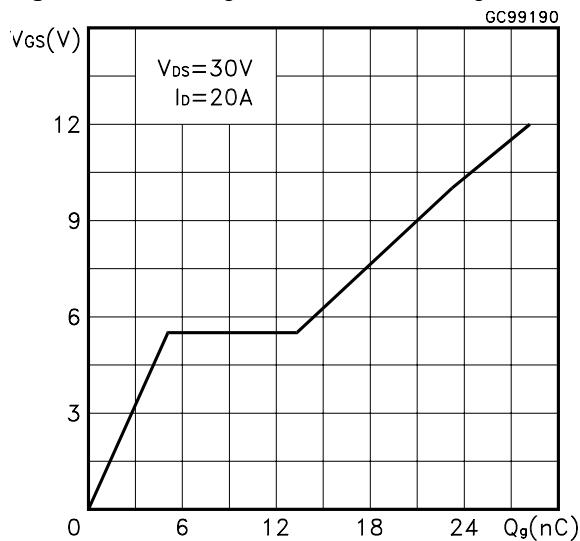
**Figure 7:** Transconductance



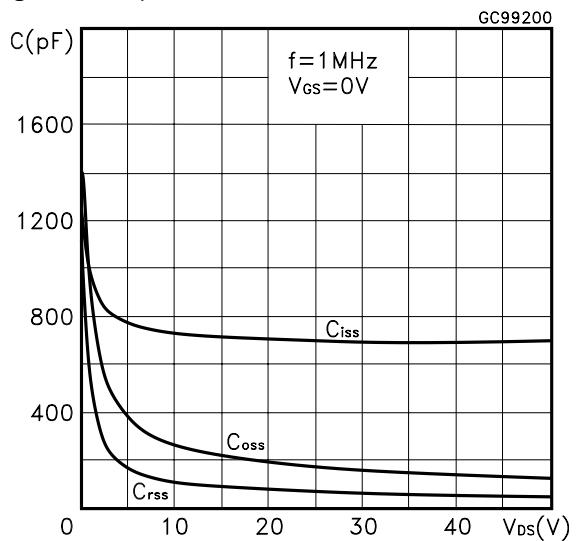
**Figure 8:** Static Drain-source On Resistance



**Figure 9:** Gate Charge vs Gate-source Voltage

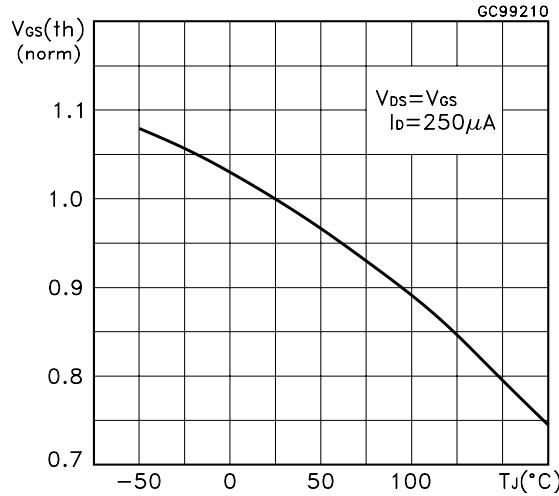


**Figure 10:** Capacitance Variations

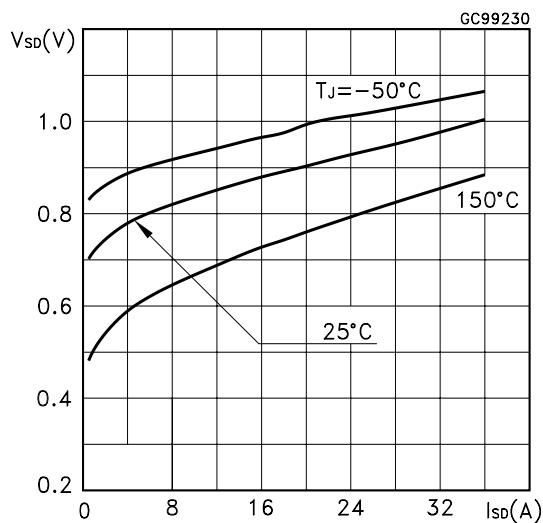


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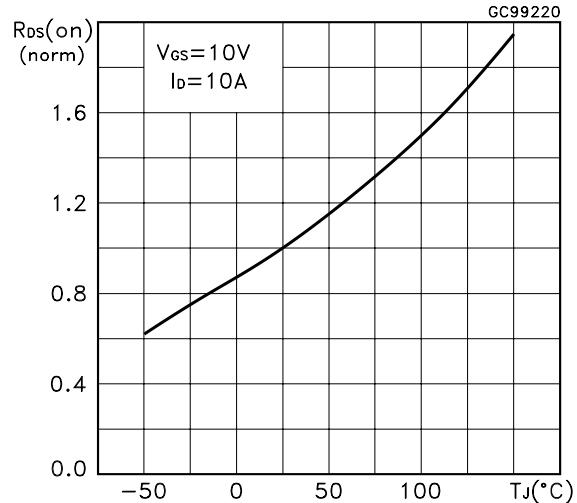
**Figure 11:** Normalized Gate Threshold Voltage vs Temperature



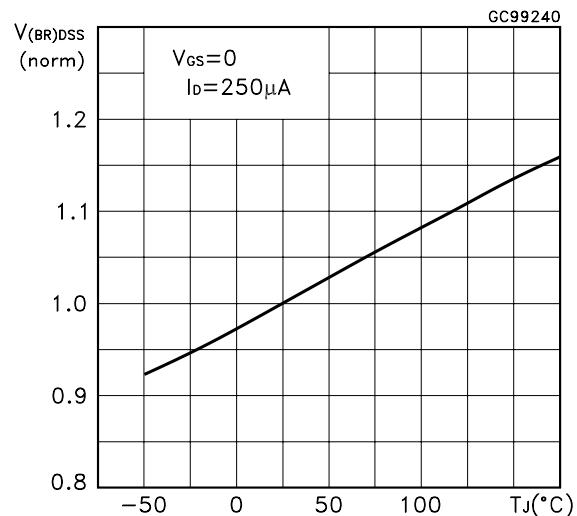
**Figure 13:** Source-drain Diode Forward Characteristics



**Figure 12:** Normalized on Resistance vs Temperature

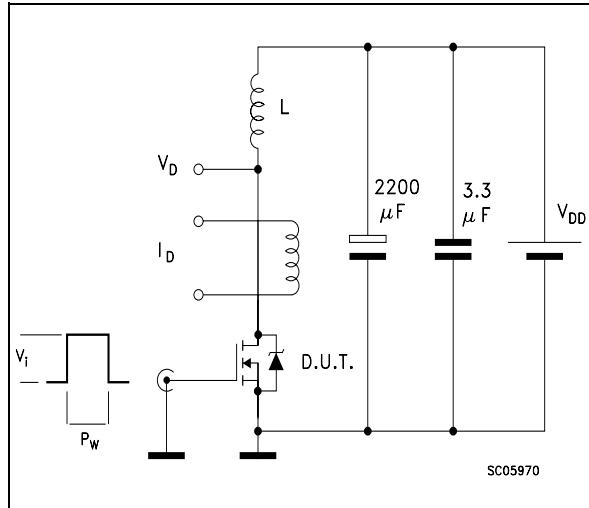


**Figure 14:** Normalized Breakdown Voltage vs Temperature.

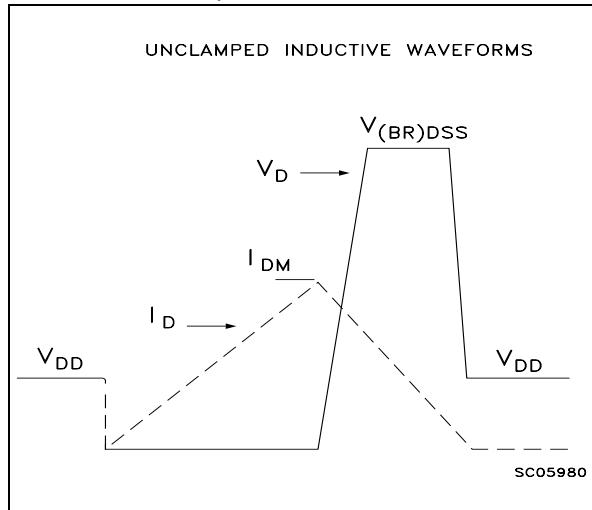


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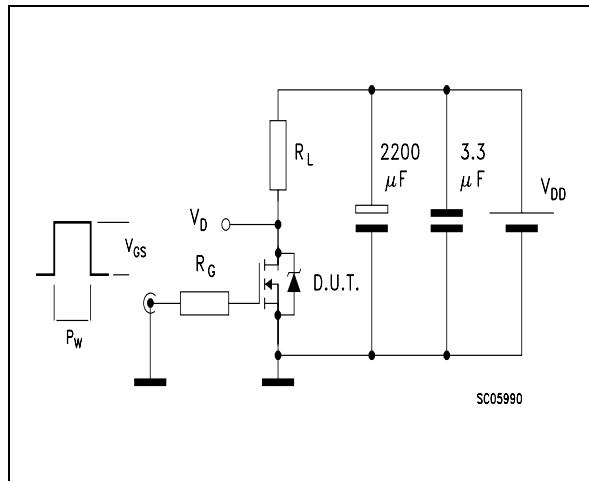
**Figure 15:** Unclamped Inductive Load Test Circuit



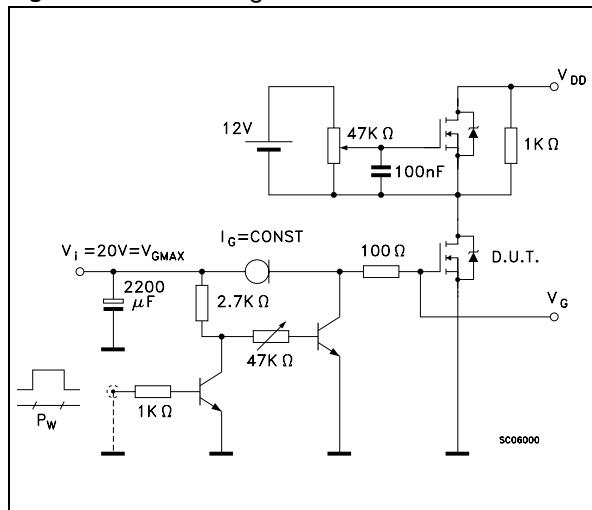
**Figure 16:** Unclamped Inductive Waveform



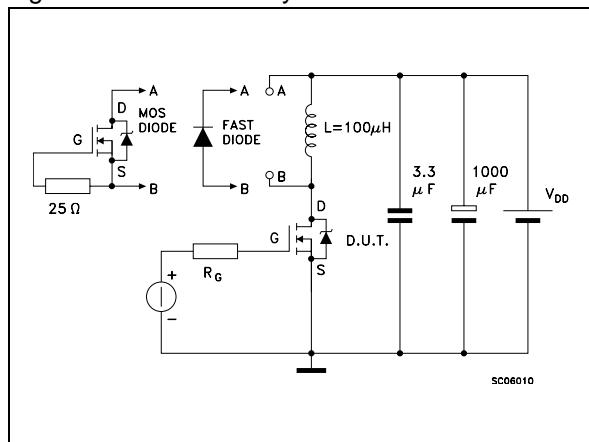
**Figure 17:** Switching Times Test Circuits For Resistive Load



**Figure 18:** Gate Charge test Circuit

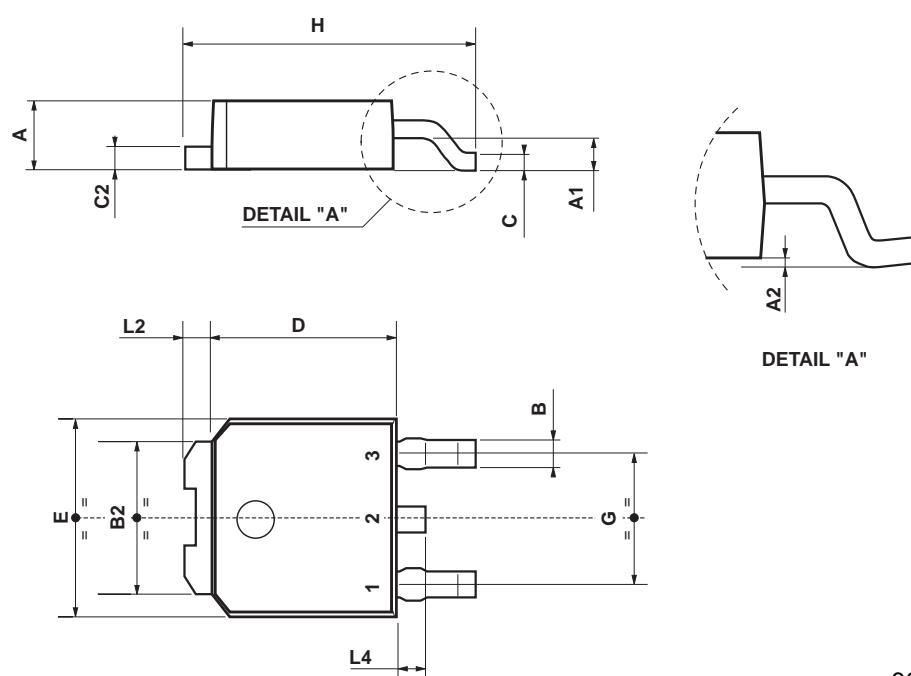


**Figure 19:** Test Circuit For Inductive Load Switching And Diode Recovery Times



## TO-252 (DPAK) MECHANICAL DATA

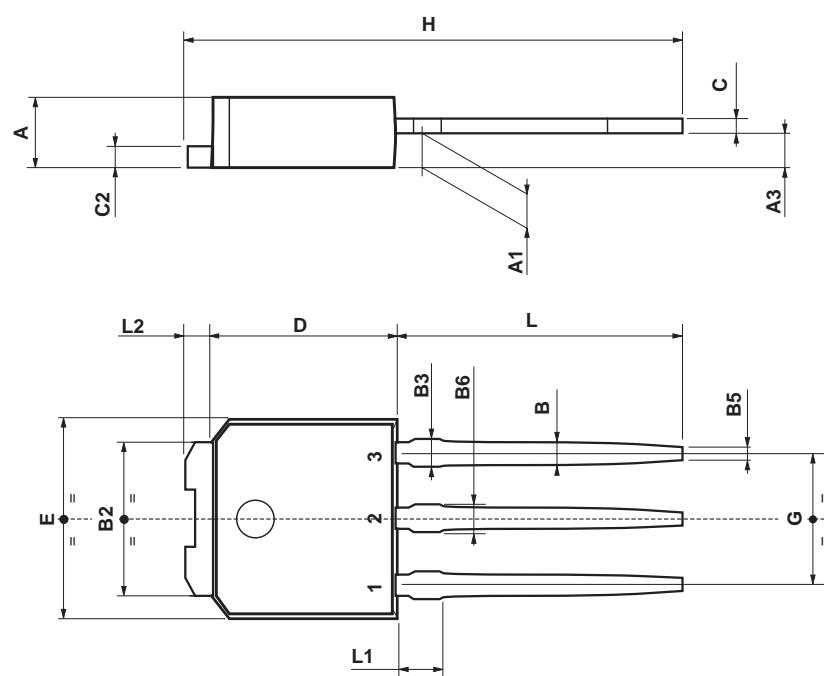
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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## TO-251 (IPAK) MECHANICAL DATA

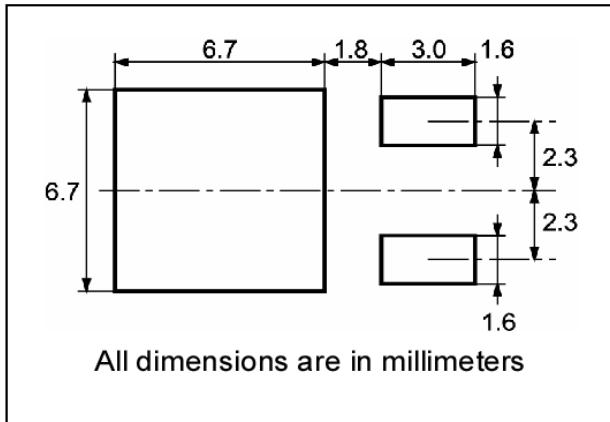
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



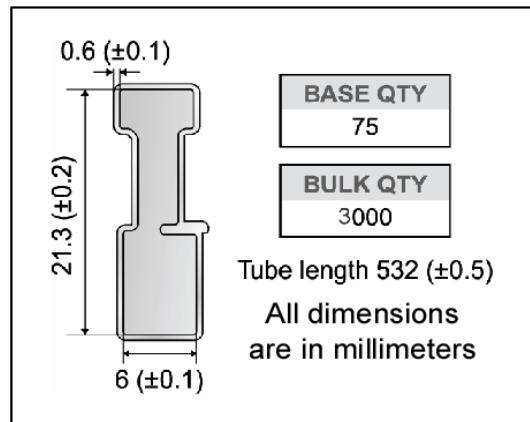
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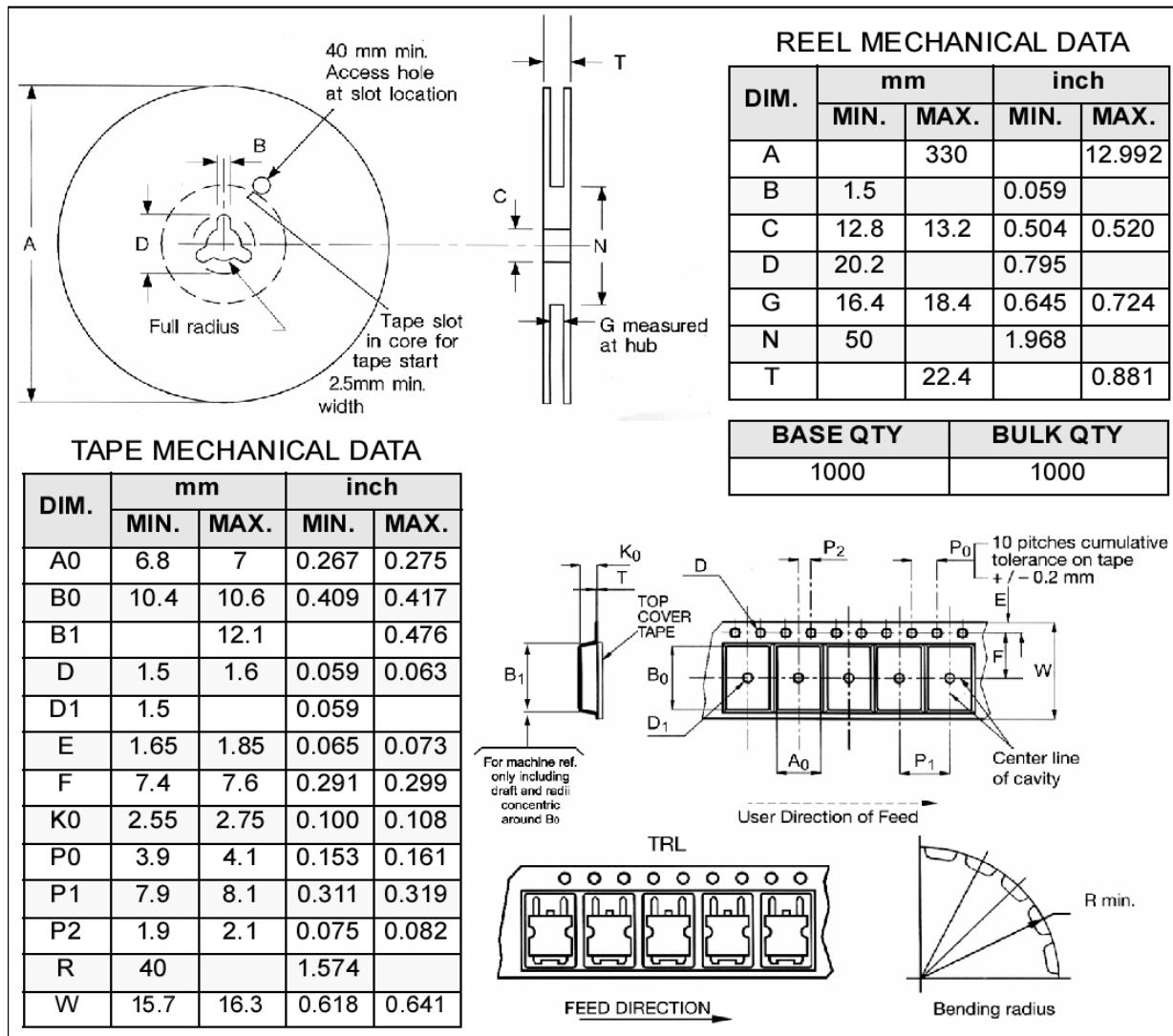
### DPAK FOOTPRINT



### TUBE SHIPMENT (no suffix)\*



### TAPE AND REEL SHIPMENT (suffix "T4")\*



\*on sales type

**STD20NF06L**

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**Table 11:Revision History**

Date	Revision	Description of Changes
Friday 15 April 2005	1.0	FIRST ISSUE
April 2005	2.0	ADDED PACKAGE IPAK

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