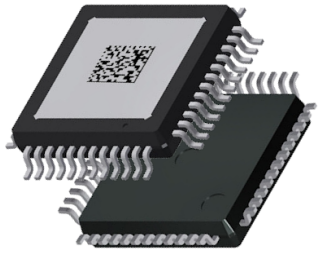
# HFDA80D

Data brief

# 4-channel digital input class-D automotive audio amplifier with Hi-Fi audio quality, in-play diagnostics, 2 MHz switching frequency



**LQFP48L exposed pad up (7x7x1.4 mm)**

| Product summary | | |
|---|---|---|
| **Order code** | **Package** | **Packing** |
| HFDA80D-F2Y | LQFP48L 7x7x1.4 mm | Tray |
| HFDA80D-F2T | | Tape and reel |

## Features

- AEC-Q100 qualified
- Supply operating range: 4.5 V–18 V
- EMI compliance evaluated according to CISPR25
- Class-D BTL outputs
- Integrated 112 dB D/A conversion
- Battery load dump compatible (40 V)
- Reduced size and cost of output LC thanks to 2 MHz switching PWM
- $I^2S$ and TDM digital input (up to 16 channels TDM)
- Selectable input sample rate frequency (44.1/48/96/192 kHz)
- Multiple load configurations:
  - Able to drive 4 Ω and 2 Ω speaker loads
- MOSFET power outputs allowing high output power capability:
  - Typ. 4x29 W on 4 Ω at 14.4 V, 1 kHz, THD = 10%
  - Typ. 4x22.5 W on 4 Ω at 14.4 V, 1 kHz, THD = 1%
  - Typ. 4x47.5 W on 2 Ω at 14.4 V, 1 kHz, THD = 10%
  - Typ. 4x35.5 W on 2 Ω at 14.4 V, 1 kHz, THD = 1%
- Outstanding audio performances
  - THD 0.015% typ. at 1 W 1 kHz on 4 Ω loads
  - Output noise 27 µV typ. A-weighted
  - Crosstalk 100 dB typ. at 1 W 1 kHz on 4 Ω loads
  - PSRR 80 dB typ. at 1 W 1 kHz on 4 Ω loads
- Fast turn-on and very low latency for high-speed audio processing applications
- Very low latency for noise cancelling application
- I²C full configurability with channel independent mute/play/gain selection/ diagnostic
- 4 I²C addresses
- Full diagnostic matrix with info available both on I²C and CD/DIAG pin:
  - 4 thermal warnings
  - Independent by-channel DC and AC load detection diagnostic with selectable threshold
  - Startup diagnostic for shorts to VCC/GND
  - OCP protection with configurable OCP limit (2 selectable)
  - Input offset detector
  - Free-running diagnostics
    - Output current offset detector
    - DC/AC diagnostic
    - Including open-load in play detection
- Synchronization output pin
- Immune to pop/tick noise at turn on/off, battery variations, during diagnostic
- Legacy (backup mode without I²C control)
- Integrated short circuit protections

- ESD integrated protections (2 kV HBM, 500 V / 750 V corner CDM)
- LQFP48L exposed pad up package

## Description

The HFDA80D is a new STMicroelectronics class-D audio amplifier, specifically designed for automotive applications in the latest BCD technology.

The HFDA80D integrates advanced solutions for an excellent GSM noise immunity combined with the advantages of 2 MHz switching PWM class-D output stages. This configuration allows outstanding audio performance while designing a compact and inexpensive application.

The HFDA80D supports wide band applications up to 40 kHz, with extremely low level of noise and low THD.

Moreover, it features a broad diagnostics matrix, to support the most demanding OEM requirements in terms of speaker control and system robustness/reliability. The HFDA80D supports start/stop cranking down to 4.5 V and is housed in a very compact and thin LQFP48L 7x7x1.4 mm package, making it suitable for any level of automotive application.

# 1 Block diagram and pin description

Figure 1. **Block diagram**

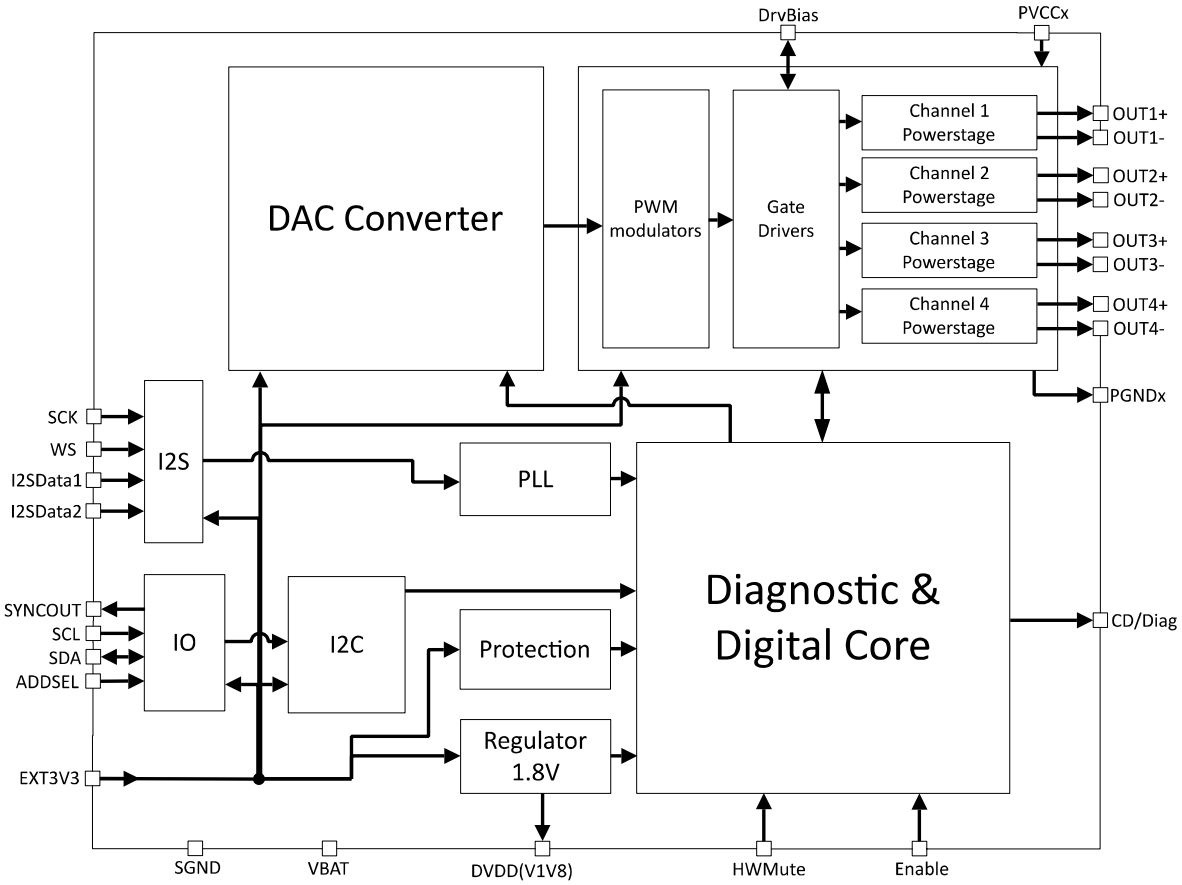



Figure 2. **Pin connection diagram (top view on left, bottom view on right)**

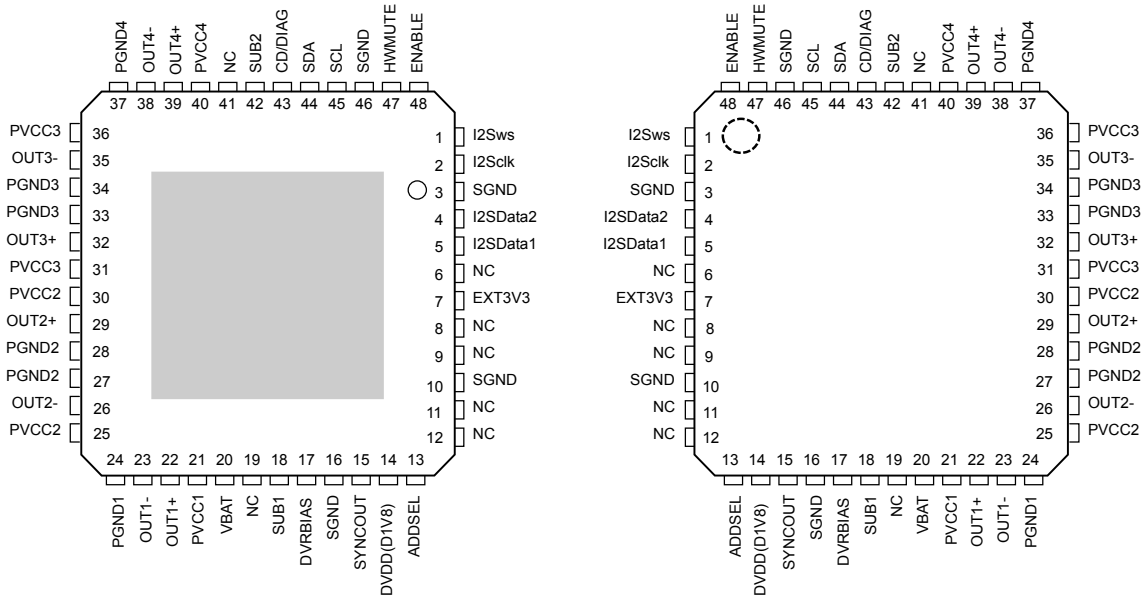


**Table 1. Pins list description**

| # | Pin | Function | Definition | Internal structure |
|---|---|---|---|---|
| 1 | I2Sws | I2S/TDM sync input | Input | |
| 2 | I2Sclk | I2S/TDM clock input | Input | |
| 3 | SGND | Signal ground | Supply | |
| 4 | I2SData2 | I2S/TDM data input 2 | Input | |
| 5 | I2SData1 | I2S/TDM data input 1 | Input | |
| 6 | NC | Not connected | | |
| 7 | EXT3V3 | Auxiliary external 3.3 V supply | Supply | |
| 8 | NC | Not connected | | |
| 9 | NC | Not connected | | |
| 10 | SGND | Signal ground | Supply | |
| 11 | NC | Not connected | | |
| 12 | NC | Not connected | | |
| 13 | ADDSEL | Address selection | Input | |
| 14 | DVDD(D1V8) | Digital power supply | Supply internal reference | |
| 15 | SYNCOUT | Synchronization clock out | Output | Push-pull |
| 16 | SGND | Signal ground | Supply | |
| 17 | DRVBIAS | Gate driver bias | Supply internal reference | |
| 18 | SUB1 | Die substrate pin | Supply | |
| 19 | NC | Not connected | | |
| 20 | VBAT | Battery voltage pin | Supply | |
| 21 | PVCC1 | Channel 1, power supply | Supply | |
| 22 | OUT1+ | Channel 1, half-bridge plus, output | Output | |
| 23 | OUT1- | Channel 1, half-bridge minus, output | Output | |
| 24 | PGND1 | Channel 1, power ground | Supply | |
| 25 | PVCC2 | Channel 2, power supply | Supply | |
| 26 | OUT2- | Channel 2, half-bridge minus, output | Output | |
| 27 | PGND2 | Channel 2, power ground | Supply | |
| 28 | PGND2 | Channel 2, power ground | Supply | |
| 29 | OUT2+ | Channel 2, half-bridge plus, output | Output | |
| 30 | PVCC2 | Channel 2, power supply | Supply | |
| 31 | PVCC3 | Channel 3, power supply | Supply | |
| 32 | OUT3+ | Channel 3, half-bridge plus, output | Output | |
| 33 | PGND3 | Channel 3, power ground | Supply | |
| 34 | PGND3 | Channel 3, power ground | Supply | |
| 35 | OUT3- | Channel 3, half-bridge minus, output | Output | |
| 36 | PVCC3 | Channel 3, power supply | Supply | |
| 37 | PGND4 | Channel 4, power ground | Supply | |
| 38 | OUT4- | Channel 4, half-bridge minus, output | Output | |
| 39 | OUT4+ | Channel 4, half-bridge plus, output | Output | |
| 40 | PVCC4 | Channel 4, power supply | Supply | |

| # | Pin | Function | Definition | Internal structure |
|---|---|---|---|---|
| 41 | NC | Not connected | | |
| 42 | SUB2 | Die substrate pin | Supply | |
| 43 | CD/DIAG | Clipping detector and diagnostic output | Output | Open-drain |
| 44 | SDA | I²C data | Input/Output | Open-drain |
| 45 | SCL | I²C clock | Input | |
| 46 | SGND | Signal ground | Supply | |
| 47 | HWMUTE | Hardware mute | Input | Internal pull-up |
| 48 | ENABLE | Enable | Input | |

## 1.1 Application diagram

**Figure 3. Application diagram**

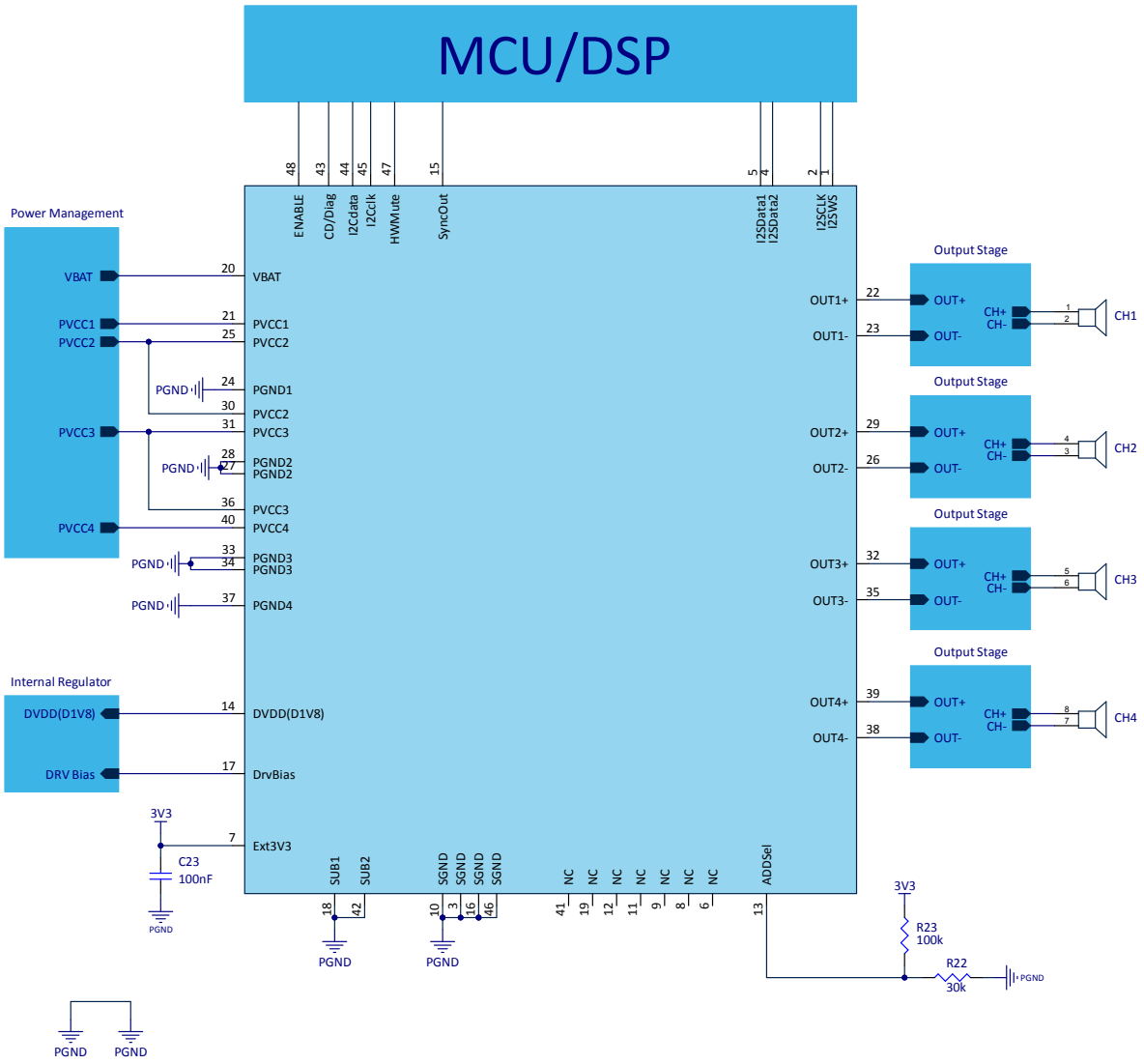
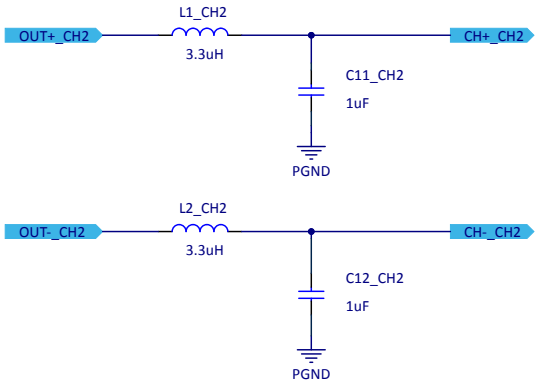


**Figure 4. Output stage**




*Note: The figure above reports the output stage filter of the channel two as reference. The other channels follow the same configuration.*

**Figure 5. Power supply filter**

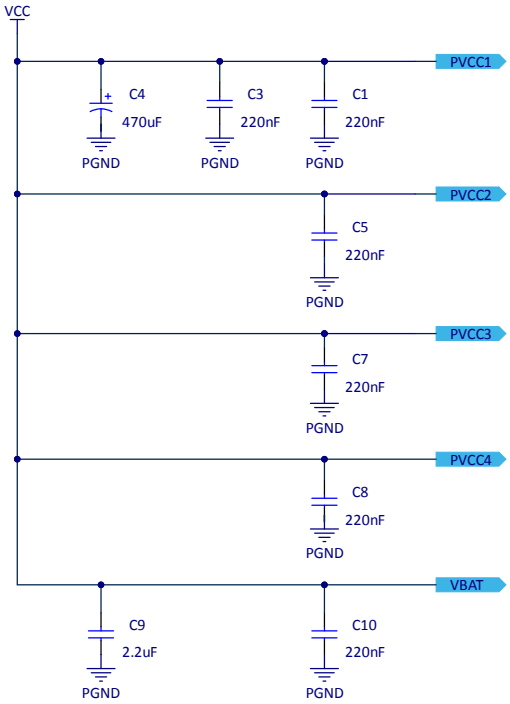



**Figure 6. Internal regulator**

# 2 Electrical specifications

## 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CCmax}$ | DC supply pins [VBAT, PVCC(x)] | -0.3 to 40 | V |
| $OUT_{(x)}{}^{+}$, $OUT_{(x)}{}^{-}$ | Output ± pin | -0.3 to 25 | V |
| DRVBIAS | Gate driver bias pin(1) | -0.3 to 20 | V |
| EXT3V3 | Voltage on EXT3V3 pin | -0.3 to 4.6 | V |
| $I2C_{data}$, $I2C_{clk}$ | I²C bus pins [SDA, SCL] | -0.3 to 4.6 | V |
| $I2S_{data1}$, $I2S_{data2}$, $I2S_{clk}$, $I2S_{ws}$ | I²C bus pins [I2SData1, I2SData2, I2Sclk, I2Sws] | -0.3 to 4.6 | V |
| SYNCOUT | Synchronization pin | -0.3 to 4.6 | V |
| ADDSEL | Address selection pin | -0.3 to 4.6 | V |
| ENABLE | Enable pin | -0.3 to 4.6 | V |
| CD/DIAG | Clipping detector and diagnostic pin | -0.3 to 4.6 | V |
| HWMUTE | Hardware mute pin | -0.3 to 4.6 | V |
| DVDD(D1V8) | Digital power supply pin(1) | -0.3 to 2.5 | V |
| $GND_{max}$ | Voltage difference between ground pins [SGND, $PGND_{(x)}$, $SUB_{(x)}$] | -0.3 to 0.3 | V |
| $T_A$ | Ambient operating temperature | -40 to 125 | °C |
| $T_{stg}$, $T_J$ | Storage and junction temperature | -55 to 150 | °C |
| $ESD_{HBM}$ | ESD protection HBM (2) | 2000 | V |
| $ESD_{CDM}$ | ESD protection CDM standard (2) | 500 | V |
| | ESD protection CDM corner (2) | 750 | V |

1. *Internal circuit output pin: not to be controlled externally.*
2. *Definition according to the international standard.*

## 2.2 Thermal data

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance, junction-to-case (1) | 2.05 | °C/W |

1. *By simulation with top cold plate as per JEDEC best practice guidelines (JESD51) in contact with package top side (e-pad). Ambient temperature set to 85 °C.*

# 3 General description

The HFDA80D is a quad-channel, 24-bit digital input, class-D BTL audio amplifier with advanced diagnostics, high PWM switching frequency and high-resolution audio. The high integration level and the embedded signal processing allow excellent audio performances.

The HFDA80D includes an I²C bus interface to control the operation and read the state of the power amplifier, perform diagnostics and in general access the features reported in the datasheet.

The communication load towards the microcontroller is eased by the presence of a dedicated clipping detector and diagnostics output pin, CD/DIAG, that can trigger the host to read important information as it becomes available. All useful information derived from internal detectors (thermal warnings, output offset, overcurrent protection etc.) can in fact be selectively set to toggle the CD/DIAG pin, according to programmable configuration registers.

The HFDA80D implements a new concept of load diagnostics specifically designed for automotive applications, embedding a highly reliable noise-immune load diagnostic algorithm with self-generated stimuli: this allows to detect anomalous load connections or variations and make this information available through the I²C bus.

## 3.1 Pulse width modulator (PWM)

The HFDA80D channels output a modulated version of the digital inputs, through in-phase pulse-width modulation. Thanks to proprietary technology, this is performed with excellent stability, high bandwidth, low noise, and low distortion. The PWM signal is demodulated by an external LC filter (see LC filter design for more details).

The choice of a high PWM switching frequency allows the use of a small-sized inductor for the demodulator filter, thus contributing to the minimization of PC real estate occupation and cost, and makes the PWM tones lie outside the AM band, thus avoiding by design EMC interference due to the PWM harmonics.

## 3.2 Feedback topology and switching frequency

The device works with a “feedback before the LC filter” output topology. This choice, together with the 2 MHz switching PWM, allows for the usage of smaller and cost-effective components for the demodulator filter. The HFDA80D is ensured with a flat frequency response up to around 40 kHz, but can reach up to 80 kHz of bandwidth by tailoring the demodulator filter for this task.

## 3.3 Load configurations

The HFDA80D supports several load configurations. The default configuration is suitable for a 4-speaker (front/rear–left/right) application. The maximum allowed supply voltage depends on the impedance of the loads:

- 4 x 4 Ω or 8 Ω load driving is supported for $V_{CC}$ up to 18 V.
- 4 x 2 Ω load driving is supported up to 16 V of $V_{CC}$.

## 3.4 Low latency

The HFDA80D offers a very low latency signal processing pipeline: the delay from the input signal to the output PWM is only $T_{latency}$. This makes the HFDA80D eligible for high-speed audio processing applications like noise canceling.

# 4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 LQFP48L (7x7x1.4 mm exp. pad up) package information

**Figure 7. LQFP48L (7x7x1.4 mm exp. pad up) package outline**

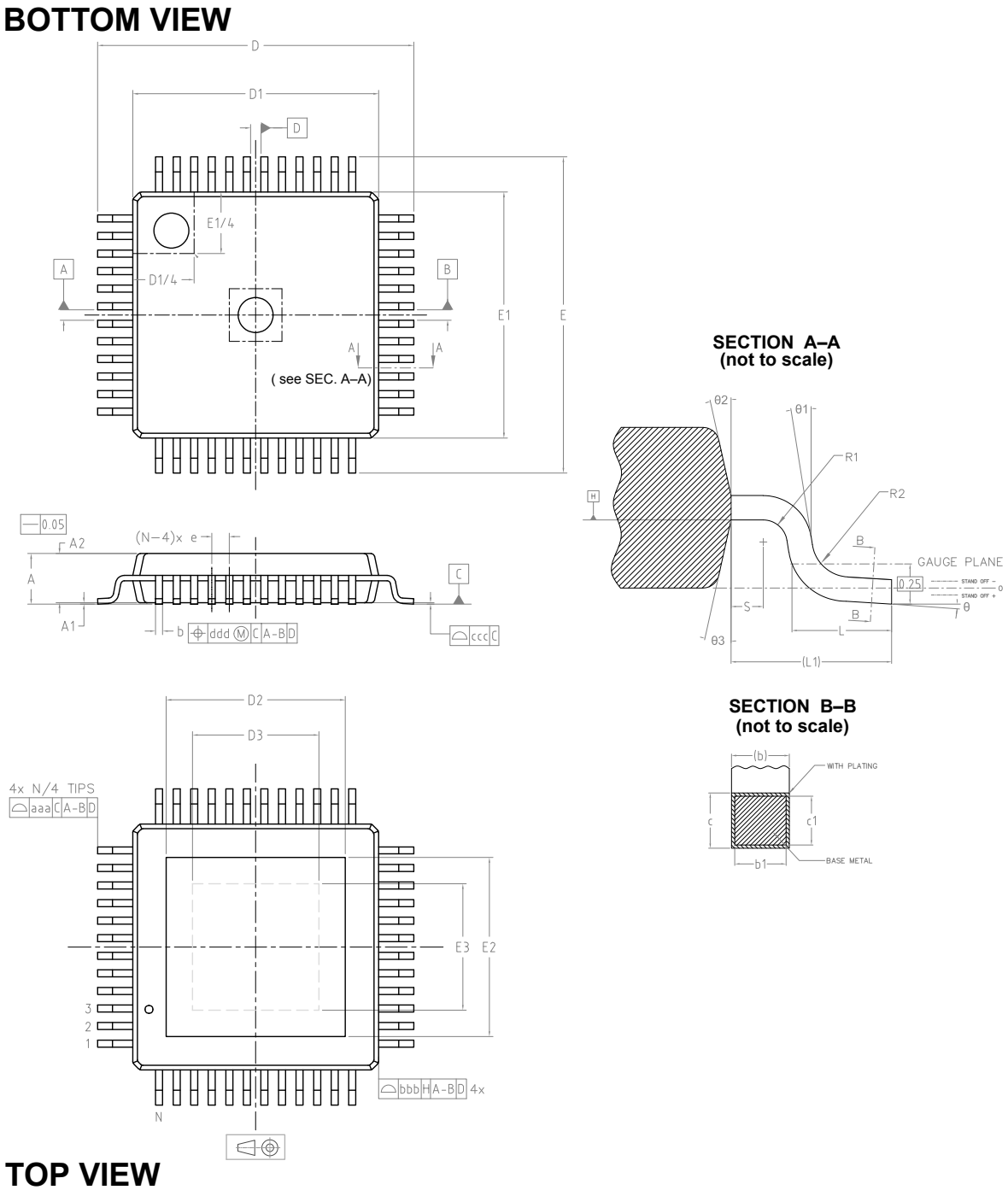


Table 4. **LQFP48L (7x7x1.4 mm exp. pad up) package mechanical data**

| Symbol | Dimensions in mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| Θ | 0° | 3.5° | 7° |
| Θ1 | 0° | | |
| Θ2 | 10° | 12° | 14° |
| Θ3 | 10° | 12° | 14° |
| A | | | 1.49 |
| A1 | -0.03 | | 0.05 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.09 | | 0.20 |
| c1 | 0.09 | | 0.16 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| D2 | | | 5.60 |
| D3 | 3.90 | | |
| e | 0.50 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| E2 | | | 5.60 |
| E3 | 3.90 | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| N | 48 | | |
| R1 | 0.08 | | |
| R2 | 0.08 | | 0.20 |
| S | 0.20 | | |
| Tolerance of form and position | | | |
| aaa | 0.20 | | |
| bbb | 0.20 | | |
| ccc | 0.08 | | |
| ddd | 0.08 | | |

## Revision history

Table 5. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 17-Jan-2025 | 1 | Initial release. |
| 05-Mar-2025 | 2 | Updated Features. |

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