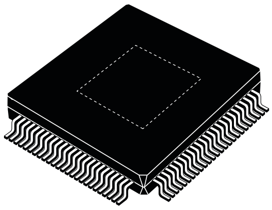
L99DZ380

Datasheet

Automotive high end front door module with 2 LIN and CAN FD



LQFP100 14x14 mm (exposed pad down)

Product summary	
Order code	**L99DZ380TR**
Package	LQFP100 14x14 mm (exposed pad down)
Packing	Tape and reel

Features

Channel	R_{ON}	I_{LIMH}
2 half bridge	100 mΩ	7.5 A
1 half bridge	150 mΩ	6 A
2 half bridges	1600 mΩ	0.5 A
3 half bridges	300 mΩ	3 A
1 configurable high-side driver	300 mΩ	1.5 A
	1600 mΩ	0.35 A
2 high-side drivers	1.4 Ω	0.5 A
1 high-side driver to supply EC Glass MOSFET	1.4 Ω	0.5 A
10 high-side drivers	7 Ω	0.15 A

- AEC-Q100 qualified
- CAN FD transceiver supporting communication up to 5 Mbit/s (ISO 11898-2/2016 and SAE J2284 compliant) with local failure and bus failure diagnosis
- 2 LIN transceivers ISO 17987-4/2016 compliant
- Advanced lock and fold closing by means of PWM control on HB1-HB6, HB4-HB5, HB20 and HB21
- Advanced short-circuit detection on all the half bridges
- All HS drivers with constant current mode at start-up to drive capacitive loads
- Internal 10-bit PWM timer for each stand-alone high-side driver
- Buffered supply for voltage regulators and 2 high-side drivers (HS15 and HS0/ both P-channel) to supply, for example, external contacts
- Programmable overcurrent recovery function, to drive loads with higher inrush currents as current limitation value (for HB1-HB6, HS7-HS10)
- Flexible HS drivers (HS7-HS19 and HS0), suitable to drive external LED modules with high input capacitance value
- Programmable periodic system wake-up feature
- Complete 9-channel contact monitoring interface, with programmable cyclic sense functionality, one of them also with DIR functionality
- Dedicated debug input pin
- Configurable window watchdog
- STM standard serial peripheral interface (32-bit/ST-SPI 4.0)
- Programmable reset generator for power-on and undervoltage
- Ultra low quiescent current in standby modes
- No electrolytic capacitor required on regulator outputs
- Two 5 V voltage regulators for microcontroller and peripheral supply
- Central two-stage charge pump
- Control block for electrochromic element
- Driver for external MOSFET in high-side configuration with SC protection/ diagnosis and open-load diagnosis
- Motor bridge driver for 4 external MOSFETs, in H-bridge configuration with short-circuit protection/diagnosis and open-load diagnosis

- Diagnostic functions
- Current monitor output for all internal high-side drivers
- Digital thermal clusters
- Device contains temperature warning and protection
- Open-load diagnosis for all the outputs
- Overcurrent protection for all the outputs

Description

The L99DZ380 is a door zone system IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as CAN FD and 2 identical LIN physical communication layers. The device has two low drop voltage regulators to supply the system microcontroller and external peripheral loads such as sensors and provides enhanced system standby functionality with programmable local and remote wake-up capability. Moreover, the 14 high-side drivers (13 to supply LEDs and 1 to supply bulbs) increase the system integration level; all the high-side drivers support the constant current mode for LED module with high input capacitance. Up to 7 DC motors and 4 external MOS transistors in H-bridge configuration can be driven in PWM mode up to 25 kHz. An additional gate drive can control an external MOSFET in high-side configuration to supply a resistive load connected to GND (for example mirror heater). An electrochromic mirror glass can be controlled using the integrated SPI-driven module in conjunction with an external MOS transistor. All the outputs are SC protected and implement an open-load diagnosis. The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

1 Block diagram and pin description

Figure 1. Block diagram

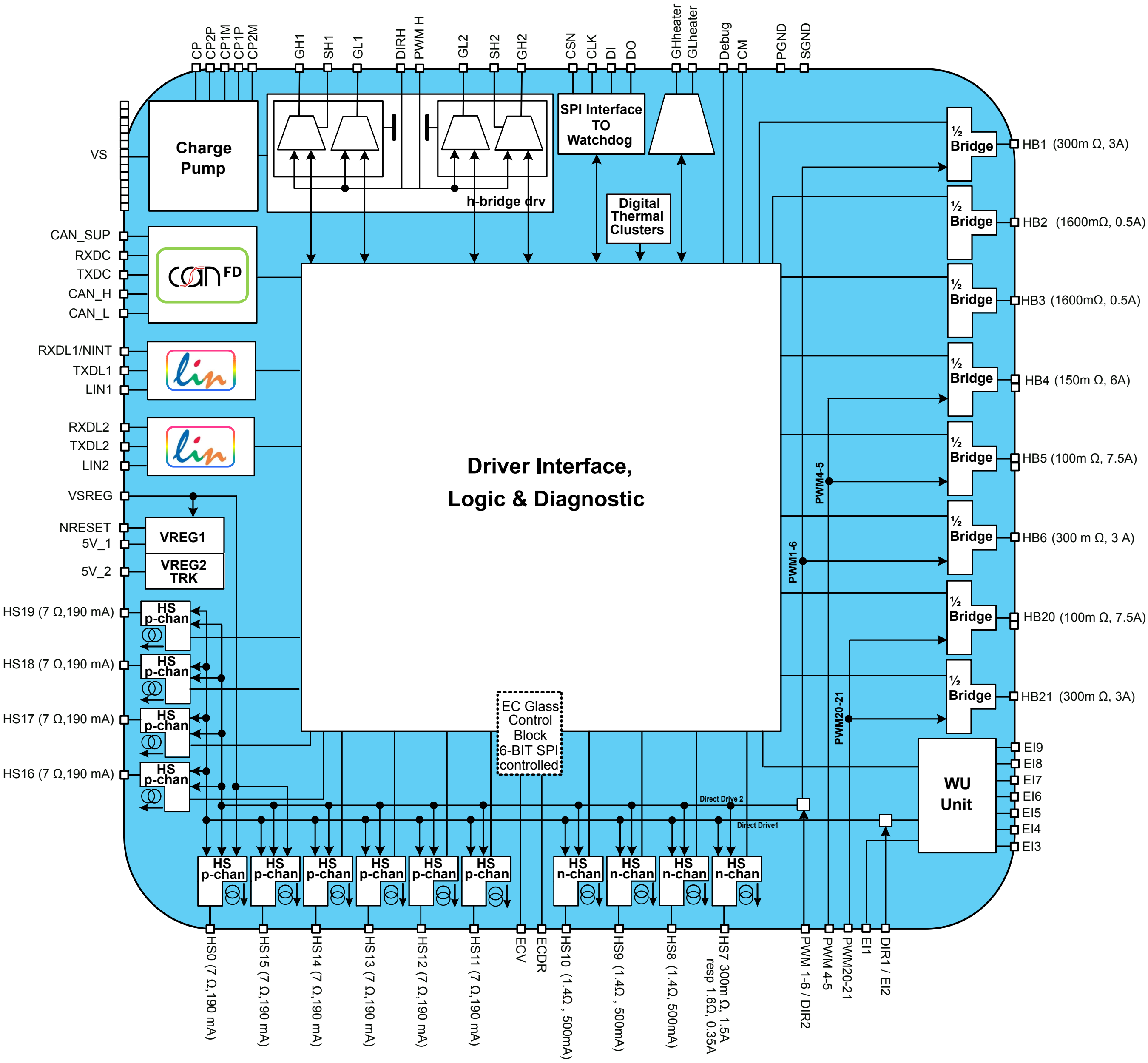


Figure 2. Pin connection (top view)

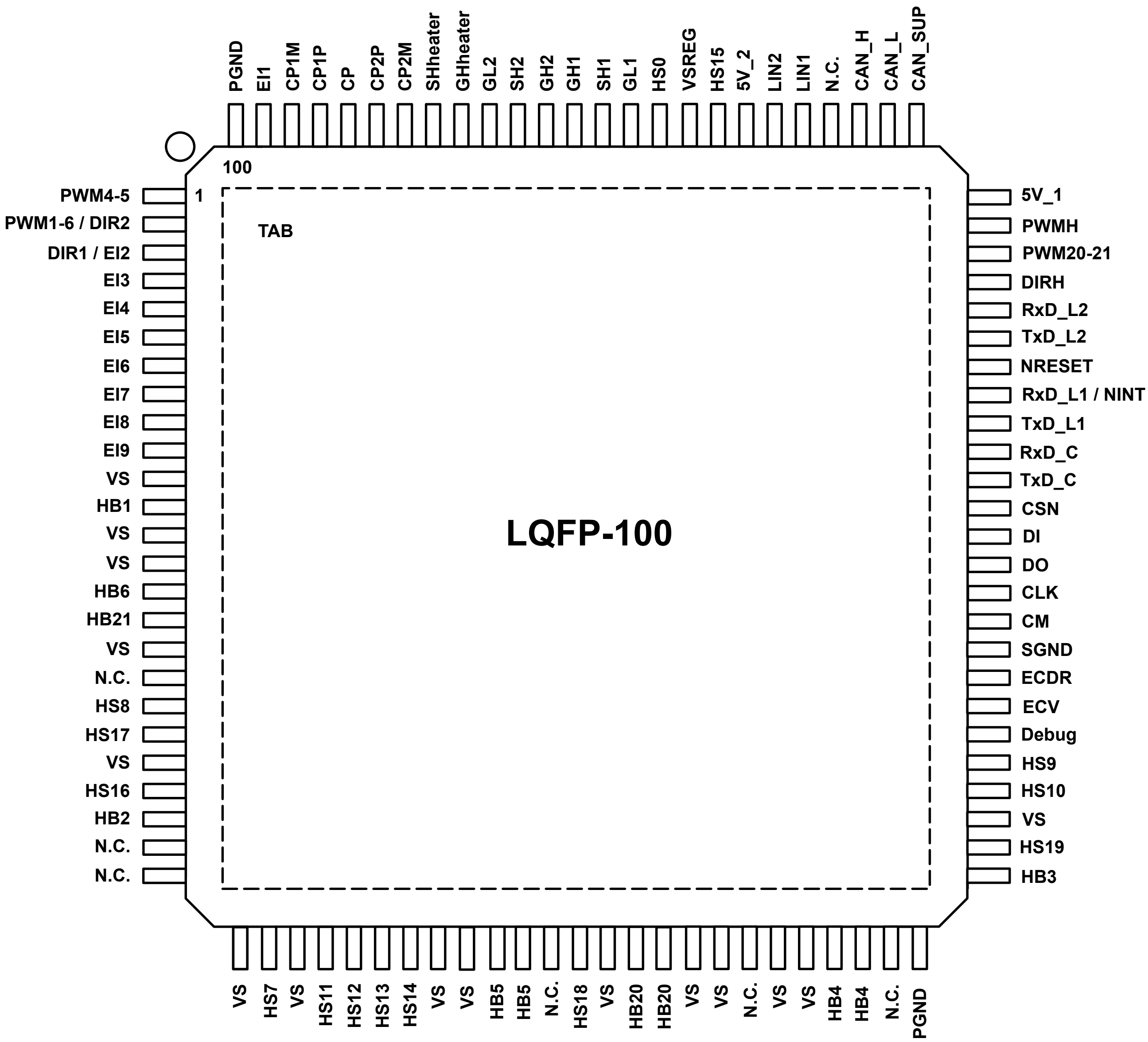


Table 1. Pin function

Pin	Name	Function
1	PWM4-5	PWM input: this input signal can be used to control the HB4 or HB5
2	PWM1-6/DIR2	PWM1-6 input: this input signal can be used to control the HB1 or HB6; DIR2: direct HS drive 2;
3	DIR1/EI2	DIR1: direct HS drive 1; EI2: input pin for static or cyclic monitoring of external contacts
4	EI3	Input pin for static or cyclic monitoring of external contacts
5	EI4	Input pin for static or cyclic monitoring of external contacts
6	EI5	Input pin for static or cyclic monitoring of external contacts

Pin	Name	Function
7	EI6	Input pin for static or cyclic monitoring of external contacts
8	EI7	Input pin for static or cyclic monitoring of external contacts
9	EI8	Input pin for static or cyclic monitoring of external contacts
10	EI9	Input pin for static or cyclic monitoring of external contacts
11	VS	Power supply voltage for power stage outputs (external reverse battery protection required), for this input a ceramic capacitor as close as possible to GND is recommended. Important: For the capability of driving the full current at the outputs, all pins of VS must be connected externally!
12	HB1	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
13	VS; 2nd pin	Current capability (pin description see above)
14	VS; 3rd pin	Current capability (pin description see above)
15	HB6	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
16	HB21	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
17	VS; 4th pin	Current capability (pin description see above)
18	NC	Not connected
19	HS8	High-side driver output to drive LEDs. The channel is protected by auto-recovery feature.
20	HS17	High-side driver output to drive LEDs
21	VS; 5th pin	Current capability (pin description see above)
22	HS16	High-side driver output to drive LEDs
23	HB2	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
24	NC	Not connected
25	NC	Not connected
26	VS; 6th pin	Current capability (pin description see above)
27	HS7	High-side driver output to drive LEDs or a 10 W bulb (programmable Rdson). The channel is protected by auto-recovery feature.
28	VS; 7th pin	Current capability (pin description see above)
29	HS11	High-side driver output to drive LEDs
30	HS12	High-side driver output to drive LEDs
31	HS13	High-side driver output to drive LEDs
32	HS14	High-side driver output to drive LEDs
33	VS; 8th pin	Current capability (pin description see above)
34	VS; 9th pin	Current capability (pin description see above)
35	HB5	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to Vs, low-side driver from GND to output). The channel is protected by auto-recovery feature.

Pin	Name	Function
36	HB5; 2nd pin	Current capability (pin description see above)
37	NC	Not connected
38	HS18	High-side driver output to drive LEDs.
39	VS; 10th pin	Current capability (pin description see above)
40	HB20	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
41	HB20; 2nd pin	Current capability (pin description see above)
42	VS; 11th pin	Current capability (pin description see above)
43	VS; 12th pin	Current capability (pin description see above)
44	NC	Not connected
45	VS; 13th pin	Current capability (pin description see above)
46	VS; 14th pin	Current capability (pin description see above)
47	HB4	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
48	HB4; 2nd pin	Current capability (pin description see above)
49	NC	Not connected
50	PGND	Power ground
51	HB3	Half-bridge outputs: the output is built by a high-side and a low-side switch which are internally connected. The output stage of both switches is a power DMOS transistor. Each driver has an internal parasitic reverse diode (bulk-drain-diode: high-side driver from output to VS, low-side driver from GND to output). The channel is protected by auto-recovery feature.
52	HS19	High-side driver output to drive LEDs.
53	VS; 15th pin	Current capability (pin description see above)
54	HS10	High-side driver-output; Important: Beside the HS10-HS on/off bit this output can be switched on setting the ECON bit for electro-chrome control mode with higher priority. The channel is protected by auto-recovery feature.
55	HS9	High-side driver output to drive LEDs. The channel is protected by auto-recovery feature.
56	Debug	Debug input to deactivate the window watchdog (high active). Voltage capability linked to Vs.
57	ECV	ECV: using the device in EC control mode this pin is used as voltage monitor input. For fast discharge an additional low-side switch is implemented
58	ECDR	ECDR: using the device in EC control mode this pin is used to control the gate of an external N-channel Power MOSFET
59	SGND	Signal ground
60	CM	Current monitor output: depending on the selected multiplexer bits of the Control register this output sources an image of the instant current through the corresponding high-side driver with a fixed ratio
61	CLK	SPI: serial clock input
62	DO	SPI: serial data output (push pull output stage)
63	DI	SPI: serial data input
64	CSN	SPI: chip select not input
65	TXDC	CAN transmit data input
66	RXDC	CAN receive data output (push pull output stages)
67	TXDL1	LIN1 transmit data input

Pin	Name	Function
68	RXDL1/NINT	RXDL: LIN1 receive data output; NINT: indicates local/remote wake-up events
69	NRESET	Power GND NReset output to micro controller; internal pull-up of typical 110 kΩ (reset state = LOW)(open drain output stage)
70	TXDL2	LIN2 transmit data input
71	RXDL2	RXDL2: LIN2 receive data output
72	DIRH	Direction Input: this input controls the H-bridge drivers for the external Power MOSFETs
73	PWM20-21	PWM input: this input signal can be used to control the HB20 or HB21
74	PWMH	PWMH input: this input signal can be used to control the H-bridge gate driver
75	5V_1	Voltage regulator output: 5 V supply for example micro controller, CAN transceiver
76	CAN supply	CAN supply input; to allow external CAN supply from V1
77	CAN_L	CAN low level voltage I/O
78	CAN_H	CAN high level voltage I/O
79	NC	Not connected
80	LIN1	LIN bus line 1
81	LIN2	LIN bus line 2
82	5V_2	Voltage tracker output: 5 V supply for external loads (potentiometer, sensors). V2 is protected against reverse supply
83	HS15	High-side driver output to drive LEDs
84	VSREG	Power supply voltage to supply the internal voltage regulators and the HS0 (external reverse battery protection required / Diode) for this input a ceramic capacitor as close as possible to GND and an electrolytic back up capacitor is recommended.
85	HS0	High-side driver output to drive LEDs or to supply contacts
86	GL1	Gate driver for Power MOSFET low-side switch in half-bridge 1
87	SH1	Source of high-side switch in half-bridge 1
88	GH1	Gate driver for Power MOSFET high-side switch in half-bridge 1
89	GH2	Gate driver for Power MOSFET high-side switch in half-bridge 2
90	SH2	Source of high-side switch in half-bridge 2
91	GL2	Gate driver for Power MOSFET low-side switch in half-bridge 2
92	GHheater	Gate driver for external N-channel Power MOSFET in high-side configuration to control the heater
93	SHheater	Source of high-side Power MOSFET to control the heater
94	CP2M	Charge pump pin for capacitor 2, negative side
95	CP2P	Charge pump pin for capacitor 2, positive side
96	CP	Charge pump output
97	CP1P	Charge pump pin for capacitor 1, positive side
98	CP1M	Charge pump pin for capacitor 1, negative side
99	EI1	Input pin for static or cyclic monitoring of external contacts
100	PGND	Power GND
-	TAB	Ground connection

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_S, V_{Sreg}	DC supply voltage/jump start		-0.3		28	V
V_S, V_{Sreg}	DC supply voltage/load dump		-0.3		40	
5V1	Stabilized supply voltage, logic supply	V1 < V_{SREG}	-0.3		6.5	V
5V2	Stabilized supply voltage (1)		-0.3		28	V
V_{DI}, V_{CLK}, V_{CSN}, V_{DO}, $V_{RXDL/NINT}$, V_{RXDC}, V_{NRESET}, V_{CM}, V_{PWMH}, V_{DIRH}, V_{PWM1-6}, V_{PWM4-5}, V_{PW20}, V_{PWM21}	Logic input/output voltage range		-0.3		V1+0.3	V
V_{TXDC}, V_{TXDL}	Logic input/output voltage range		-0.3		V1+0.3	V
V_{Debug}	Debug input pin voltage range		-0.3		V_S+0.3	V
$V_{EI1,3,..9}$	DC external input voltage/"jump start"		-0.3		28	V
$V_{DIR1/EI2}$	DC external input voltage/"jump start"		-0.3		28	V
V_{LIN}	LIN bus I/O voltage range		-27		40	V
I_{Input}	Current injection into V_S related input pins			20		mA
I_{out_inj}	Current injection into V_S related outputs			20		mA
V_{CANSUP}	CAN supply		-0.3		5.25	V
V_{CANH}, V_{CANL}	CAN bus I/O voltage range		-27		40	V
V_{CANH} - V_{CANL}	Differential CAN-bus voltage		-5		10	V
V_{HBn}, V_{HSm}, V_{ECDR}, V_{ECV}, V_{HS0}	Output voltage: • for HB (n = 1 to 6, 20, 21) • for HS (m = 7 to 19)		-0.3		V_S+0.3	V
V_{GH1}, V_{GH2}, (V_{Gxy})	High voltage signal pins	V_{CP}+0.3	V_{Sxy}-0.3		V_{Sxy}+13	V
V_{GL1}, V_{GL2}	High voltage signal pins	V_{CP}+0.3	-0.3		12	V
V_{SH1}, V_{SH2} (V_{Sxy})	High voltage signal pins		-1		40	V
	High voltage signal pins; single pulse with $t_{max.}$ = 200 ns		-5		40	V
V_{CP1P}	High voltage signal pins		V_S-0.3		V_S+10	V
V_{CP2P}	High voltage signal pins		V_S-0.6		V_S+10	V
V_{CP1M}, V_{CP2M}	High voltage signal pins		-0.3		V_S+0.3	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CP}	High voltage signal pin — $V_S \le 26$ V		V_S-0.3		V_S+14	V
	High voltage signal pin — $V_S > 26$ V		V_S-0.3		40	V
V_{GH_heater}		V_{CP}+0.3	$V_{Sheater}$-0.3		$V_{Sheater}$+13	V
V_{SH_heater}			-0.3		40	V
$I_{ECV, HB2, HB3, HS9, HS10, HS11, HS12, HS13, HS14, HS15, HS16, HS17, HS18, HS19, HS0}$	Output current (2)		-1.25		1.25	A
I_{HS8}	Output current(2)		-2.5		2.5	A
I_{HS7}	Output current(2)		-5		5	A
$I_{HB1,6,21}$	Output current(2)		-5		5	A
$I_{HB4,5,20}$	Output current(2)		-10		10	A
I_{VScum}	Maximum cumulated current at V_S drawn by HB1 & HB2(2)		-7.5		7.5	A
	Maximum cumulated current at V_S drawn by HB3, HS8 & HS10(2)		-2.5		2.5	
	Maximum cumulated current at V_S drawn by HB4(2)		-10		10	
	Maximum cumulated current at V_S drawn by HB5(2)		-10		10	
	Maximum cumulated current at V_S drawn by HB6 & HS7(2)		-7.5		7.5	
	Maximum cumulated current at V_S drawn by HS9, HS11, HS12, HS13, HS14, HS15 and CP		-2.5		2.5	
I_{VSREG}	Maximum current at V_{SREG} pin(2) (5V_1. 5V_2 and HS0)		-2.5		2.5	A
$I_{PGNDcum}$	Maximum cumulated current at PGND drawn by HB1 & HB6(2)		-7.5		7.5	A
	Maximum cumulated current at PGND drawn by HB2 & HB5(2)		-12.5		12.5	
	Maximum cumulated current at PGND drawn by HB3, HB4 & ECV(2)		-12.5		12.5	
I_{SGND}	Maximum current at SGND(2)		-1.25		1.25	A
GND pins	PGND vs SGND		-0.3		0.3	V

1. *L99DZ380 is protected against 5V2 shorted to V_S and 5V2 reverse biasing when V_{SREG} is higher than 3.5 V.*
2. *Values for the absolute maximum DC current through the bond wires. This value does not consider maximum power dissipation or other limits.*

Note:

1. *All maximum ratings are absolute ratings. Leaving the limitation of any of these values may cause an irreversible damage of the integrated circuit.*
2. *Loss of ground or ground shift with externally grounded loads: ESD structures are configured for nominal currents only. If external loads are connected to different grounds, the current load must be limited to this nominal current.*

2.2 ESD protection

Table 3. ESD protection

Parameter	Value	Unit
All pins[1]	±2	kV
All power output pins[2] : HB1–HB6, HB20, HB21, HS7 - HS19, HS0, ECV	±4	kV
LIN	±8[2]	kV
	±8[3]	
	±6[4]	
CAN_H, CAN_L	±8[2]	kV
	±6[4]	
All pins[5]	±500	V
Corner pins[5]	±750	V

1. *HBM (human body model, 100 pF, 1.5 kΩ) according to AEC-Q100-002.*
2. *HBM with all none zapped pins grounded. HBx (x = 1, …, 6, 20, 21) and HSy (y = 7, ..., 15, 0, 16, …, 19).*
3. *Indirect ESD Test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware requirements for LIN, CAN and flexray interfaces in automotive applications' (version 1.3, May 2012).*
4. *Direct ESD test according to IEC 61000-4-2 (150 pF, 330 Ω) and 'Hardware Requirements for LIN, CAN and Flexray interfaces in automotive applications' (version 1.3, May 2012).*
5. *Charged device model according to AEC-Q100-011.*

2.3 Thermal data

Table 4. Operation junction temperature

Symbol	Parameter	Typ. value	Unit
T_J	Operating junction temperature	-40 to 175	°C

All parameters are guaranteed in the temperature range -40 to 150°C (unless otherwise specified); the device is still operative and functional at higher temperatures (up to 175°C).

Note:
1. *Parameters limits at higher temperatures than 150°C may change with respect to what is specified as per the standard temperature range.*
2. *Device functionality at high temperature is guaranteed by characterization.*

Table 5. Temperature warning and thermal shutdown

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
T_W	Thermal overtemperature warning threshold	T_J[1]	140	150	160	°C	F.025
T_{SD1}	Thermal shutdown junction temperature 1	T_J[1]	165	175	185	°C	F.026
T_{SD2}	Thermal shutdown junction temperature 2	T_J[1]	175	185	195	°C	F.028
$T_{SD12hys}$		Hysteresis		5		°C	F.029
t_{fTjTW}	Thermal warning/shutdown filter time	Tested by scan		32		µs	F.030

1. *Non overlapping.*

2.3.1 L99DZ380 thermal profiles

Profile 1

Battery voltage: 16 V, ambient temperature start: 85 °C.

DC activation:

- V1 charged with 70 mA (68 Ω - DC activation)
- V2 charged with 30 mA (120 Ω - DC activation)
- HS7: 1 x 10 W bulb (DC activation)
- HS11: 300 Ω resistor (DC activation)
- HS12: 300 Ω resistor (DC activation)
- HS13: 300 Ω resistor (DC activation)
- HS14: 300 Ω resistor (DC activation)

Cyclic activation:

- **HB4–HB5**: 3.3 Ω resistor placed across those outputs
  – 10 activations of lock/unlock (250 ms ON lock; 500 ms wait; 250 ms ON unlock; 500 ms wait).
- **HB5–HB6**: 10 Ω resistor placed across those outputs
  – 10 activations of safe lock/unlock (250 ms ON lock; 500 ms wait; 250 ms ON unlock; 500 ms wait).

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic activation” sequence is applied.

The device operates always without triggering the thermal warning threshold.

Profile 2

Battery voltage: 16 V, ambient temperature start: 85 °C.

DC activation:

- V1 charged with 70 mA (68 Ω - DC activation)
- V2 charged with 30 mA (120 Ω - DC activation)
- HS7: 1 x 10 W bulb (DC activation)
- HS11: 300 Ω resistor (DC activation)
- HS12: 300 Ω resistor (DC activation)
- HS13: 300 Ω resistor (DC activation)
- HS14: 300 Ω resistor (DC activation)
- HS16: 300 Ω resistor (DC activation)
- HS17: 300 Ω resistor (DC activation)
- HS18: 300 Ω resistor (DC activation)
- HS19: 300 Ω resistor (DC activation)

Cyclic activation:

- **HB1–HB6**: 10 Ω resistor placed across those outputs
  – 2 activations of fold/unfold. (3 s fold; 1 s wait; 3 s unfold; 1 s wait)
- **HB20–HB5**: 10 Ω resistor placed across those outputs
  – 2 activations of soft door in/out. (1 s ON; 3 s wait; 1 s ON; 3 s wait)

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic activation” sequence is applied.

The device operates always without triggering the thermal warning threshold.

Profile 3

Battery voltage: 16 V, ambient temperature start: 85°C.

DC activation:

- V1 charged with 70 mA (68 Ω - DC activation)
- V2 charged with 30 mA (120 Ω - DC activation)
- HS7: 1 x10 W bulb (DC activation)
- HS8: 100 Ω resistor (DC activation)
- HS11: 300 Ω resistor (DC activation)
- HS12: 300 Ω resistor (DC activation)
- HS13: 300 Ω resistor (DC activation)
- HS14: 300 Ω resistor (DC activation)

Cyclic activation:

- **HB5–HB21**: 10 Ω resistor placed across those outputs
  - 5 activations of door handle in/out. (1 s ON; 5 s wait; 1 s OFF; 5 s wait)
  - T_{ON} PWM: 20 kHz

Test execution:

Once thermal equilibrium is reached with all DC load active, the “Cyclic activation” sequence is applied. The device operates always without triggering the thermal warning threshold.

2.4 Electrical characteristics

For an efficient and easy tracking, numbering has been added to each electrical parameter.

Device features are split into categories (see Table 3. ESD protection, Table 4. Operation junction temperature and Table 5. Temperature warning and thermal shutdown) and each of them is represented by a letter (such as A, B, C); all parameters are completely identified by a letter and a three-digit number (for example B.125, C.096) for their whole lifetime.

New inserted parameters continue with the numbering of the related category, no matter of where they are placed.

To facilitate insertion, the last number inserted for each category is also reported in the second column of the table.

Table 6. Electrical parameters numbering

Category	Parameters numbering	Last Inserted
Analog I/O	A.xxx	A.195
Digital I/O	B.xxx	B.034
Voltage regulators	C.xxx	C.057
Outputs	D.xxx	D.137
Transceivers	E.xxx	E.124
Others	F.xxx	F.030

Due to these rules and taking into account that deleted parameter numbers are no more reassigned, numbering inside each category may not be sequential.

Note: For all the parameters described as "Tested by scan", the related timings are specified by design and have been measured in lab.

2.4.1 Supply, supply monitoring and current consumption

All SPI communication, logic and oscillator parameters are working down to V_{SREG} = 3.5 V and parameters are as specified in the respective chapters.

- SPI thresholds
- Oscillator frequency (delay times correctly elapsed)
- Internal register status correctly kept (reset at default values for V_S< V_{POR})
- Reset threshold correctly detected

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.

6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40°C to 150°C, unless otherwise specified.

Table 7. Supply monitoring and current consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{SUV}	V_S undervoltage threshold	V_S increasing / decreasing	4.7		5.4	V	A.001
V_{hyst_UV}	V_S undervoltage hysteresis		0.025	0.1	0.2	V	A.002
V_{SOV}	V_S overvoltage threshold	V_S increasing	19		22.5	V	A.003
V_{SOV}	V_S overvoltage threshold	V_S decreasing	18.5		22.5	V	A.004
V_{hyst_OV}	V_S overvoltage hysteresis		0.5	1.3	1.7	V	A.005
V_{SREGUV}	V_{SREG} undervoltage threshold	V_{SREG} increasing/decreasing	4.2		4.9	V	A.006
V_{hyst_UV}	V_{SREG} undervoltage hysteresis		0.025	0.1	0.2	V	A.007
V_{SREGOV}	V_{SREG} overvoltage threshold	V_{SREG} increasing	19		22.5	V	A.008
V_{SREGOV}	V_{SREG} overvoltage threshold	V_{SREG} decreasing	18.5		22.5	V	A.009
V_{hyst_OV}	V_{SREG} overvoltage hysteresis		0.5	1.3	1.7	V	A.010
t_{ovuv_filt}	V_S/ V_{SREG} overvoltage/ undervoltage filter time	Tested by scan		64		µs	A.011
$I_{V(act)}$	Current consumption in active mode	V_S =12 V, TXD CAN = high, TXD LIN = high, V1 = on, V2 = on, HS/LS driver OFF		6.2	12	mA	A.012
$I_{V(BAT)}$	Current consumption in VBAT_Standby mode (1)	V_S = 12 V, T_J = 85°C, HS/LS driver OFF, CAN WU disabled	8	20	35	µA	A.013
$I_{V(BAT)CS}$	Current consumption in VBAT_Standby mode with cyclic sense enabled(1)	V_S = 12 V, T_J = 85°C, HS/LS driver OFF, CAN WU disabled, T = 50 ms, t_{on} = 100 µs	40	75	125	µA	A.014
$I_{V(BAT)CW}$	Current consumption in VBAT_Standby mode with cyclic wake enabled(1)	V_S = 12 V, T_J = 85 °C, HS/LS driver OFF, CAN WU disabled, T = 50 ms, t_{on} = 100 µs, In standby phase before waking up on timer expiration	40	75	125	µA	A.015
$I_{V(V1stby)\_0}$	Current consumption in V1_Standby mode(1)	V_S = 12 V, T_J = 85°C, voltage regulator V1 active, (Iv1 = 0), HS/LS driver OFF, Voltage regulator V2 deactivated,	16	51	76	µA	A.016

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
		CAN WU disabled					
$I_{V(V1stby)}$	Current consumption in V1_Standby mode(1)	V_S = 12 V, T_J = 85°C, voltage regulator V1 active, (I_{V1}<I_{cmp}), HS/LS driver OFF		60	146	µA	A.017
I_{qEIx}(2)	Additional quiescent current for each EIx active (x = 1, …, 9)			200		nA	A.018
I_{qCAN_WU}(2)	Additional quiescent current with CAN wake-up enabled (CAN_WU_EN = 1)			10		µA	A.019
$I_{HS0\_HS15\_DIR}$(2)	Quiescent current adder if HS0 or HS15 is configured for direct drive; value during output OFF				5	µA	A.021

1. *Conditions for specified current consumption:*
   - *V_{LIN} > (V_S -1.5 V)*
   - *(CAN_H - CAN_L) < 0.4 V or (CAN_H - CAN_L) > 1.2 V*
   - *V_{WU} < 1 V or V_{WU} > (V_S - 1.5 V)*
   - *LIN wake-up is possible*
2. *Parameter specified by design, not tested in production.*

2.4.2 Oscillator

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.

6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 8. Oscillator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
F_{CLK1}(1)	Oscillation frequency	-	0.80	1.0	1.20	MHz	A.023
F_{CLK2}(1)	Oscillation frequency	-	12.8	16.0	19.2	MHz	A.024

1. *1 MHz clock is used in standby mode for low quiescent requirements; 16 MHz clock is used in active mode.*

2.4.3 Power-on Reset (V_{SREG})

All outputs open; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 9. Power-on Reset

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{POR_R}	V_{POR} threshold rising	V_{SREG} rising		3.45	4.5	V	A.025
V_{POR_F}	V_{POR} threshold falling	V_{SREG} falling(1)	2.3		3.55	V	A.026

1. *This threshold is valid if V_{SREG} has already reached $V_{POR\_R(max)}$ previously.*

2.4.4 Voltage regulator V1

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
$4.5 < V_S < 28$ V, 4.5 V $< V_{SREG} < 28$ V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 10. **Voltage regulator 1**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V1	Output voltage	$V_{SREG} \geq 5.6$ V		5.0		V	C.001
$V1_{10mA}$	Output voltage tolerance (0 ... I_{cmp})	I_{LOAD} = 100 µA to I_{cmp}, V_{SREG} = 13.5 V	-3		3	%	C.003
$V1_{high\_acc}$	Output voltage tolerance high accuracy mode	$I_{LOAD} = I_{cmp}$ to 100 mA, active mode, V_{SREG} = 13.5 V	-2		2	%	C.004
$V1_{250mA}$	Output voltage tolerance (100 … 250 mA)	I_{LOAD} = 250 mA, V_{SREG} = 13.5 V	-3		3	%	C.005
V_{DP1}	Drop-out voltage	I_{LOAD} = 50 mA		0.2	0.4	V	C.006
		I_{LOAD} = 100 mA		0.3	0.5		C.007
		I_{LOAD} = 150 mA		0.45	0.65		C.008
I_{CC1}	Output current in active mode (to GND)	Maximum continuous load current			250	mA	C.009
I_{CCmax1}	Short-circuit output current (to GND)	Current limitation	340	600	900	mA	C.010
C_{load1} (1)	Load capacitor 1	Ceramic (±20%)	1 (2)	2.2	10	µF	C.011
t_{TSD}	V1 deactivation time after thermal shutdown	Tested by scan		1.5		s	C.012
I_{CMP_ris} (3)	Current comp. rising threshold (to GND)	Rising current	6	12	21	mA	C.013
I_{CMP_fal} (3)	Current comp. falling threshold (to GND)	Falling current	5	10	18	mA	C.014
I_{CMP_hys} (3)	Current comp. hysteresis			2		mA	C.015
$V1_{fail}$	V1 fail threshold	V1 forced		2		V	C.019
t_{V1fail}	V1 fail filter time	Tested by scan	6	13	20	µs	C.020
$t_{V1short}$	V1 short filter time	Tested by scan	2	4	5	ms	C.021
t_{V1FS}	V1 fail-safe filter time	Tested by scan	1.43	2	2.06	ms	C.022
t_{V1off}	V1 deactivation time after 8 consecutive WD failures	Tested by scan		200	270	ms	C.023

1. *Specified by design, not tested in production.*
2. *Nominal capacitor value required for stability of the regulator. Tested with 1 µF ceramic (±20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor value is recommended to minimize the DPI stress in the application.*
3. *In active mode, V1 regulator is switched to high accuracy mode. Below the I_{CMP} threshold, regulator switches in any case to nominal accuracy mode (same behavior applies also in case of high current).*

2.4.5 Voltage regulator V2

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
4.5 V < V_S < 28 V, 4.5 V < V_{SREG} < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 11. Voltage regulator 2

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V2	Output voltage	V_{SREG} ≥ 5.6 V		5.0		V	C.024
ΔVo	Output voltage tracking accuracy	I_{CC2} = 100 µA to 50 mA, I_{CC1} = 30 mA, V_{SREG} = 6.5 V to 28 V	-20		20	mV	C.038
I_{CCmax2}	Output current limitation		80		170	mA	C.040
C_{load2}[(1)]	Load capacitor 2	Ceramic (±20%)	1[(2)]		10	µF	C.042
$V2_{fail}$	V2 fail threshold	V2 forced		2	3	V	C.043
t_{V2fail}	V2 fail filter time	Tested by scan		12		µs	C.056
$t_{V2short}$	V2 short filter time	Tested by scan		4		ms	C.044

1. *Specified by design, not tested in production.*
2. *Nominal capacitor value required for stability of the regulator. Tested with 1 µF ceramic (±20%). Capacitor must be located close to the regulator output pin. A 2.2 µF capacitor value is recommended to minimize the DPI stress in the application.*

2.4.6 Reset output

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.
4 V ≤ V_S ≤ 28 V, 4 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 12. Reset output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{RT1}	Reset threshold voltage1	V_{V1} decreasing	3.3	3.5	3.7	V	C.045
V_{RT2}	Reset threshold voltage2	V_{V1} decreasing	3.6	3.8	4	V	C.046
V_{RT3}	Reset threshold voltage3	V_{V1} decreasing	3.8	4.0	4.2	V	C.047
V_{RT4-1}	Reset threshold voltage4	V_{V1} decreasing	4.1	4.3	4.5	V	C.048
V_{RT4-2}	Reset threshold voltage4	V_{V1} increasing	4.6	4.75	4.9	V	C.049
V_{RESET}	Reset pin low output voltage	V1 > 1V, I_{RESET} = 5 mA		0.3	0.5	V	C.050
R_{RESET}	Reset pull-up int. resistor		70	110	180	kΩ	C.051
t_{RR}	Reset reaction time	Tested by scan	6		40	µs	C.052
t_{UV1}	V1 undervoltage filter time	Tested by scan		16		µs	C.053
t_{RD}	Reset pulse duration	Tested by scan	1.5	2.0	2.5	ms	C.054

2.4.7 Watchdog

(see also Section 3.6: Configurable window watchdog)
4.5 V < V_S < 28 V, 4.5 V < V_{SREG} < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 13. Watchdog

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{LW}	Long open window	Tested by scan	246	300	375	ms	A.027
T_{EFW1}	Early Failure window 1	Tested by scan			4.5	ms	A.028
T_{LFW1}	Late Failure window 1	Tested by scan	20			ms	A.029
T_{SW1}	Safe window 1	Tested by scan	7.5		12	ms	A.030
T_{EFW2}	Early Failure window 2	Tested by scan			22.3	ms	A.031
T_{LFW2}	Late Failure window 2	Tested by scan	100			ms	A.032
T_{SW2}	Safe window 2	Tested by scan	37.5		60	ms	A.033

Figure 3. Watchdog timing

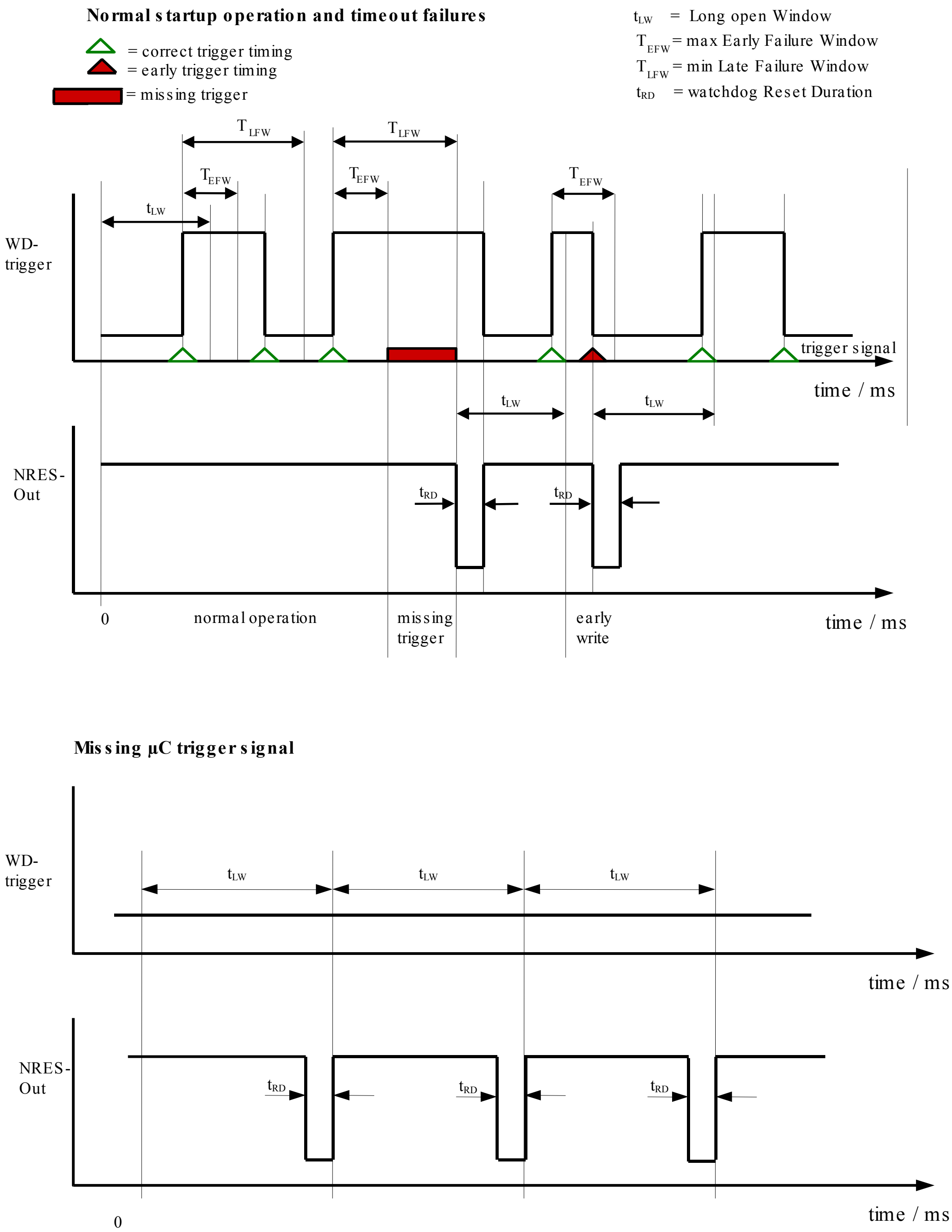
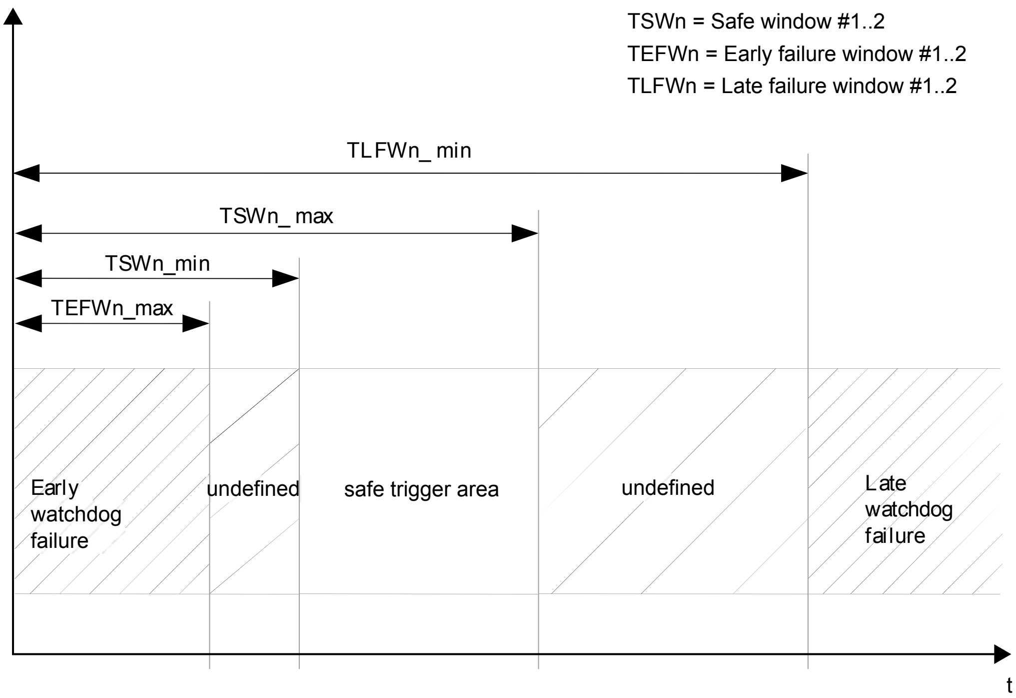


Figure 4. Watchdog early, late and safe windows



2.4.8 Current monitor output

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.

6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 14. Current monitor output

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{CM}	Functional voltage range		0		V1-1V	V	A.040
I_{CMr}	Current monitor output ratio: $I_{CM}/I_{HB1,HB6,HB21}$	0 V ≤ V_{CM} ≤ V1 - 1 V		1/9400			A.041
	I_{CM}/I_{HS7} (low on-resistance)			1/9800			A.191
	I_{CM}/I_{HB4}			1/10700			A.042
	$I_{CM}/I_{HB5,HB20}$			1/10600			A.192
	I_{CM}/I_{HS7} (high on-resistance)			1/2000			A.043
	I_{CM}/I_{HB2}			1/2020			A.044
	I_{CM}/I_{HB3}			1/2050			A.193
	$I_{CM}/I_{HS8,HS9,HS10}$			1/1000			A.045
	$I_{CM}/I_{HS11,HS12,HS13,HS14,HB16,HB17,HB18,HB19}$			1/1000			A.194
	$I_{CM}/I_{HS15, HS0}$			1/1000			A.195

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
I_{CM} acc	Current monitor accuracy for HB1, ..., HB6, HS7, .., HS10	Ranges extracted at the output: $I_{HB2,HB3min}$ = 100 mA, $I_{HB2,HB3max}$ = 0.4 A	-8% I_{HS} *I_{CMr_typ} - 2% FS (1)	0	8% I_{HS} *I_{CMr_typ} + 2% FS (1)	A	A.046
		$I_{HB1,HB6,HB21min}$ = 500 mA, $I_{HB1,HB6,HB21max}$ = 2.9 A					
		I_{HB4min} = 500 mA, I_{HB4max} = 5.9 A					
		$I_{HB5,HB20min}$ = 500 mA, $I_{HB5,HB20max}$ = 7.4 A					
		$I_{HS8,HS9,HS10min}$ = 100 mA, $I_{HS8,HS9,HS10max}$ = 0.3 A					
		$I_{HS7(High\ on\text{-}resistance)}$, I_{HSmin} = 100 mA, I_{HSmax} = 300 mA					
		$I_{HS7(Low\ on\text{-}resistance)}$, I_{HSmin} = 500 mA, I_{HSmax} = 1.4 A					
	Current monitor accuracy for HS11, .., HS19, HS0	$I_{HS11,HS12,HS13,HS14,HS15,HS16,HS17,HS18,HS19\ and\ HS0}$ I_{HSmin} = 100 mA, I_{HSmax} = 0.13 A	-8% I_{HS} *I_{CMr_typ} - 4% FS (1)	0	8% I_{HS} *I_{CMr_typ} + 4% FS (1)	A	A.047
t_{cmb} (2)	Current monitor setting time			32		μs	A.051

1. *FS (full scale) = $I_{HB(HS)max}$ * I_{CMr_typ}.*
2. *Parameter is specified by design, not tested in production.*

2.4.9 Charge pump

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
6 V < V_S < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 15. Charge pump

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Items
V_{CP}	Charge pump output voltage	V_S = 6 V, I_{CP} = -15 mA	V_S + 6	V_S + 7		V	A.052
		V_S ≥ 10 V, I_{CP} = -15 mA	V_S + 11	V_S + 12	V_S + 13.5	V	A.053
I_{CP}	Charge pump output current(1)	V_{CP} = V_S + 10 V; V_S = 13.5 V; C_1 = C_2 = C_{CP} = 100 nF	22			mA	A.054
I_{CPlim}	Charge pump output current limitation(2)	V_{CP} = V_S; V_S = 13.5 V; C_1 = C_2 = C_{CP} = 100 nF	25		70	mA	A.055
V_{CP_low}	Charge pump low threshold voltage		V_S + 4.5	V_S + 5	V_S + 5.5	V	A.056
T_{CP}	Charge pump low filter time	Tested by scan	44	64	77	μs	A.057
$t_{set,CP}$	Charge pump startup blanking time	Tested by scan	358	576	692	μs	A.183
f_{CP}	Charge pump frequency	Tested by scan		400		kHz	A.058

1. *I_{CP} is the minimum current the device can provide to an external circuit without V_{CP} going below V_S + 10 V.*
2. *I_{CPlim} is the maximum current, which flows out of the device in case of a short to V_S.*

2.4.10 Outputs HB1-HB6, HB20, HB21, HS7-HS19, HS0, ECV, ECDR

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.

6 V ≤ V_S ≤ 18 V, all outputs open, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 16. Outputs HB1–HB6, HB20, HB21, HS7–HS19, HS0, ECV, ECDR

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$r_{ON\ HB1,\ HB6,\ HB21}$	On-resistance to supply or GND	V_S = 13.5 V, T_A = 25 °C, $I_{HB1,HB6,\ HB21}$ = ±1.5 A		300	400	mΩ	D.001
		V_S = 13.5 V, T_A = 125 °C, $I_{HB1,HB6,\ HB21}$ = ±1.5 A		450	600	mΩ	D.002
$r_{ON\ HB2,\ HB3}$	On-resistance to supply or GND	V_S = 13.5 V, T_A = 25 °C, $I_{HB2,HB3}$ = ±0.4 A		1600	2200	mΩ	D.005
		V_S = 13.5 V, T_A = 125 °C, $I_{HB2,HB3}$ = ±0.4 A		2500	3400	mΩ	D.006
$r_{ON\ HB4}$	On-resistance to supply or GND	V_S = 13.5 V, T_A = 25 °C, I_{HB4} = ±3 A		150	200	mΩ	D.093
		V_S = 13.5 V, T_A = 125 °C, I_{HB4} = ±3 A		225	300	mΩ	D.094
$r_{ON\ HB5,\ HB20}$	On-resistance to supply or GND	V_S = 13.5 V, T_A = 25 °C, I_{HB5} = ±3 A		100	140	mΩ	D.095
		V_S = 13.5 V, T_A = 125 °C, I_{HB5} = ±3 A		140	190	mΩ	D.096
$r_{ON\ HS7}$	On-resistance to supply in low resistance mode	V_S = 13.5 V, T_A = 25 °C, I_{HS7} = -1.1 A		300	420	mΩ	D.007
		V_S = 13.5 V, T_A = 125 °C, I_{HS7} = -1.1 A		450	620	mΩ	D.008
	On-resistance to supply in high resistance mode	V_S = 13.5 V, T_A = 25 °C, I_{HS7} = -0.2 A		1600	2200	mΩ	D.009
		V_S = 13.5 V, T_A = 125 °C, I_{HS7} = -0.2 A		2500	3400	mΩ	D.010
$r_{ON\ HS8,\ HS9,\ HS10}$	On-resistance to supply	V_S = 13.5 V, T_A = 25 °C, $I_{HS8,HS9,HS10}$ = -0.4 A		1400	2200	mΩ	D.011
		V_S = 13.5 V, T_A = 125 °C, $I_{HS8,HS9,HS10}$ = -0.4 A		2700	3400	mΩ	D.012
$r_{ON\ HS0,\ HS11,\ HS12,\ HS13,\ HS14,\ HS15,\ HS16,\ HS17,\ HS18,\ HS19}$	On-resistance to supply	V_S = 13.5 V, T_A = 25 °C, $I_{HS0,HS11,HS12,HS13,HS14,HS15,HS16,HS17,HS18,HS19}$ = -60 mA		7	10	Ω	D.017
		V_S = 13.5 V, T_A = 125 °C, $I_{HS0,HS11,HS12,HS13,HS14,HS15,HS16,HS17,HS18,HS19}$ = -60 mA		11	15	Ω	D.018
$r_{ON\ ECV}$	On-resistance to GND	V_S = 13.5 V, T_A = 25 °C, $I_{OUTECV,ECFD}$ = +0.4 A		1600	2200	mΩ	D.019
		V_S = 13.5 V, T_A = 125 °C, $I_{OUTECV,ECFD}$ = 0.4 A		2500	3400	mΩ	D.020
I_{QLH}	Switched-off output current high-side drivers of HS7-HS15, HS0, HS16-HS19 (1)	V_{OUT} = 0 V, standby mode	-5			µA	D.021
		V_{OUT} = 0 V, active mode	-10			µA	D.022

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
I_{QLH}	Switched-off output current high-side drivers of HB1-HB6, HB20, HB21 (1)	V_{OUT} = 0 V, standby mode	-6			µA	D.023
		V_{OUT} = 0 V, active mode	-100			µA	D.024
I_{QLL}	Switched-off output current low-side drivers of HB1-HB6, HB20, HB21 (1)	V_{OUT} = V_S, standby mode			165	µA	D.025
		V_{OUT} = V_S -0.5 V, active mode	-100			µA	D.026
	Switched-off output current low-side driver of ECV (1)	V_{OUT} = V_S -2.5 V, standby mode (with E_{CDR} = V_S)	-15		15	µA	D.027
		V_{OUT} = V_S - 2.5 V, active mode (with E_{CDR} = V_S)	-10			µA	D.028

1. *Negative value: leakage internally sink from driver output pin to internal IC ground. Positive value: leakage sourced from internal driver output pin to external ground.*

2.4.11 Power outputs switching times

Table 17. Power outputs switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Items
$t_{d\ ON\ H}$	Output delay time high-side driver on HS7 low resistance	V_S = 13.5 V(1)(2) See Figure 12. SPI CSN output timing	5.5		77.5	µs	D.099
	Output delay time high-side driver on HS7 high resistance		15	35	60	µs	D.100
$t_{d\ OFF\ H}$	Output delay time high-side driver off HS7 low resistance	V_S = 13.5 V(1)(2) See Figure 12. SPI CSN output timing	7	150	300	µs	D.101
	Output delay time high-side driver off HS7 high resistance		9	18	45	µs	D.102
$t_{d\ ON\ H}$	Output delay time high-side driver on (HB1,HB6, HB21)	V_S = 13.5 V(2) corresponding high-side driver is not active; Rload = 16 Ω (from CSN 50% to OUT 20%)	0.05		5	µs	D.029
$t_{d\ OFF\ H}$	Output delay time high-side driver off (HB1,HB6, HB21)	V_S = 13.5 V(2) Rload = 16 Ω (from CSN 50% to OUT 80%)	0.05		7	µs	D.031
$t_{d\ ON\ L}$	Output delay time low-side driver on (HB1,HB6, HB21)	V_S = 13.5 V(2) corresponding high-side driver is not active 3 Rload = 16 Ω (from CSN 50% to OUT 80%)	0.05		3	µs	D.035
$t_{d\ OFF\ L}$	Output delay time low-side driver off (HB1,HB6, HB21)	V_S = 13.5 V(1) corresponding high-side driver is not active 1 (from CSN 50% to OUT 20%)	0.05		3	µs	D.036
$t_{d\ ON\ H}$	Output delay time high-side driver on (HB2,HB3)	V_S = 13.5 V(2) corresponding high-side driver is not active; (from CSN 50% to OUT 20%)	5.5		77.5	µs	D.103

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Items
$t_{d\ OFF\ H}$	Output delay time high-side driver off (HB2,HB3)	V_S = 13.5 V(2) (from CSN 50% to OUT 80%)	20	70	140	µs	D.104
$t_{d\ ON\ L}$	Output delay time low-side driver on (HB2,HB3)	V_S = 13.5 V(2) corresponding high-side driver is not active; (from CSN 50% to OUT 80%)	10	30	70	µs	D.105
$t_{d\ OFF\ L}$	Output delay time low-side driver off (HB2,HB3)	V_S = 13.5 V(2) (from CSN 50% to OUT 20%)	35	150	300	µs	D.106
$t_{d\ ON\ H}$	Output delay time high-side driver on (HB4)	V_S = 13.5 V(3) corresponding high-side driver is not active; (from CSN 50% to OUT 20%)	0.05		5	µs	D.107
$t_{d\ OFF\ H}$	Output delay time high-side driver off (HB4)	V_S = 13.5 V(3) (from CSN 50% to OUT 80%)	0.05		7	µs	D.108
$t_{d\ ON\ L}$	Output delay time low-side driver on (HB4)	V_S = 13.5 V(3) corresponding high-side driver is not active; (from CSN 50% to OUT 80%)	0.05		3	µs	D.109
$t_{d\ OFF\ L}$	Output delay time low-side driver off (HB4)	V_S = 13.5 V(3) (from CSN 50% to OUT 20%)	0.05		3	µs	D.110
$t_{d\ ON\ H}$	Output delay time high-side driver on (HB5, HB20)	V_S = 13.5 V(3) corresponding high-side driver is not active; (from CSN 50% to OUT 20%)	0.05		5	µs	D.111
$t_{d\ OFF\ H}$	Output delay time high-side driver off (HB5, HB20)	V_S = 13.5 V(3) (from CSN 50% to OUT 80%)	0.05		7	µs	D.112
$t_{d\ ON\ L}$	Output delay time low-side driver on (HB5, HB20)	V_S = 13.5 V(3) corresponding high-side driver is not active; (from CSN 50% to OUT 80%)	0.05		3	µs	D.113
$t_{d\ OFF\ L}$	Output delay time low-side driver off (HB5, HB20)	V_S = 13.5 V(3) (from CSN 50% to OUT 20%)	0.05		3	µs	D.114
$T_{d\ OFF\ H}$	Output delay time high-side driver HS8,HS9,HS10 OFF (delay between CSN or DIR 50% to OUT at 20% of VS)	V_S = 13.5 V, V1 = 5 V, R_{load} = 128 Ω	5		70	µs	D.115
$T_{d\ ON\ H}$	Output delay time high-side driver HS8,HS9,HS10 ON (delay between CSN or DIR 50% to OUT at 20% of VS)	V_S = 13.5 V, V1 = 5 V, R_{load} = 128 Ω	2		50	µs	D.116
$T_{d\ OFF\ H}$	Output delay time high-side driver OFF (HS11,..,HS19,HS0) (delay between CSN or DIR 50% to OUT at 20% of VS)	V_S = 13.5 V, V1 = 5 V, R_{load} = 128 Ω	20		140	µs	D.034
$T_{d\ ON\ H}$	Output delay time high-side driver ON (HS11,..,HS19,HS0) (delay between CSN or DIR 50% to OUT at 80% of VS)	V_S = 13.5 V, V1 = 5 V, R_{load} = 128 Ω	10		60	µs	D.033
$t_{d\ ON\ L}$	Output delay time low-side driver on (ECV)	V_S = 13.5 V(1)(2)(3) See Figure 12. SPI CSN output timing	10	30	70	µs	D.134

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Items
$t_{d\ OFF\ L}$	Output delay time low-side driver off (ECV)	V_S = 13.5 V(1)(2)(3) See Figure 12. SPI CSN output timing	25	90	200	µs	D.037
t_{CCP}	Cross current protection time HB1,… HB6, HB20, HB21		180	300	500	µs	D.038
$d_{VOUT/dt}$	Slew rate for drivers HB2,HB3, HS7-HS19, HS0, LS ECV	V_S = 13.5 V(1)(2)(3)(4)		0.2		V/µs	D.040
	Slew rate on output drivers HB1,HB4,HB5, HB6, HB20, HB21 controlled by PWM4-5 / PWM1-6, PWM20 and PWM21	V_S = 13.5 V(1)(2)(3)(4)	6	10	20	V/µs	D.117
$d_{Vmax/dt}$(5)	Maximum external applied slew rate on HB1-HB6, HB20, HB21 without switching on the LS and HS		20			V/µs	D.041
f_{PWM1}	PWM switching frequency Tested by scan	V_S/V_{SREG} = 13.5 V		100		Hz	D.043
f_{PWM2}	PWM switching frequency Tested by scan	V_S/V_{SREG} = 13.5 V		200		Hz	D.044
DC1	SPI configurable duty cycle for HS7… HS19 and HS0 Tested by scan	0.1% steps	0.1		100	%	D.118

1. *R_{load} = 16 Ω at HB1, HB6, HB21, and HS7 in low on-resistance mode.*
2. *R_{load} = 128 Ω at HB2, HB3, HS8, HS9, HS10, HS11, HS12, HS13, HS14, HS15, HS16, HS17, HS18, HS19, HS0, ECV and HS7 in high on-resistance mode.*
3. *R_{load} = 4 Ω at HB4,HB5.*
4. *Slope $d_{VOUT/dt}$ is measured between 20% and 80% of the final output voltage value.*
5. *Parameter specified by design, not tested in production.*

2.4.12 Output current thresholds

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V; 6 V < V_{SREG} < 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 18. **Output current thresholds**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$\lvert I_{SC1}\rvert$ $\lvert I_{SC6}\rvert$ $\lvert I_{SC21}\rvert$	Short-current threshold HS and LS	V_S = 13.5 V, V1 = 5 V, sink full V_S range is specified by design	5		11	A	D.049
$\lvert I_{SC2}\rvert$ $\lvert I_{SC3}\rvert$	Short-current threshold HS and LS	V_S = 13.5 V, V1 = 5 V, sink full V_S range is specified by design	0.9		1.8	A	D.047
$\lvert I_{SC4}\rvert$	Short-current threshold HS and LS	V_S = 13.5 V, V1 = 5 V, sink full V_S range is specified by design	9		19	A	D.119
$\lvert I_{SC5}\rvert$ $\lvert I_{SC20}\rvert$	Short-current threshold HS and LS	V_S = 13.5 V, V1 = 5 V, sink full V_S range is specified by design	10		21	A	D.120
$\lvert I_{OC1th1}\rvert$	Overcurrent threshold HS and LS of HB1 (config. 1)	V_S = 13.5 V, Current limitation set by CR16, bit 12 and 13	1.5	2	2.7	A	D.121
$\lvert I_{OC1th2}\rvert$	Overcurrent threshold HS and LS of HB1 (config. 2)		2.25	3	4	A	D.122
$\lvert I_{OC1th3}\rvert$	Overcurrent threshold HS and LS of HB1 (config. 3)		3	4	4.9	A	D.123
$\lvert I_{OC2}\rvert$ $\lvert I_{OC3}\rvert$	Overcurrent threshold HS and LS	V_S = 13.5 V, sink and source	0.5		1.0	A	D.050
$\lvert I_{OC4}\rvert$			6		9.2	A	D.124
$\lvert I_{OC5th1}\rvert$	Overcurrent threshold HS and LS of HB5 (config. 1)	V_S = 13.5 V, Current limitation set by CR16, bit 14 and 15	3.4	4	5.3	A	D.125
$\lvert I_{OC5th2}\rvert$	Overcurrent threshold HS and LS of HB5 (config. 2)		5.1	6	7.9	A	D.126
$\lvert I_{OC5th3}\rvert$	Overcurrent threshold HS and LS of HB5 (config. 3)		7.5		10.5	A	D.127
$\lvert I_{OC6th1}\rvert$	Overcurrent threshold HS and LS of HB6 (config. 1)	V_S = 13.5 V, Current limitation set by CR16, bit 16 and 17	1.5	2	2.7	A	D.128
$\lvert I_{OC6th2}\rvert$	Overcurrent threshold HS and LS of HB6 (config. 2)		2.25	3	4	A	D.129
$\lvert I_{OC6th3}\rvert$	Overcurrent threshold HS and LS (config. 3)		3	4	4.9	A	D.052
$\lvert I_{OC7}\rvert$	Overcurrent threshold HS in low on-resistance mode	V_S = 13.5 V, source	1.5		2.5	A	D.053
	Overcurrent threshold HS in high on-resistance mode		0.35		0.65	A	D.054
$\lvert I_{OC8}\rvert$ $\lvert I_{OC9}\rvert$ $\lvert I_{OC10}\rvert$	Overcurrent threshold HS		0.5		1	A	D.059
$\lvert I_{OC11}\rvert$ $\lvert I_{OC12}\rvert$ $\lvert I_{OC13}\rvert$ $\lvert I_{OC14}\rvert$ $\lvert I_{OC15}\rvert$			0.19		0.35	A	D.062

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$\|I_{OC16}\|$ $\|I_{OC17}\|$ $\|I_{OC18}\|$ $\|I_{OC19}\|$ $\|I_{OC0}\|$	Overcurrent threshold HS	V_S = 13.5 V, source					
$\|I_{OC20}\|$	Overcurrent threshold HS	V_S = 13.5 V, sink and source	7.5	8	10.5	A	D.131
$\|I_{OC21}\|$	Overcurrent threshold HS	V_S = 13.5 V, sink and source	3	4	4.9	A	D.132
$\|I_{OCECV}\|$	Output current limitation LS	V_S = 13.5 V, sink	0.5		1.0	A	D.063
$\|I_{CCM7}\|$ $\|I_{CCM8}\|$ $\|I_{CCM9}\|$ $\|I_{CCM10}\|$ $\|I_{CCM11}\|$ $\|I_{CCM12}\|$ $\|I_{CCM13}\|$ $\|I_{CCM14}\|$ $\|I_{CCM15}\|$ $\|I_{CCM16}\|$ $\|I_{CCM17}\|$ $\|I_{CCM18}\|$ $\|I_{CCM19}\|$ $\|I_{CCM0}\|$	Constant current mode value for HS7 (in high on-resistance mode) to HS19 and HS0	V_S = 13.5 V; HSx_CCM = 1 (x = 7 to 19, 0)	100			mA	D.064
$t_{CCMtimeout}$	Constant current mode expiration time	HSx_CCM = 1 (x = 7 to 19, 0) tested by scan		20		ms	D.065
t_{FSC}	Filter time of short-current signal in half bridge outputs	Tested by scan	1	3	6.5	µs	D.066
t_{FOC}	Filter time of overcurrent signal in HS11, .., HS19 and HS0	Tested by scan		48		µs	D.137
t_{BLK}	Blanking time of overcurrent signal (all outputs) and of short-circuit current signal in half bridges	Tested by scan		40		µs	D.067
t_{FOC_PWM} (1)	Filter time of overcurrent signal in all half bridges in PWM mode (no blanking time t_{BLK} applied)		5	9	12	µs	D.135
t_{FSC_PWM} (1)	Filter time of short-circuit current signal in all half bridges in PWM mode (no blanking time t_{BLK} applied)		4	7	10	µs	D.136
t_{OCR00}	T_{ON} time of overcurrent signal in HB1,.. HB6, HB20, HB21, HS7, .., HS10 (includes blanking time t_{BLK} and is also valid if OCR is disabled) Tested by scan	xx_OCR_TON[0,1] = 00		88		µs	D.068
t_{OCR01}		xx_OCR_TON[0,1] = 01		80		µs	D.069
t_{OCR10}		xx_OCR_TON[0,1] = 10		72		µs	D.070
t_{OCR11}		xx_OCR_ TON[0,1] = 11		64		µs	D.071
f_{OCR00}	Recovery frequency for OC	xx_OCR_FREQ[0,1] = 00		1.7		kHz	D.072

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
f_{OCR01}	Tested by scan	xx_OCR_FREQ[0,1] = 01		2.2		kHz	D.073
f_{OCR10}		xx_OCR_FREQ[0,1] = 10		3		kHz	D.074
f_{OCR11}		xx_OCR_FREQ[0,1] = 11		4.4		kHz	D.075
$\|I_{OLD1}\|$(2) $\|I_{OLD6}\|$(2) $\|I_{OLD21}\|$(2)	Undercurrent threshold HS and LS	V_S = 13.5 V, sink and source	1	30	95	mA	D.079
$\|I_{OLD2}\|$(2) $\|I_{OLD3}\|$(2)			1	20	36	mA	D.078
$\|I_{OLD4}\|$(2) $\|I_{OLD5}\|$(2) $\|I_{OLD20}\|$(2)			30	150	300	mA	D.133
$\|I_{OLD7}\|$(2)	Undercurrent threshold HS in low on-resistance mode	V_S / V_{SREG} = 13.5 V source	15	50	90	mA	D.081
	Undercurrent threshold HS in high on-resistance mode		3	12	25	mA	D.082
$\|I_{OLD8}\|$(2) $\|I_{OLD9}\|$ $\|I_{OLD10}\|$(2)	Undercurrent threshold HS		10	20	30	mA	D.083
$\|I_{OLD11}\|$(2) $\|I_{OLD12}\|$(2) $\|I_{OLD13}\|$(2) $\|I_{OLD14}\|$(2) $\|I_{OLD15}\|$ $\|I_{OLD16}\|$(2) $\|I_{OLD17}\|$(2) $\|I_{OLD18}\|$(2) $\|I_{OLD19}\|$(2) $\|I_{OLD0}\|$(2)	Undercurrent threshold HS		0.2	0.65	1.5	mA	D.086
$\|I_{OLDECV}\|$(2)	Undercurrent threshold LS	V_S = 13.5 V, sink	2	20	35	mA	D.091
t_{FOL}	Filter time of open-load signal	Duration of open-load condition to set the status bit. Tested by scan		200		μs	D.092

1. *Parameter specified by design, not tested in production.*
2. *I_{OLD} parameters, in the range 8 V to 16 V, are specified by design and evaluated by characterization. Production testing is done at 13.5 V.*

2.4.13 Heater

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.
6 V < V_S < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 19. Heater

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$I_{GHheater}$	Average charge current (charge sage)	T_J = 25°C		0.3		A	A.059
$V_{GHheater}$	Gate-on voltage	V_S = SH = 6 V; No load	$V_{SHeater}$ + 6			V	A.062
		V_S = SH = 12 V; No load	$V_{SHeater}$ + 8	$V_{SHeater}$ + 10	$V_{SHeater}$ + 12	V	A.063
$R_{GSHeater}$	Passive gate clamp resistance	Measurement of the slope between V_{GHx} = 6 V and V_{GHx} = 3 V		15		kΩ	A.064
$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode)1	V_S = 13.5 V, V_{SHx} = 0 V, R_G = 0 Ω, C_G = 2.7 nF		1.5		µs	A.065
$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode)	V_S = 13.5 V, V_{SLx} = 0, R_G = 0 Ω, C_G = 2.7 nF		1.5		µs	A.066
$t_{0GHheaterr}$	Rise time (switch mode)	V_S = 13.5 V, $V_{Sheater}$ = 0, R_G = 0 Ω, C_G = 2.7 nF		45		ns	A.067
$t_{0GHheaterf}$	Fall Time (switch mode)	V_S = 13.5 V, $V_{Sheater}$ = 0, R_G = 0 Ω, C_G = 2.7 nF		85		ns	A.068

2.4.14 H-bridge driver

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin.
6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 20. H-bridge driver

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$I_{GHx(Ch)}$	Average charge current (charge stage)	T_J = 25°C	0.1	0.3	0.75	A	A.069
R_{GHx}	On-resistance (discharge stage)	V_{SHx} = 0 V, I_{GHx} = 50 mA, T_J = 25°C	4	8	12	Ω	A.070
		V_{SHx} = 0 V, I_{GHx} = 50 mA, T_J = 125°C		12	18	Ω	A.071
V_{GHHx}	Gate on voltage	V_S = SH = 6 V; I_{CP} = 15 mA	V_{SHx} + 6			V	A.072
		V_S = SH = 12 V; I_{CP} = 15 mA	V_{SHx} + 8	V_{SHx} + 10	V_{SHx} + 11.5	V	A.073
R_{GSHx}	Passive gate clamp resistance	Measurement of the slope between V_{GHx} = 6 V and V_{GHx} = 3 V		15		kΩ	A.074
Drivers for external low-side Power MOSFET							
$I_{GLx(Ch)}$	Average charge current (charge stage)	T_J = 25°C	0.1	0.3	0.75	A	A.075
R_{GLx}	On-resistance (discharge stage)	V_{SLx} = 0 V, I_{GLx} = 50 mA, T_J = 25°C	4	8	12	Ω	A.076
		V_{SLx} = 0 V, I_{GLx} = 50 mA, T_J = 125°C		12	18	Ω	A.077
V_{GHLx}	Gate on voltage	V_S = 6 V; I_{CP} = 15 mA	V_{SLx} + 6			V	A.078
		V_S = 12 V; I_{CP} = 15 mA	V_{SLx} + 8	V_{SLx} + 10	V_{SLx} + 11.5	V	A.079
R_{GSLx}	Passive gate clamp resistance			15		kΩ	A.080

2.4.15 Gate drivers for the external Power MOSFET switching times

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V; 6 V < V_{SREG} < 28 V; T_J = -40 °C to 150 °C, unless otherwise specified.

Table 21. Gate drivers for external Power MOSFET switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$T_{G(HL)xHL}$	Propagation delay time high to low (switch mode)(1)	V_S = 13.5 V, V_{SHx} = 0, R_G = 0 Ω, C_G = 2.7 nF		1.5		µs	A.081
$T_{G(HL)xLH}$	Propagation delay time low to high (switch mode)(1)	V_S = 13.5 V, V_{SLx} = 0, R_G = 0 Ω, C_G = 2.7 nF		1.5		µs	A.082
$I_{GHxrmax}$	Maximum source current (current mode)	V_S = 13.5 V, V_{SHx} = 0, V_{GHx} = 1 V, SLEW<4:0> = 1FH		32		mA	A.083
$I_{GHxfmax}$	Maximum sink current (current mode)	V_S = 13.5 V, V_{SHx} = 0, V_{GHx} = 2 V, SLEW<4:0> = 1FH		32		mA	A.084
d_{IIGHxr}	Source current accuracy	V_S = 13.5 V, V_{SHx} = 0 V, V_{GHx} = 1 V		See Figure 6. IGHxr range (a)			A.085
d_{IIGHxf}	Sink current accuracy	V_S = 13.5 V, V_{SHx} = 0 V, V_{GHx} = 2 V		See Figure 7. IGHxf range (b)			A.086
$V_{DSHxrSW}$(2)	Switching voltage (V_S-V_{SH}) between current mode and switch mode (rising)	V_S = 13.5 V	0.4	1.5	2.6	V	A.087
$V_{DSHxfSW}$(2)	Switching voltage (V_S-V_{SH}) between switch mode and current mode (falling)	V_S = 13.5 V	0.4	1.5	2.6	V	A.088
t_{0GHxr}	Rise time (switch mode)	V_S = 13.5 V, V_{SHx} = 0 V, R_G = 0 Ω, C_G = 2.7 nF		45		ns	A.089
t_{0GHxf}	Fall time (switch mode)	V_S = 13.5 V, V_{SHx} = 0 V, R_G = 0 Ω, C_G = 2.7 nF		85		ns	A.090
t_{0GLxr}	Rise time	V_S = 13.5 V, V_{SLx} = 0 V, R_G = 0 Ω, C_G = 2.7 nF		45		ns	A.091
t_{0GLxf}	Fall time	V_S = 13.5 V, V_{SLx} = 0 V, R_G = 0 Ω, C_G = 2.7 nF		85		ns	A.092
$t_{ccp0010}$	Programmable cross current protection time	Tested by scan		750		ns	A.095
$t_{ccp0011}$	Programmable cross current protection time	Tested by scan		1000		ns	A.096
$t_{ccp0100}$	Programmable cross current protection time	Tested by scan		1250		ns	A.097
$t_{ccp0101}$	Programmable cross current protection time	Tested by scan		1500		ns	A.098
$t_{ccp0110}$	Programmable cross current protection time	Tested by scan		1750		ns	A.099
$t_{ccp0111}$	Programmable cross current protection time	Tested by scan		2000		ns	A.100
$t_{ccp1000}$	Programmable cross current protection time	Tested by scan		2250		ns	A.101

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$t_{ccp1001}$	Programmable cross current protection time	Tested by scan		2500		ns	A.102
$t_{ccp1010}$	Programmable cross current protection time	Tested by scan		2750		ns	A.103
$t_{ccp1011}$	Programmable cross current protection time	Tested by scan		3000		ns	A.104
$t_{ccp1100}$	Programmable cross current protection time	Tested by scan		3250		ns	A.105
$t_{ccp1101}$	Programmable cross current protection time	Tested by scan		3500		ns	A.106
$t_{ccp1110}$	Programmable cross current protection time	Tested by scan		3750		ns	A.107
$t_{ccp1111}$	Programmable cross current protection time	Tested by scan		4000		ns	A.108
f_{PWMH}	PWMH switching frequency (1)	V_S = 13.5 V, V_{SLx} = 0, R_G = 0 Ω, C_G = 2.7 nF, PWMH-duty-cycle = 50%			50	kHz	A.109

1. *Without cross-current protection time t_{CCP}.*
2. *Specified by design, not tested in production.*

Figure 5. H-Driver delay times

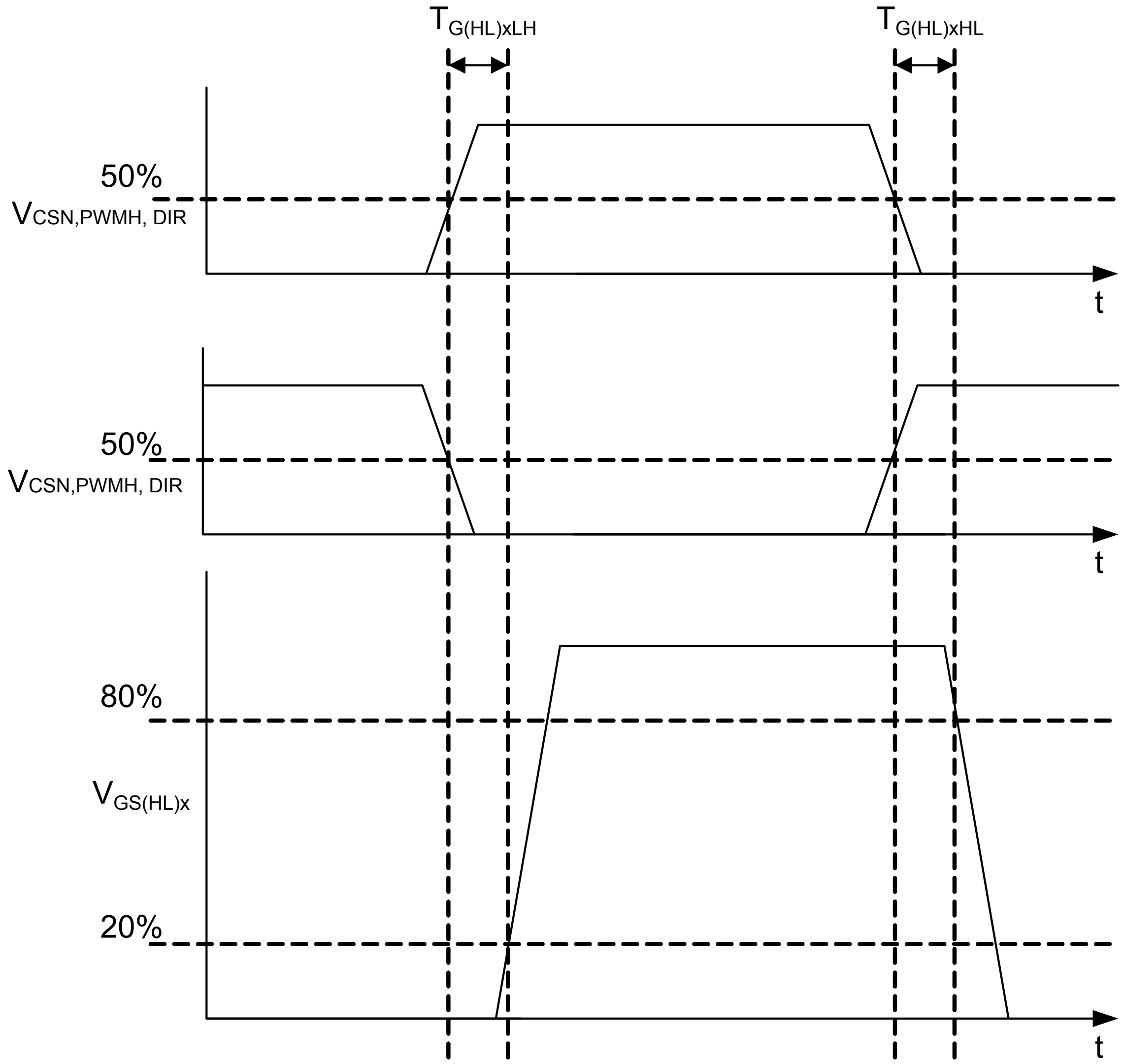


Figure 6. IGHxr range (a)

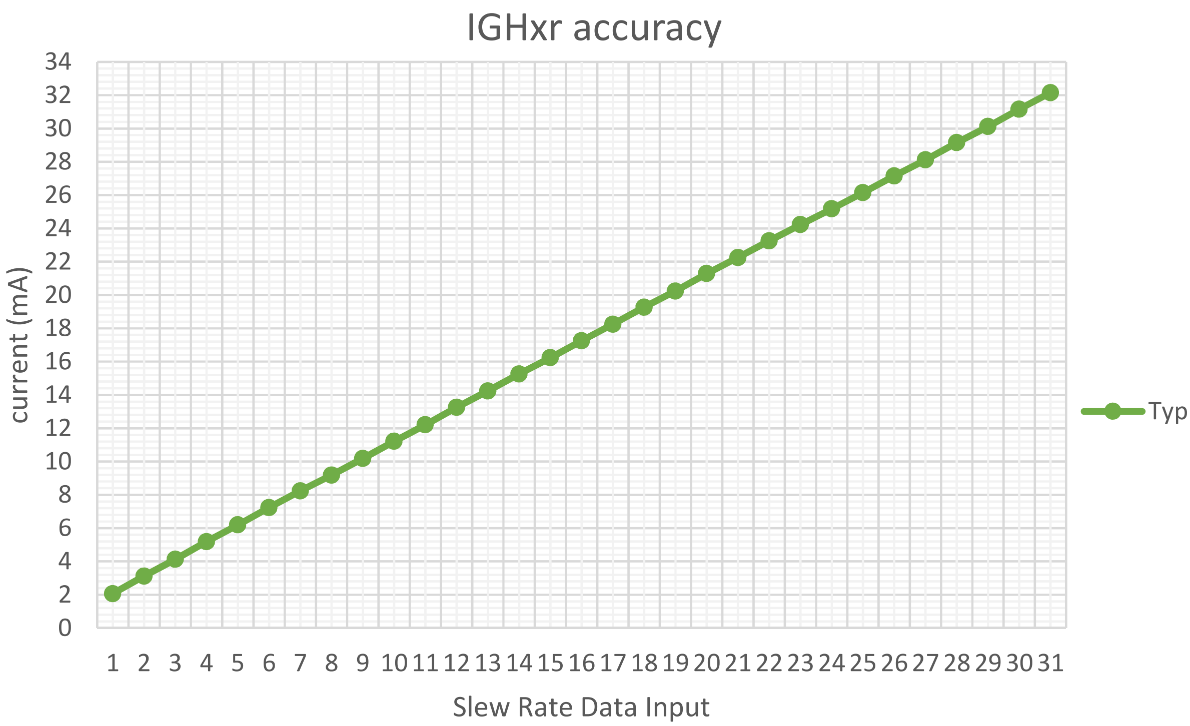
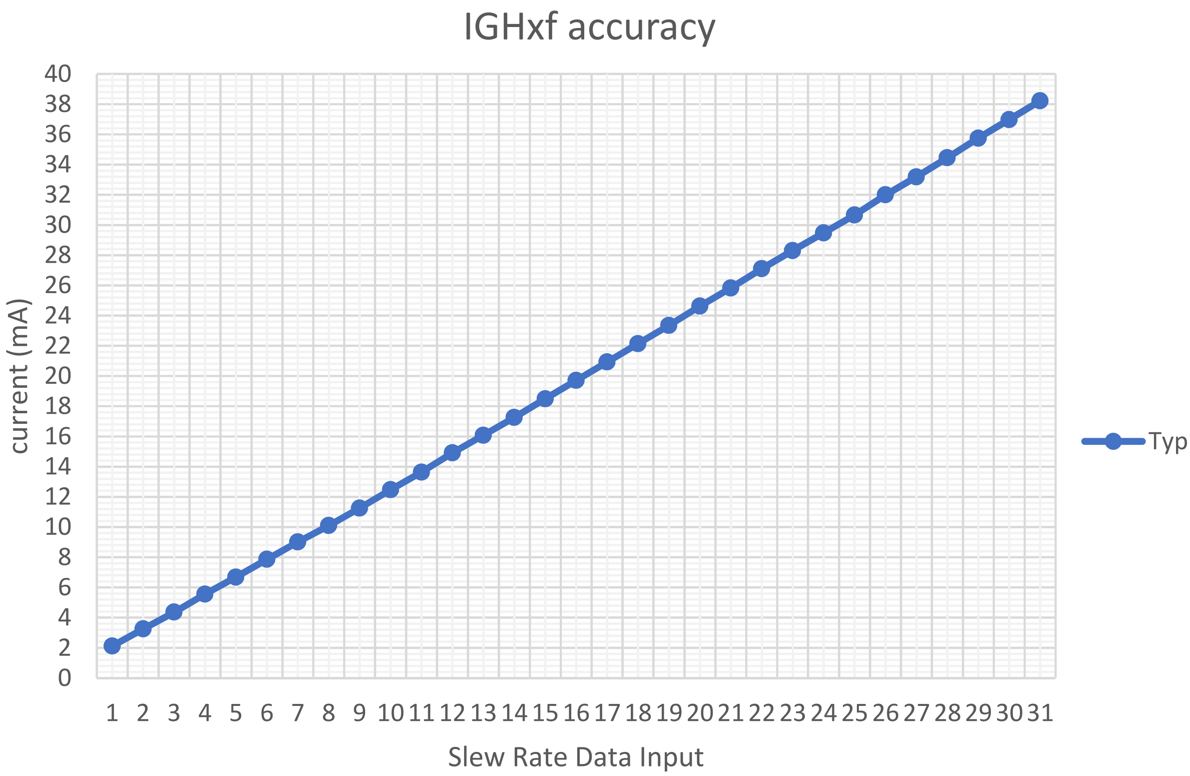


Figure 7. IGHxf range (b)



2.4.16 Drain-source monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 22. Drain-source monitoring external H-bridge

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{scd1_HS}	Drain-source threshold voltage on HS		0.4	0.55	0.7	V	A.110
V_{scd1_LS}	Drain-source threshold voltage on LS		0.3	0.45	0.6	V	A.196
V_{scd2_HS}	Drain-source threshold voltage on HS		0.89	1.05	1.2	V	A.111
V_{scd2_LS}	Drain-source threshold voltage on LS		0.75	0.95	1.15	V	A.197
V_{scd3_HB}	Drain-source threshold voltage		1.27	1.5	1.73	V	A.112
V_{scd4_HB}	Drain-source threshold voltage		1.7	2	2.3	V	A.113
t_{SCd_HB}	Drain-source monitor filter time	Tested by scan		6		µs	A.117
t_{scs_HB}	Drain-source comparator settling time	V_S = 13.5 V, V_{SH} = jump from GND to V_S			5	µs	A.118

2.4.17 Drain-source monitoring external heater Power MOSFET

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 23. Drain-source monitoring external heater Power MOSFET

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{SCd1_HE}	Drain-source threshold voltage		175	205	240	mV	A.119
V_{SCd2_HE}	Drain-source threshold voltage		220	256	295	mV	A.120
V_{SCd3_HE}	Drain-source threshold voltage		265	308	350	mV	A.121
V_{SCd4_HE}	Drain-source threshold voltage		310	360	405	mV	A.122
V_{SCd5_HE}	Drain-source threshold voltage		350	410	460	mV	A.123
V_{SCd6_HE}	Drain-source threshold voltage		395	460	515	mV	A.124
V_{SCd7_HE}	Drain-source threshold voltage		440	513	570	mV	A.125
V_{SCd8_HE}	Drain-source threshold voltage		480	564	625	mV	A.126
V_{SCd9_HE}	Drain-source threshold voltage		525	615	680	mV	A.184
V_{SCd10_HE}	Drain-source threshold voltage		570	666	735	mV	A.185
t_{SCd_HE}	Drain-source monitor filter time	Tested by scan		6		µs	A.127
t_{scs_HE}	Drain-source comparator settling time	V_S = 13.5 V; V_{SH} = jump from GND to V_S			5	µs	A.128

2.4.18 Open-load monitoring external H-bridge

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 24. Open-load monitoring external H-bridge

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{ODSL}	Low-side drain-source monitor low threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	0.05xV_S	0.15xV_S	0.25xV_S	V	A.130
V_{ODSH}	Low-side drain-source monitor high off threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	0.75xV_S	0.85xV_S	0.95xV_S	V	A.131
V_{OLSHx}	Output voltage of selected S_{Hx} in open-load test mode	V_{SLx} = 0 V; V_S = 13.5 V	0.4xV_S	0.5xV_S	0.6xV_S	V	A.132
R_{pdOL}	Pulldown resistance of the non selected S_{Hx} pin in open-load mode	V_{SLx} = 0 V; V_S = 13.5 V; V_{SHX} = 4.5 V		20		kΩ	A.133
t_{OL_HB}	Open-load filter time	Tested by scan		2		ms	A.134

2.4.19 Open-load monitoring external heater Power MOSFET

The voltages are referred to power ground and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 25. Open-load monitoring external heater Power MOSFET

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{OLheater}$	Open-load threshold voltage	V_{SLx} = 0 V; V_S = 13.5 V	1	2	3	V	A.135
$I_{OLheater}$	Pull-up current source open-load diagnosis activated	V_{SLx} = 0 V; V_S = 13.5 V; $V_{SHheater}$ = 4.5 V	0.5	1	2	mA	A.136
t_{OL_HE}	Open-load filter time	Tested by scan		2		ms	A.137

2.4.20 Electrochrome mirror driver

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin. 6 V < V_S < 28 V, 6 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 26. Electrochrome mirror driver

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{CTRLmax}$	Maximum EC-control voltage	Bit19 = 1 in CR1 (0x26)(1)	1.4		1.6	V	A.138
		Bit19 = 0 in CR1 (0x26)(1)	1.12		1.28	V	A.139
DNL_{ECV}	Differential Non Linearity		-1		1	LSB(2)(3)	A.140
I_{dVECVI}	Voltage deviation between target and ECV	dV_{ECV} = V_{target} (4) - V_{ECV}, $I I_{ECDR} I$ < 1 µA	-5%-1LSB(2)		+5%+1LSB(2)	mV	A.141
d_{VECVnr}	Difference voltage between target and ECV sets flag if VECV is below it	dV_{ECV} = V_{target}(4) - V_{ECV} toggle bitx = 1 status reg. x		120		mV	A.142
d_{VECVhi}	Difference voltage between target and ECV sets flag if VECV is above it	dV_{ECV} = V_{target}(4) - V_{ECV} toggle bitx = 1 status reg. x		-120		mV	A.143
t_{FECVNR}	ECVNR filter time	Tested by scan		32		µs	A.144

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{FECVHI}	ECVHI filter time	Tested by scan		32		μs	A.145
$V_{ECDRminHIGH}$	Output voltage range	I_{ECDR} = -10 μA	V1-0.3		V1	V	A.146
$V_{ECDRmaxLOW}$		I_{ECDR} = 10 μA	0		0.7	V	A.147
I_{ECDR}	Current into ECDR	V_{target}[(4)] > V_{ECV} +500 mV, V_{ECDR} = 3.5 V	-100		-10	μA	A.148
		V_{target}[(4)] < V_{ECV} - 500 mV, V = 1.0 V; Vtarget = 0 V; V_{ECV} = 0.5 V	10		100	μA	A.149
$R_{ecdrdis}$	Pull-down resistance at ECDR in fast discharge mode and while EC mode is off.	V_{ECDR} = 0.7 V ; ECON = '1', EC<5:0> = 0 or ECON = '0'			10	kΩ	A.150

1. *Bit ECV_HV = '1' or '0': ECV voltage, where II$_{ECDR}$ can change sign.*
2. *1 LSB (least significant bit) = 23.8m V_{typ}.*
3. *0000 DAC code is not included in DNL_{ECV} test.*
4. *V_{target} is set by bits EC_[5:0] and bit ECV_HV; tested for each individual bit.*

2.4.21 External interrupts (EI1, DIR1/EI2,EI3 .. EI9)

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V < V_{SREG} < 28 V, T_J = -40 to 150°C, unless otherwise specified.

Table 27. External interrupts

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{WU_THn}	Wake-up negative edge threshold voltage		0.4 V_{SREG}	0.45 V_{SREG}	0.5 V_{SREG}	V	A.159
V_{WU_THp}	Wake-up positive edge threshold voltage		0.5 V_{SREG}	0.55 V_{SREG}	0.65 V_{SREG}	V	A.160
V_{HYST}	Hysteresis		0.05 V_{SREG}	0.1 V_{SREG}	0.15 V_{SREG}	V	A.161
t_{wu_stat}	Static wake filter time	Tested by scan		64[(1)]		μs	A.162
I_{wu_stdby}	Input current in standby mode on EIx pins	V_{WU} < 1 V or V_{WU} > (V_S – 1.5 V)	2	30	60	μA	A.163
R_{wu_act}	Input resistor to Gnd in active mode and in standby mode during wake-up input sensing		80	160	300	kΩ	A.164
t_{wu_cyc}	Cyclic wake filter time	Tested by scan		16		μs	A.165

1. *Specified by design, not tested in production.*

2.4.22 CAN FD transceiver

ISO 11898-2:2016 compliant.

SAE J2284 compliant.

The voltages are referred to GND and currents are assumed positive when the current flows into the pin.

6 V < V_{SREG} < 18 V, 4.8 V < $V_{cansup.}$ < 5.2 V, T_J = -40°C to 150°C, unless otherwise specified.

-12 V ≤ (CANH + CANL)/2 ≤ 12 V.

Table 28. CAN communication operating range

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{SREG\_Transmitter}$	Supply voltage operating range for CAN transmitter(1)		5.5		18	V	E.001
$V_{SREG\_Receiver}$	Supply voltage operating range for CAN receiver		5		18	V	E.093
$V_{CANSUPlow}$	CAN supply low voltage flag	V_{V1} = V_{CANSUP} decreasing	3.9	4.2	4.5	V	E.002
$V_{CANHL,CM}$	Common mode bus voltage (VCANH + VCANL)/2	Measured with respect to the ground of each CAN transceiver	-12		12	V	E.003
I_{TRCV}	Transceiver current consumption during normal mode	Active mode: R_L = from 50 Ω to 65 Ω, C_{RXD} = 15 pF, 70% V_{RXDC} (rising) - 30% V_{RXDC} (falling), TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%), Test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width rectangular pulse signal T_{TXDC} = 6*TBIT(2), high pulse 1*TBIT, low pulse 5*TBIT			120	mA	E.094
I_{TRCV_short}	Transceiver current consumption during output short	R_L = 50 Ω to 65 Ω, V_{CANH} = -3 V or V_{CANL} = 40 V			120	mA	E.095
$I_{TRCVLPbias}$	Transceiver current consumption; biasing active	R_L = from 50 to 65 Ω, V_{TXDC} = $V_{TXDCHIGH}$,		400	600	μA	E.096
I_{TRCVLP}	Transceiver current consumption during low-power mode; biasing inactive	R_L = 50 Ω to 65 Ω, V_{TXDC} = $V_{TXDCHIGH}$			50	μA	E.097
BR	Supported bitrates	Supported bitrates at which all requirements are fulfilled			2	Mb/s	E.098

1. *At V_{SREG} < $V_{SREG\_Tranmitter(min)}$ the transceiver shall enter high impedance state.*
2. *The bit time T_{BIT} is the nominal bit time at a given bit rate (T_{BIT} = 1/BR). For example: at BR = 2 Mb/s => T_{BIT} = 500 ns.*

Table 29. CAN transmit data input: pin TXDC

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{TXDCLOW}$	Input voltage dominant level	Active mode	1.0	1.45	2.0	V	E.004
$V_{TXDCHIGH}$	Input voltage recessive level	Active mode	1.2	1.85	2.3	V	E.005
$V_{TXDCHYS}$	$V_{TXDCHIGH}$ - $V_{TXDCLOW}$	Active mode	0.2		0.7	V	E.006
R_{TXDCPU}	TXDC pull-up resistor	Active Mode	20	50	110	kΩ	E.007
$t_{d,TXDC(dom-rec)}$	TXDC - $CAN_{H,L}$ delay time dominant - recessive	R_L = from 50 Ω to 65 Ω, 70 % VTXD – 30% VDIFF, 5.5 V ≤ V_S ≤ 18 V, TXDC rise time = 10 ns (10% - 90%)		120		ns	E.008
$t_{d,TXDC(rec-diff)}$	TXDC - $CAN_{H,L}$ delay time recessive - dominant	R_L = from 50 Ω to 65 Ω, 30 % V_{TXD} – 70% V_{DIFF}, 5.5 V ≤ V_S ≤ 18 V, TXDC fall time = 10 ns (90% - 10%)		120		ns	E.009
$t_{dom(TXDC)}$	TXDC dominant time-out	Tested by scan	0.8	2	5	ms	E.010

Table 30. CAN receive data output: pin RXDC

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{RXDCLOW}$	Output voltage dominant level	Active mode, I_{RXDC} = 2 mA	0	0.2	0.5	V	E.011
$V_{RXDCHIGH}$	Output voltage recessive level	Active mode, I_{RXDC} = -2 mA	V1-0.5	V1-0.2	V1	V	E.012
$t_{r,RXDC}$ (1)	RXDC rise time	C_L = 15 pF, 30% - 70% V_{RXDC}	0		25	ns	E.013
$t_{f,RXDC}$(1)	RXDC fall time	C_L = 15 pF, 70% - 30% V_{RXDC}	0		25	ns	E.014
$t_{d,RXDC(dom-rec)}$(1)	$CAN_{H,L}$ – RXDC delay time dominant - recessive	C_L = 15 pF, 30% V_{DIFF} – 70% V_{RXDC}		120		ns	E.015
$t_{d,RXDC(rec - dom)}$(1)	$CAN_{H,L}$ – RXDC delay time recessive - dominant	C_L = 15 pF, 70% V_{DIFF} – 30% V_{RXDC}		120		ns	E.016

1. *Specified by design, not tested in production.*

Table 31. CAN transmitter dominant output characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{CANHdom}$	Single ended CANH voltage level in dominant state	V_{TXDC} = $V_{TXDCLOW}$, R_L = from 50 Ω to 65 Ω	2.75	3.5	4.5	V	E.017
$V_{CANLdom}$	Single ended CANL voltage level in dominant state	V_{TXDC} = $V_{TXDCLOW}$, R_L = from 50 Ω to 65 Ω	0.5	1.5	2.25	V	E.018
$V_{DIFF,dom}$	Differential output voltage in dominant state: $V_{CANHdom}$- $V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$, R_L = from 50 Ω to 65 Ω	1.5	2.0	3	V	E.019
V_{DIFF_Arb}	Differential output voltage in dominant state during arbitration: $V_{CANHdom}$-$V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$, R_L = 2240 Ω	1.5		5	V	E.099

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{DIFF,dom_ext}	Differential output voltage in dominant state on extended bus load range: $V_{CANHdom}$-$V_{CANLdom}$	V_{TXDC} = $V_{TXDCLOW}$, R_L = from 45 Ω to 70 Ω	1.4		3.3	V	E.100
$V_{DIFF,domVsLow}$	Differential output voltage in dominant state: $V_{CANHdom}$-$V_{CANLdom}$ at low VS	V_{TXDC} = $V_{TXDCLOW}$, R_L = from 50 Ω to 65 Ω, 5 V < V_S < 5.5 V (1)	1.35		3	V	E.101
V_{DIFF,dom_ext_VsLow}	Differential output voltage in dominant state: $V_{CANHdom}$-$V_{CANLdom}$ with 45 Ω to70 Ω load at low V_S	V_{TXDC} = $V_{TXDCLOW}$, R_L = from 45 Ω to 70 Ω, 5 V < V_S < 5.5 V (1)	1.25		3.3	V	E.102
V_{SYM}	Driver symmetry V_{SYM} = (V_{CANH} + V_{CANL})/ V_{CANSUP} V_{CANSUP} = 5 V (2)	R_L = 60 Ω ± 1%, f_{TXDC} = 1 MHz,(3) C_{SPLIT} = 4.7 nF (±5%)	0.9	1	1.1		E.020
$I_{OCANH,dom\ (-3V)}$	CANH output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$, V_{CANH} = from -3 V to 18 V	-115		115	mA	E.021
$I_{OCANL,dom\ (18V)}$	CANL output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$, V_{CANL} = from - 3 V to18 V	-115		115	mA	E.022
$I_{OCANH,dom\ (40V)}$	CANH output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$, V_{CANH} = 40 V, V_S = 40 V	0		15	mA	E.023
$I_{OCANL,dom\ (40V)}$	CANL output current in dominant state	V_{TXDC} = $V_{TXDCLOW}$, V_{CANL} = 40 V, V_S = 40 V	0		115	mA	E.024

1. *V_S at device pin after reverse battery protection, while application is supplied with 6 V. Operating condition has to be adapted, if a higher voltage drop occurs in the application.*
2. *If it is an external pin, it should be supplied externally.*
3. *Measurement equipment input load < 20 pF, > 1 MΩ, guaranteed by E.017, E.018, E.021, E.022, E.045, E.046 measurements.*

Table 32. CAN transmitter recessive output characteristics, CAN normal mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{CANHrec}$	CANH voltage level in recessive state (normal mode)	V_{TXDC} = $V_{TXDCHIGH}$, no load	2	2.5	3	V	E.025
$V_{CANLrec}$	CANL voltage level in recessive state (normal mode)	V_{TXDC} = $V_{TXDCHIGH}$, no load	2	2.5	3	V	E.026
$V_{DIFF,recOUT}$	Differential output voltage in recessive state (normal mode): $V_{CANHrec}$-$V_{CANLrec}$	V_{TXDC} = $V_{TXDCHIGH}$, no load	-50		50	mV	E.027

Note: CAN normal mode: tested in TRX ready state while the device is in active mode.

Table 33. CAN receiver input characteristics during CAN normal mode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{THdom}	Differential receiver threshold voltage recessive to dominant state	-12 V≤ V_{CANH} ≤12 V, 12 V≤ V_{CANL} ≤12 V	0.5		0.9	V	E.034
V_{dom_range}	Differential dominant input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	0.9		10	V	E.103
V_{THrec}	Differential receiver threshold voltage dominant to recessive state	12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	0.5		0.9	V	E.035
V_{rec_range}	Differential recessive input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	-5		0.5	V	E.104

Note: CAN normal mode: tested in TRX ready state while the device is in active mode.

Table 34. CAN receiver input characteristics during CAN low-power mode, biasing inactive

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{THdomLP}$	Differential receiver threshold voltage recessive to dominant state	12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	0.4		1.15	V	E.038
$V_{dom\_range\_LP}$	Differential dominant input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	1.15		10	V	E.105
$V_{THrecLP}$	Differential receiver threshold voltage dominant to recessive state	12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	0.4		1.15	V	E.039
$V_{rec\_range\_LP}$	Differential recessive input level voltage range	-12 V ≤ V_{CANH} ≤ 12 V, -12 V ≤ V_{CANL} ≤ 12 V	-5		0.4	V	E.106
$V_{CANHrecLP}$	CANH output voltage in recessive state		-0.1		0.1	V	E.120
$V_{CANLrecLP}$	CANL output voltage in recessive state		-0.1		0.1	V	E.121
$V_{DIFF,recOUTLP}$	Differential output voltage in recessive state: $V_{CANHrecLP}$-$V_{CANLrecLP}$		-0.2		0.2	V	E.122

Note: CAN low-power mode, biasing inactive: tested in CAN TRX STDBY (bias off) state while the device is in active mode, V1_Standby mode and VBAT_Standby mode.

Table 35. CAN receiver input resistance

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
R_{diff}	Differential internal resistance	V_{TXDC} = $V_{TXDCHIGH}$, No load R_{diff} = R_{CANH} + R_{CANL} -2 V ≤ V_{CANH} ≤ 7 V, -2 V ≤ V_{CANL} ≤ 7 V(1)	12		100	kΩ	E.040
$R_{CANH,\ CANL}$	Single ended internal resistance	V_{TXDC} = $V_{TXDCHIGH}$, No load -2 V ≤ V_{CANH} ≤ 7 V, -2 V ≤ V_{CANL} ≤ 7 V(1)	6		50	kΩ	E.041
m_R	Internal resistance matching $R_{CANH,CANL}$	Biasing active, V_{TXDC} = $V_{TXDCHIGH}$, no load, m_R = 2 x (R_{CAN_H} - R_{CAN_L}) / (R_{CAN_H} + R_{CAN_L}), 10 kΩ resistor between CANH-CANL pin with external 5 V	-0.03		0.03		E.042

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
C_{in}(2)	Internal capacitance			20	40	pF	E.043
$C_{in,diff}$(2)	Differential internal capacitance			10	20	pF	E.044

1. *Voltage range is taken from ISO CD 16845-2 (high speed medium access unit - conformance test plan).*
2. *Parameter specified by design, not tested in production.*

Note: CAN normal and low-power mode, biasing active: tested in CAN TRX normal and CAN TRX STDBY (bias on) state while the device is in active and V1_Standby mode.

Table 36. CAN transceiver delay

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$t_{LOOP,hl}$	Loop delay TXDC to RXDC (high to low)	5.5 V < V_S < 18 V, R_L = 60 Ω ±1%, C_L = 100 pF, C_{RXDC} = 15 pF, 30%V_{TXDC} - 30%V_{RXDC}, TXDC fall time = 10 ns (90% - 10%)			255	ns	E.045
$t_{LOOP,lh}$	Loop delay TXDC to RXDC (low to high)	5.5 V < V_S < 18 V, R_L = 60 Ω ±1%, C_L = 100 pF, C_{RXDC} = 15 pF, 70%V_{TXD} - 70%V_{RXD}, TXDC rise time = 10 ns (10% - 90%)			255	ns	E.046
$t_{LOOP150,hl}$	Loop delay TXDC to RXDC (high to low) with 150 Ω bus load	5.5 V < V_S < 18 V, R_L = 150 Ω, C_L = 100 pF, C_{RXDC} = 15 pF, 30%V_{TXDC} - 30%V_{RXDC}, TXDC fall time = 10 ns (90% - 10%)			350	ns	E.107
$t_{LOOP150,lh}$	Loop delay TXDC to RXDC (low to high) with 150 Ω bus load	5.5 V < V_S < 18 V, R_L = 150 Ω, C_L = 100 pF, C_{RXDC} = 15 pF, 70%V_{TXD} - 70%V_{RXD}, TXDC rise time = 10 ns (10% - 90%)			350	ns	E.108
$T_{Bit(RXD)}$ ≤ 1 Mb/s(1)	Recessive bit symmetry at RXDC	5.5 V < V_S < 18 V, R_L = 60 Ω ±1%, C_L = 100 pF, C_{RXD} = 15 pF, 70%V_{RXDC} (rising) - 30%V(falling), TXDC rise and fall time = 10 ns (10% - 90%, 90% - 10%), Test signal to be applied on the TXDC input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width. Rectangular pulse signal T_{TXDC} = 6000 ns, high pulse 1000 ns, low pulse 5000 ns	900	1000	1050	ns	E.047
$T_{Bit(RXD)\_150\ \Omega}$ ≤ 1 Mb/s		R_L = 150 Ω, other conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s, value may be obtained by characterization only.	800		1050		E.109
$T_{Bit(RXD)}$ ≤ 2 Mb/s		Conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s, Rectangular pulse signal T_{TXDC} = 3000 ns, high pulse 500 ns, low pulse 2500 ns	400	500	550		E.110
$T_{Bit(RXD)\_150\ \Omega}$ ≤ 2 Mb/s		R_L = 150 Ω, other conditions as $T_{Bit(RXD)}$ ≤ 1 Mb/s, value may be obtained by characterization only	300		550		E.111

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$T_{Bit(RXD)} \leq$ 5 Mb/s	Recessive bit symmetry at RXDC	Conditions as $T_{Bit(RXD)} \leq$ 1 Mb/s, Rectangular pulse signal T_{TXDC} = 1200 ns, high pulse 200 ns, low pulse 1000 ns	120	200	220	ns	E.112
$T_{Bit(BUS)} \leq$ 1 Mb/s	Recessive bit symmetry at CAN-Bus	5.5 V < V_S < 18 V, R_L = 60 Ω ±1%, C_L = 100 pF, C_{RXD} = 15 pF, V_{DIFF}: 0.5 V (falling) - 0.9 V (rising), TXD rise and fall time = 10 ns (10% - 90%, 90% - 10%), test signal to be applied on the TXD input of the implementation is a square wave signal with a positive duty cycle of 1/6 and a period of six times the nominal recessive bit width. Rectangular pulse signal T_{TXDC} = 6000 ns, high pulse 1000 ns, low pulse 5000 ns	935	1000	1030	ns	E.113
$T_{Bit(BUS)} \leq$ 2 Mb/s		Conditions as $T_{Bit(BUS)} \leq$ 1 Mb/s, Rectangular pulse signal T_{TXDC} = 3000 ns, high pulse 500 ns, low pulse 2500 ns	435	500	530		E.114
$T_{Bit(BUS)} \leq$ 5 Mb/s		Conditions as $T_{Bit(BUS)} \leq$ 1Mb/s, Rectangular pulse signal T_{TXDC} = 1200 ns, high pulse 200 ns, low pulse 1000 ns	155	200	210		E.115
$\Delta t_{REC} \leq$ 2 Mb/s	Receiver timing symmetry ($T_{Bit(RXD)}$ - $T_{Bit(BUS)}$)	5.5 V < V_S < 18 V, R_L = 60 Ω ±1%, C_L = 100 pF, C_{RXD} = 15 pF, Rectangular pulse signal T_{TXDC} = 3000 ns, high pulse 500 ns, low pulse 2500 ns	-65		40	ns	E.116
$\Delta t_{REC} \leq$ 5 Mb/s		5.5 V < V_S < 18 V, R_L = 60 Ω ±1%, C_L = 100 pF, C_{RXD} = 15 pF, Rectangular pulse signal T_{TXDC} = 1200 ns, high pulse 200 ns, low pulse 1000 ns	-45		15		E.117
t_{CAN}(2)	CAN permanent dominant time out	Tested by scan		700		µs	E.118
t_{WUP}-V_{Cansup}	Time between WUP(3) on the CAN bus until V_{Cansup} goes active	Wake-up pattern wake-up 70% V_{DIFF} – 90% $V_{Cansup(min)}$,	0		200	µs	E.049
$t_{WUP-RXD}$	Time between WUP(3) on the CAN bus until RXD is active (the CAN signal is represented at the RXD output)	Wake-up pattern wake-up RXD output enabled	0		1	ms	E.119
$t_{VCANSUPlow}$	Filter time needed to display CANSUPlow flag	Tested by SCAN		5		µs	E.124

1. *$T_{Bit(RXD)}$ for the highest supported data rate has to be specified (1 Mb/s, 2 Mb/s, 5 Mb/s).*
2. *At the expiration of this filter time a flag is set.*
3. *Time starts with the end of last dominant phase of the WUP.*

Table 37. CAN receiver input current

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$I_{Leakage, CANH}$	Input leakage current CANH	Unpowered device, V_{CANH} = 5 V, V_{CANL} = 5 V, V_S < V_{POR_F}(1), V_S, V_{CANSUP}(2) connected via 0 Ω to GND, V_S, V_{CANSUP} (2) connected via 47 kΩ to GND, T_J = -40 to 130 °C	-5		5	µA	E.050
$I_{Leakage, CANL}$	Input leakage current CANL	Unpowered device, V_{CANH} = 5 V, V_{CANL} = 5 V, V_S < V_{POR_F}(1), V_S, V_{CANSUP} (3) connected via 0 Ω to GND, V_S, V_{CANSUP} (3) connected via 47 kΩ to GND, T_J = -40 to 130 °C	-5		5	µA	E.052

1. *Vs not floating.*
2. *Related to the external supply pin of the CAN-transceiver. If the transceiver supply is generated entirely inside the device the parameter is measured with respect to the supply of the device.*
3. *Related to the external supply pin of the CAN-transceiver. If the transceiver supply is generated entirely inside the device the parameter is measured with respect to the supply of the device; if the transceiver is supplied by its own supply pin, this pin has to fulfill this specification as well as the supply that is used to generate the transceiver voltage in case it is on the same device.*

Note: The leakage currents have to be measured with the supply of the CAN-transceiver connected to ground either directly or via 47 kΩ. If the CAN-transceiver supply is generated by the device from V_S, V_S has to be connected to ground. If the CAN-transceiver is supplied by another device, the supply of the CAN-transceiver has to be connected to ground.

Table 38. Biasing control timings

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{filter}	CAN activity filter time		0.5		1.8	µs	E.054
t_{wake}	Wake-up time out	Tested by scan	0.8	1	5	ms	E.055
$t_{Silence}$	CAN timeout	Tested by scan	600	700	1200	ms	E.056
T_{Bias}	CAN bias reaction time				250	µs	E.123

2.4.23 LIN transceiver

LIN ISO 17987-4:2016 compliant for data rates up to 20 kBit/s

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

6 V < V_{SREG} < 18 V, T_J = -40 °C to 150 °C unless otherwise specified.

Table 39. LIN transmit data input: pin TXD

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{TXDLOW}	Input voltage dominant level	Active mode	1.0	1.45		V	E.058
$V_{TXDHIGH}$	Input voltage recessive level	Active mode		1.85	2.3	V	E.059
V_{TXDHYS}	$V_{TXDHIGH}$ - V_{TXDLOW}	Active mode	0.2	0.4		V	E.060
R_{TXDPU}	TXD pull-up resistor	Active mode	13	29	49	kΩ	E.061

Table 40. **LIN receive data output: pin RXD**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{RXDLOW}	Output voltage dominant level	Active mode		0.2	0.5	V	E.062
$V_{RXDHIGH}$	Output voltage recessive level	Active mode	V1-0.5	V1-0.2		V	E.063

Table 41. **LIN transmitter and receiver: pin LIN**

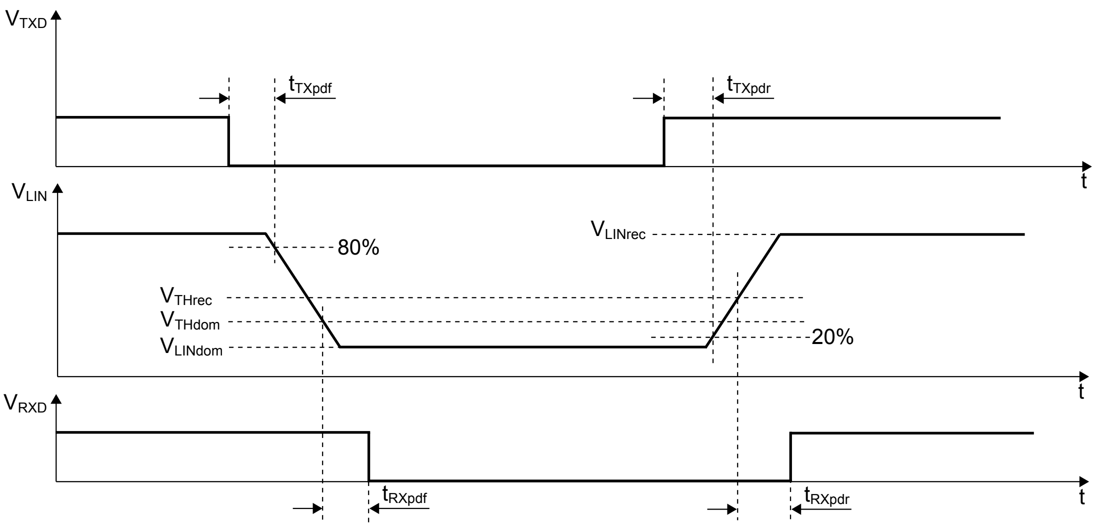
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{THdom}	Receiver threshold voltage recessive to dominant state		0.4* V_{SREG}	0.45* V_{SREG}	0.5* V_{SREG}	V	E.064
V_{Busdom}	Receiver dominant state				0.4* V_{SREG}	V	E.065
V_{THrec}	Receiver threshold voltage dominant to recessive state		0.5* V_{SREG}	0.55* V_{SREG}	0.6* V_{SREG}	V	E.066
V_{Busrec}	Receiver recessive state		0.6* V_{SREG}			V	E.067
V_{THhys}	Receiver threshold hysteresis: VTHrec -VTHdom		0.07* V_{SREG}	0.1* V_{SREG}	0.175* V_{SREG}	V	E.068
V_{THcnt}	Receiver tolerance center value: (VTHrec +VTHdom)/2		0.475* V_{SREG}	0.5* V_{SREG}	0.525* V_{SREG}	V	E.069
V_{THwkup}	Receiver wakeup threshold activation voltage (rising edge)		0.5* V_{SREG}	0.55* V_{SREG}	0.6* V_{SREG}	V	E.070
$V_{THwkdwn}$	Receiver wakeup threshold activation voltage (falling edge)		0.4* V_{SREG}	0.45* V_{SREG}	0.5* V_{SREG}	V	E.071
t_{linbus}	LIN bus wake-up dominant filter time	Sleep mode; Edge: rec-dom; Tested by scan		64		µs	E.072
t_{dom_LIN}	LIN bus wake-up dominant filter time	Sleep mode; Edge: rec-dom-rec; Tested by scan	28			µs	E.073
$I_{LINDomSC}$	Transmitter input current limit in dominant state	$V_{TXD} = V_{TXDLOW}$; $V_{LIN} = V_{BAT} = 18$ V	40	100	180	mA	E.074
$I_{bus\_PAS\_dom}$	Input leakage current at the receiver incl. pull-up resistor	$V_{TXD} = V_{TXDHIGH}$; $V_{LIN} = 0$ V; $V_{BAT} = 12$ V(1)	-1			mA	E.075
$I_{bus\_PAS\_rec}$	Transmitter input current in recessive state	In standby modes; $V_{TXD} = V_{TXDHIGH}$; $V_{LIN} > 8$ V; $V_{BAT} < 18$ V; $V_{LIN} \geq V_{BAT}$			20	µA	E.076
$I_{bus\_NO\_GND}$	Input current if loss of GND at Device	GND = V_S; 0 V < V_{LIN} < 18 V; $V_{BAT} = 12$ V	-1		1	mA	E.077
I_{bus}	Input current if loss of VBAT at Device	GND = V_S; 0 V < V_{LIN} < 18 V			30	µA	E.078
V_{LINdom}	LIN voltage level in dominant state	Active mode ; $V_{TXD} = V_{TXDLOW}$; $R_{bus} = 500\ \Omega$			1.2	V	E.080
V_{LINrec}	LIN voltage level in recessive state	Active mode; $V_{TXD} = V_{TXDHIGH}$; $I_{LIN} = 10$ µA	0.8* V_{SREG}			V	E.081
R_{LINup}	LIN output pull-up resistor	$V_{LIN} = 0$ V	20	40	60	kΩ	E.082
C_{LIN}(2)	LIN input capacitance				30	pF	E.083

1. *Slave mode.*
2. *Specified by design, not tested in production.*

Table 42. LIN transceiver timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{RXpd}	Receiver propagation delay time	t_{RXpd} = max(t_{RXpdr},t_{RXpdf}); t_{RXpdf} = t(0.5 V_{RXD}) -t(0.45 V_{LIN}); t_{RXpdr} = t(0.5 V_{RXD}) -t(0.55 V_{LIN}); V_S = 12 V; C_{RXD} = 20 pF; R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			6	µs	E.084
t_{RXpd_sym}	Symmetry of receiver propagation delay time (rising vs. falling edge)	t_{RXpd_sym} = t_{RXpdr}-t_{RXpdf}; V_S = 12 V; R_{bus} = 1 kΩ, C_{bus} = 1 nF ; C_{RXD} = 20 pF	-2		2	µs	E.085
D1	Duty cycle 1	$T_{HRec(max)}$ = 0.744*V_S; $T_{HDom(max)}$ = 0.581*V_S; V_S = from 7 V to 18 V, t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$ / (2xtbit); R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF	0.396				E.086
D2	Duty cycle 2	$T_{HRec(min)}$ = 0.422*V_S; $T_{HDom(min)}$ = 0.284*V_S; V_S = from 7.6 V to 18 V, t_{bit} = 50 µs; D2 = $t_{bus\_rec(max)}$ /(2xtbit); R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			0.581		E.087
D3	Duty cycle 3	$T_{HRec(max)}$ = 0.778*V_S; $T_{HDom(max)}$ = 0.616*V_S; V_S = from 7 V to 18 V, t_{bit} = 96 µs; D3 = $t_{bus\_rec(min)}$ /(2xtbit); R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF	0.417				E.088
D4	Duty cycle 4	$T_{HRec(min)}$ = 0.389*V_S; $T_{HDom(min)}$ = 0.251*V_S; V_S = from 7.6 V to 18 V, t_{bit} = 96 µs; D4 = $t_{bus\_rec(max)}$ /(2xtbit); R_{bus} = 1 kΩ, C_{bus} = 1 nF; R_{bus} = 660 Ω, C_{bus} = 6.8 nF; R_{bus} = 500 Ω, C_{bus} = 10 nF			0.590		E.089
$t_{dom(TXDL)}$	TXDL dominant time out	Tested by scan		12		ms	E.090
t_{LIN}	LIN permanent recessive time out	Tested by scan		40		µs	E.091
$T_{dom(bus)}$	LIN bus permanent dominant time-out	Tested by scan		12		ms	E.092

Figure 8. **LIN transmit, receive timing**



2.4.24 SPI

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
6 V < V_{SREG} < 18 V, all outputs open, T_J = -40 °C to 150 °C, unless otherwise specified.

Table 43. **Input: CSN**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{CSNLOW}	Input voltage low level	Normal mode, V1 = 5 V	1.0	1.45		V	B.001
$V_{CSNHIGH}$	Input voltage high level	Normal mode, V1 = 5 V		1.85	2.3	V	B.002
V_{CSNHYS}	$V_{CSNHIGH}$ - V_{CSNLOW}	Normal mode, V1 = 5 V	0.2	0.4		V	B.003
I_{CSNPU}	CSN pull-up resistor	Normal mode, V1 = 5 V	13	29	46	kΩ	B.004

Table 44. **Inputs: CLK, DI**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{set} (1)	Delay time from V1_Standby to active mode	Switching from V1_Standby to active mode using SPI wake-up access. Time until output drivers (P-channel) are enabled after CSN going to high. (First SPI wake-up access include the enable of the driver)		60		µs	B.005
		Switching from V1_Standby to active mode using SPI wake-up access. Time until output drivers (N-channel) are enabled after CSN going to high.		600		µs	B.006
$V_{in\ L}$	Input low level	V1 = 5 V	1.0	1.45		V	B.007
$V_{in\ H}$	Input high level	V1 = 5 V		1.8	2.3	V	B.008
$V_{in\ Hyst}$	Input hysteresis	V1 = 5 V	0.2	0.4		V	B.009
I_{in}	Pull-down current at input	V_{in} = 1 V	5	30	60	µA	B.010
C_{in} (1)	Input capacitance at input CSN, CLK, DI, PWM1-6 and PWM4-5	0 V < V1 < 5.3 V		10	15	pF	B.011
f_{CLK}	SPI input frequency at CLK				4	MHz	B.012

1. *Parameter specified by design, not tested in production.*

Table 45. DI, CLK and CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{CLK}	Clock period	V1 = 5 V	250			ns	B.013
t_{CLKH}	Clock high time	V1 = 5 V	106.25			ns	B.014
t_{CLKL}	Clock low time	V1 = 5 V	106.25			ns	B.015
$t_{set\ CSN}$	CSN setup time, CSN low before rising edge of CLK	V1 = 5 V	150			ns	B.016
$t_{set\ CLK}$	CLK setup time, CLK high before rising edge of CSN	V1 = 5 V	150			ns	B.017
$t_{set\ DI}$	DI setup time	V1 = 5 V	25			ns	B.018
$t_{hold\ DI}$	DI hold time	V1 = 5 V	25			ns	B.019
$t_{r\ in}$(1)	Rise time of input signal DI, CLK, CSN	V1 = 5 V			25	ns	B.020
$t_{f\ in}$(1)	Fall time of input signal DI, CLK, CSN	V1 = 5 V			25	ns	B.021

1. *Parameter specified by design, not tested in production.*

See also Figure 10. SPI input timing.

Table 46. Output DO

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{DOL}	Output low level	V1 = 5 V, I_{DO} = -4mA			0.5	V	B.022
V_{DOH}	Output high level	V1 = 5 V, I_{DO} = 4 mA	V1-0.5			V	B.023
I_{DOLK}	Tristate leakage current	V_{CSN} = V1, 0 V < V_{DO} < V1	-10		10	µA	B.024
C_{DO}(1)	Tristate input capacitance	V_{CSN} = V1, 0 V < V1 < 5.3 V		10	15	pF	B.025

1. *Parameter specified by design, not tested in production.*

Table 47. DO timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$t_{r\ DO}$(1)	DO rise time	C_L = 50 pF, I_{load} = -1 mA from 0.3 V1 to 0.7 V1			25	ns	B.026
$t_{f\ DO}$(1)	DO fall time	C_L = 50 pF, I_{load} = 1 mA from 0.3 V1 to 0.7 V1			25	ns	B.027
$t_{en\ DO\ tri\ L}$(1)	DO enable time from tristate to low level	C_L = 50 pF, I_{load} = 1 mA pull-up load to V1		50	100	ns	B.028
$t_{dis\ DO\ L\ tri}$(1)	DO disable time from low level to 3-state	C_L = 50 pF, I_{load} = 4 mA pull-up load to V1		50	100	ns	B.029
$t_{en\ DO\ tri\ H}$(1)	DO enable time from tristate to high level	C_L = 50 pF, I_{load} = -1 mA pull-down load to GND		50	100	ns	B.030
$t_{d\ DO}$(1)	DO delay time	V_{DO} < 0.3 V1 or V_{DO} > 0.7 V1, C_L = 50 pF		30	60	ns	B.032

1. *Parameter is specified by design, not tested in production.*

See Figure 11. SPI output timing.

Table 48. CSN timing

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$t_{CSN\_HI,min}$ (1)	Minimum CSN HI time, active mode	Transfer of SPI-command to Input register	0.5			μs	B.033
$t_{CSNfail}$ (1)	CSN low timeout	Tested by scan	20	35	50	ms	B.034

1. *Parameter is specified by design, not tested in production.*

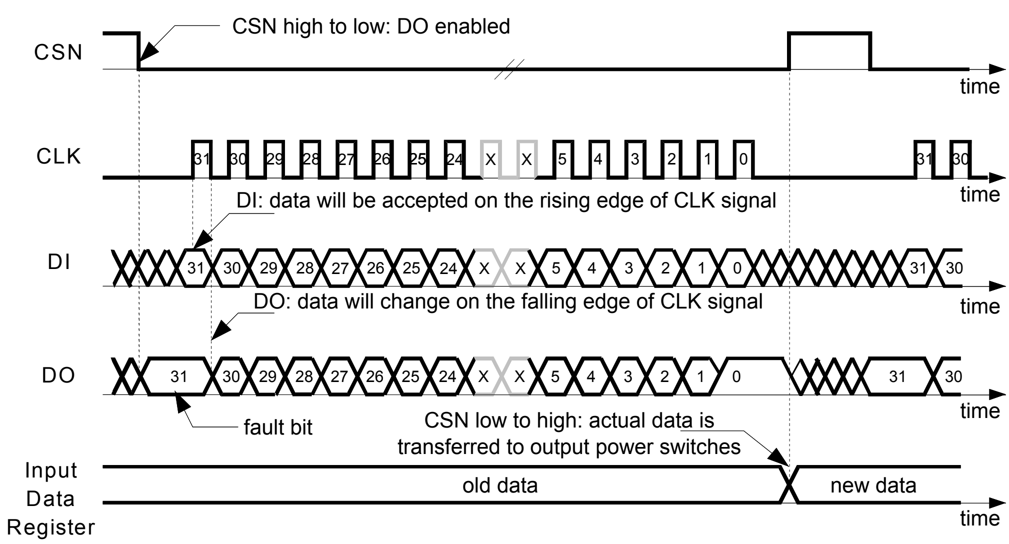


Figure 9. SPI transfer timing diagram

The SPI can be driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

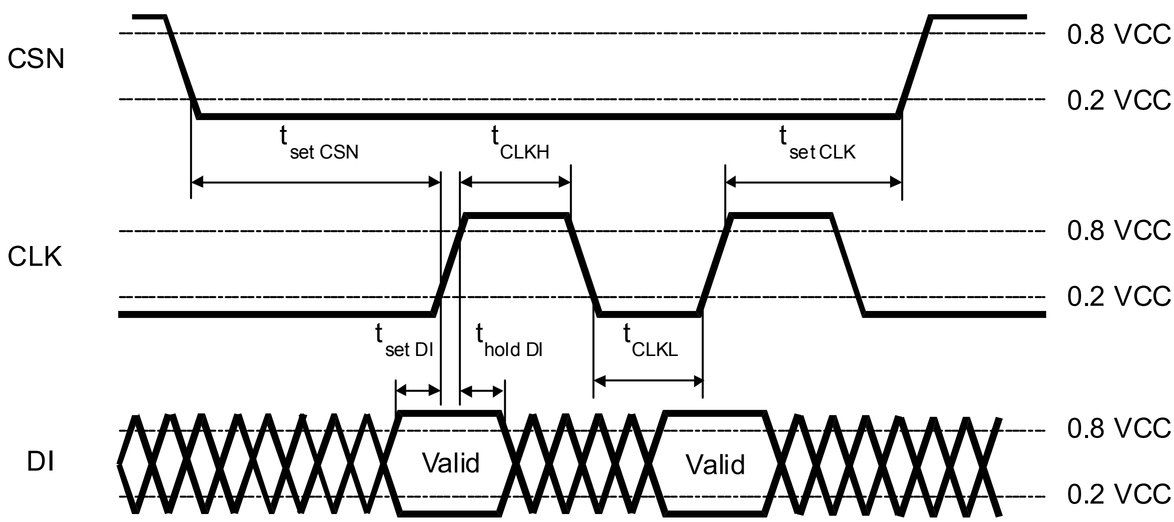


Figure 10. SPI input timing

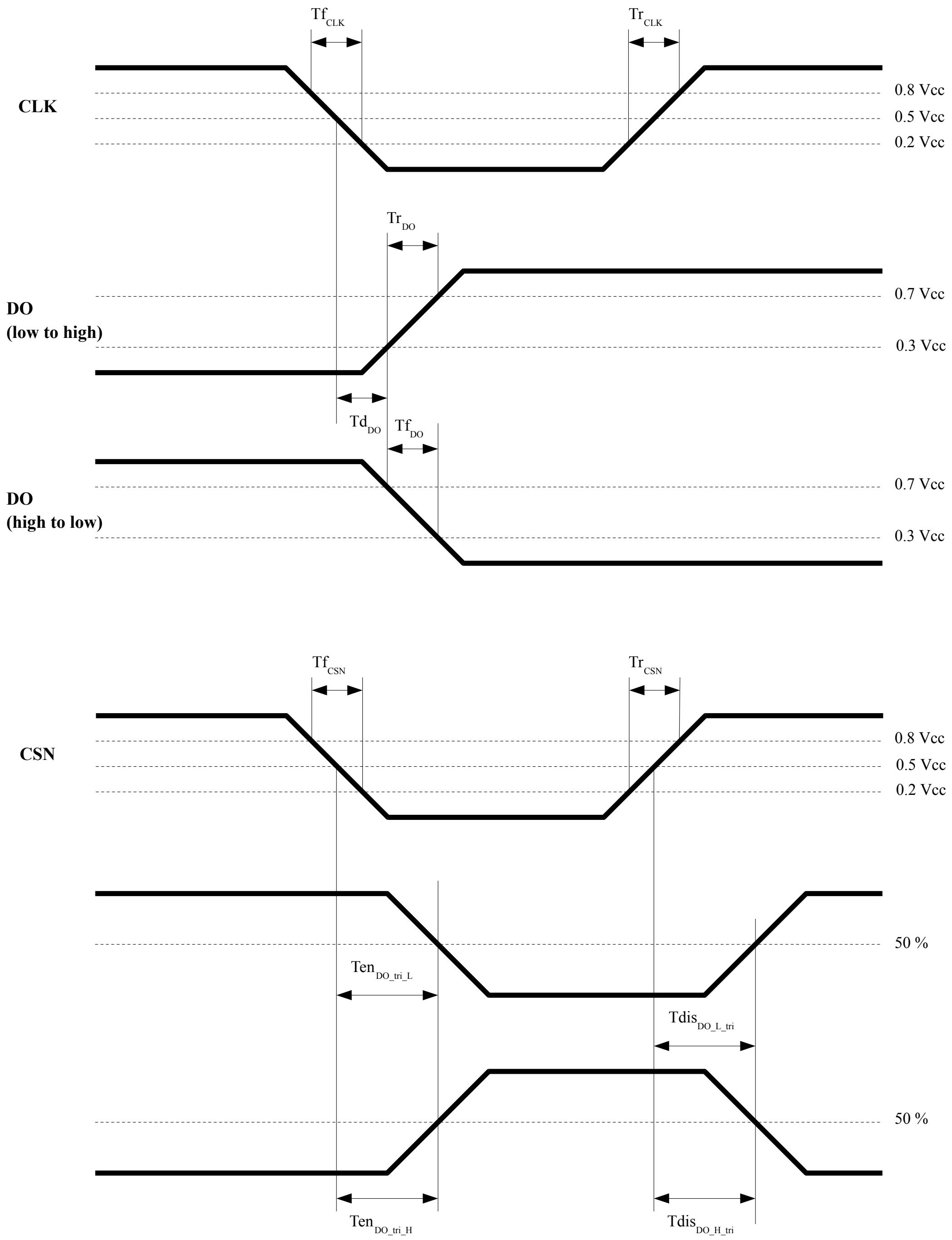


Figure 11. SPI output timing

Figure 12. **SPI CSN output timing**

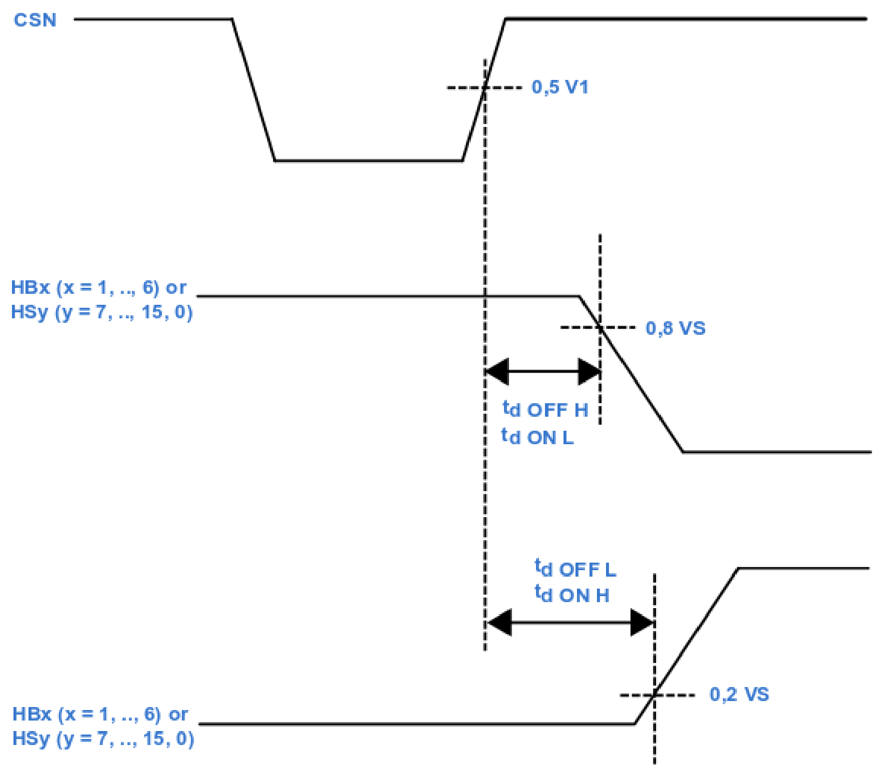
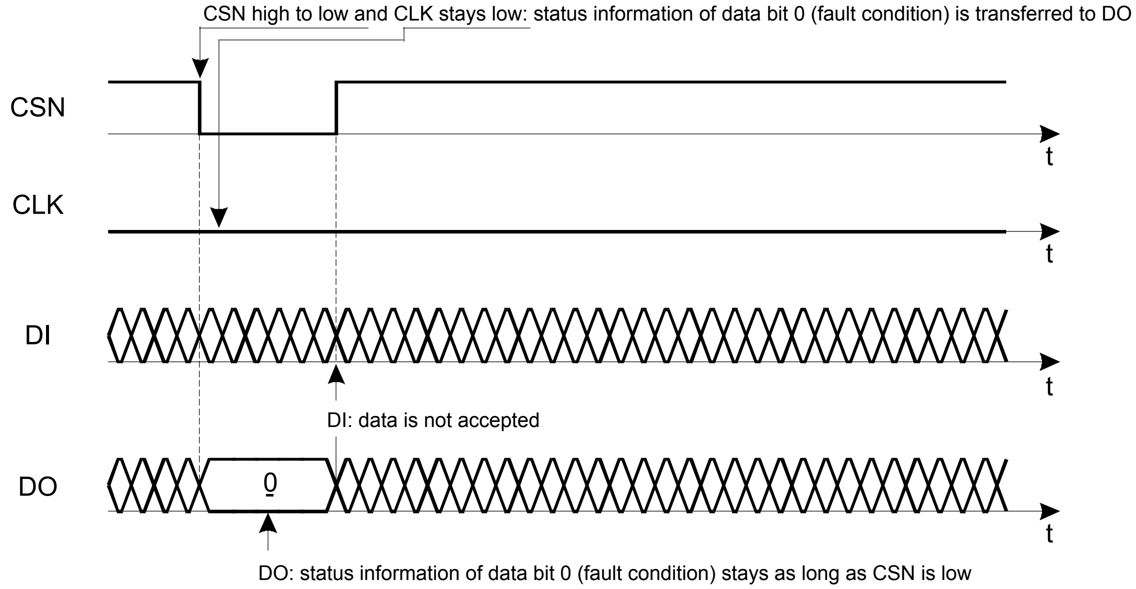


Figure 13. **SPI - CSN low to high transition and global status bit access**



2.4.25 Inputs DIRH, PWMH, PWM4-5, PWM1-6, PWM20, PWM21, DIR1, DIR2

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{SREG} ≤ 18 V, T_J = -40°C to 150°C.

Table 49. **Inputs: DIRH, PWMH, PWM4-5, PWM1-6, 6, PWM20, PWM21, DIR1, DIR2**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{IL}	Input voltage low level	V_{SREG} = 13.5 V	1	1.45		V	A.169
V_{IH}	Input voltage high level	V_{SREG} = 13.5 V		1.8	2.5	V	A.170
V_{IHYS}	Input hysteresis	V_{SREG} = 13.5 V	0.1	0.4		V	A.171
I_{in}	Input pull-down current on PWM1-6 and PWM4-5 pins	V_{SREG} = 13.5 V	2	30	60	μA	A.172

2.4.26 Debug input pin

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{SREG} ≤ 18 V, T_J = -40°C to 150°C.

Table 50. **Debug input**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{diL}	Input voltage low level	V_{SREG} = 13.5 V	6.1	7.4	8.4	V	A.187
V_{diH}	Input voltage high level	V_{SREG} = 13.5 V	7.4	8.4	9.4	V	A.188
V_{diHYS}	Input hysteresis	V_{SREG} = 13.5 V	0.25	1	1.4	V	A.189
R_{in}	Pull-down resistor	V_{DEBUG} = 6 V to 28 V	13	29	45	kΩ	A.190

2.4.27 Interrupt output

The voltages are referred to ground, and currents are assumed positive, when the current flows into the pin.
6 V ≤ V_{SREG} ≤ 18 V, T_J = -40 °C to 150 °C.

Table 51. **Interrupt output**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
V_{INTL}	output low level	V1 = 5 V, I_{INT} = -4 mA		0.2	0.5	V	A.176
V_{INTH}	output high level	V1 = 5 V, I_{INT} = 4 mA	V1-0.5	V1-0.2		V	A.177
I_{INTLK}	Tristate leakage current	0 V < V_{INT} < V1	-10		10	μA	A.178
$t_{Interrupt}$	Interrupt pulse duration (RXDL/NINT)	Tested by scan	42	56	70	μs	A.179
t_{Int_react}	Interrupt reaction time	Tested by scan			40	μs	A.180

2.4.28 Timer1 and Timer2

6 V ≤ V_{SREG} ≤ 18 V, T_J = -40°C to 150°C.

Table 52. Timer 1 and timer 2 values

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
ton1	Timer on time	Tested by scan	-	0.1	-	ms	F.012
ton2	Timer on time	Tested by scan	-	0.3	-	ms	F.013
ton3	Timer on time	Tested by scan	-	1	-	ms	F.014
ton4	Timer on time	Tested by scan	-	10	-	ms	F.015
ton5	Timer on time	Tested by scan	-	20	-	ms	F.016
T1	Timer period	Tested by scan	-	10	-	ms	F.017
T2	Timer period	Tested by scan	-	20	-	ms	F.018
T3	Timer period	Tested by scan	-	50	-	ms	F.019
T4	Timer period	Tested by scan	-	100	-	ms	F.020
T5	Timer period	Tested by scan	-	200	-	ms	F.021
T6	Timer period	Tested by scan	-	500	-	ms	F.022
T7	Timer period	Tested by scan	-	1000	-	ms	F.023
T8	Timer period	Tested by scan	-	2000	-	ms	F.024

2.4.29 SGND loss comparator

T_J = -40 °C to 150 °C, unless otherwise specified.

Table 53. SGND loss comparator

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
$V_{SGNDloss}$	Input voltage low level	V_{SREG} = 13.5 V	200	400	550	mV	A.181
$t_{SGNDloss}$	Filter time	Tested by scan		7		µs	A.182

3 Functional description

3.1 Supply VS, VSREG

VSREG supplies voltage regulators V1 and V2, all internal regulated voltages for analog and digital functionality, LIN, CAN, the EC control block and two of P-channel high-side switches (HS15 and HS0).

All other high-sides and the charge pump are supplied by VS. In case of VSREG pin disconnected, all power devices connected to VS are automatically switched off.

Filtering capacitors on VS and VSREG lines must be dimensioned to ensure transient slopes < 100 mV/µs.

3.2 Voltage regulators

The L99DZ380 contains two fully protected low drop voltage regulators, which are designed for very fast transient response and do not require electrolytic output capacitors for stability.

3.2.1 Voltage regulator V1

The V1 voltage regulator provides 5 V supply voltage and up to 250 mA continuous load current to supply the system microcontroller and the integrated CAN transceiver. The V1 regulator is embedded in the power management and fail-safe functionality of the device and operates according to the selected operating mode. The V1 voltage regulator is supplied by pin V_{SREG}.

In addition, the V1 regulator supplies the device internal loads. The voltage regulator is protected against overload and overtemperature. An external reverse current protection has to be provided by the application circuitry to prevent the input capacitor from being discharged by negative transients or low input voltage. Current limitation of the regulator ensures fast charge of external bypass capacitors. The output voltage is stable for ceramic load capacitors ≥ 1 µF.

In case the device temperature exceeds the TSD1 threshold the V1 regulator remains on. Hence, the microcontroller has the possibility for interaction or error logging. If the chip temperature exceeds TSD2 threshold (TSD2 > TSD1), V1 is deactivated and all wake-up sources (CAN, LIN1, LIN2, EI1, EI2, EI3, .., EI9 and timer) are disabled. After t_{TSD}, the voltage regulator restarts automatically. If the restart fails 7 times within one minute the L99DZ380 enters the forced VBAT-standby mode. The status bit Forced_Sleep_TSD2_V1SC is set.

3.2.2 Voltage regulator V2

The voltage regulator V2 is supplied by pin VSREG and can supply additional 5 V loads such as sensors or potentiometers.

V2 is a tracker of the V1 voltage regulator.

Voltage Regulator V2 is tracker of V1 regulator. i.e. provides a 5V output that tracks the V1 regulator output voltage with ΔVo (C.038) accuracy

Load current of V2 can be up to 50 mA.

The V2 regulator is protected against:

- overload
- overtemperature
- short-circuit (short to ground and battery supply voltage)
- reverse biasing

3.2.3 Voltage regulator failure

The V1 and V2 regulator output voltages are monitored.

In case of a drop below the V1, V2 fail thresholds ($V1,2 < V1,2_{fail}$, for $t > t_{V1,2fail}$), the failure bits V1FAIL, V2FAIL (SR7) are latched. The fail bits can be cleared by a dedicated SPI command.

3.2.4 Short to ground detection

At turn on of the V1 and V2 regulators, a short to GND condition is detected by monitoring the regulator output voltage.

If V1 (V2) is below the V_{1fail} (V_{2fail}) threshold for t > $t_{V1short}$ (t > $t_{V2short}$) after turn on, the L99DZ380 identifies a short-circuit condition at the related regulator output and the regulator is switched off.

In the case of V1 short to GND, the device enters VBAT-standby mode automatically.

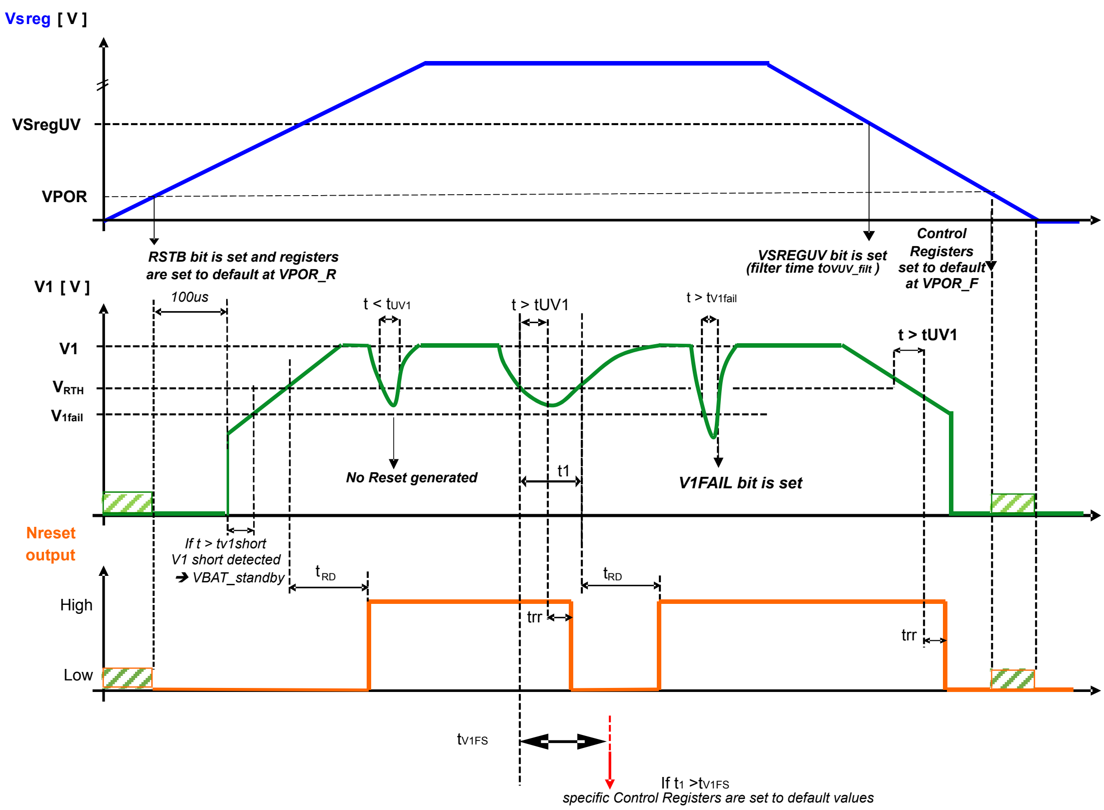
Bits FORCED_SLEEP_TSD2_V1SC (SR8) and V1FAIL (SR7) are set.

In the case of a V2 short to GND failure, the V2SC (SR7) and V1FAIL (SR7) bits are set.

Once the output voltage of the corresponding regulator V1 (V2) has exceeded the V_{1fail} (V_{2fail}) threshold, the short to ground detection is disabled. In case of a short to ground condition, the regulator is switched off due to thermal shutdown. V1 is switched off at TSD2, V2 is switched off at TSD1.

3.2.5 Voltage regulator behavior

Figure 14. Voltage regulator behavior and diagnosis during supply voltage ramp-up/ramp-down conditions



High Z Grounded

VSregUV:	Vsreg under-voltage
VPOR_R/F:	Vsreg power-on reset voltage (rising/falling)
V_{RTx}:	V1 reset threshold voltage
V1FAIL:	V1 fail threshold voltage

tUV1:	V1 under-voltage filter time
tV1fail:	V1 fail filter time
trr:	reset pulse reaction time
t_{RD}	reset pulse duration
tV1short:	V1 short filter time
tV1FS:	V1 fail safe filter time
tOVUV_filt:	Vsreg over-/undervoltage filter time

3.3 Operating modes

L99DZ380 can be operated in 4 different operating modes:

- Active
- Debug
- V1_Standby
- VBAT_Standby

3.3.1 Active mode

All functions are available, and the device is controlled by SPI.

3.3.2 Debug mode

To allow software debugging, the watchdog can be deactivated by applying an external voltage to the DEBUG input pin ($V_{debug} > V_{diH}$).

In debug mode, all device functionality is available, including CAN, which is enabled by default. The watchdog is deactivated.

At exit from debug mode ($V_{debug} < V_{diL}$) the watchdog starts with a long open window.

3.3.3 V1_Standby mode

The transition from active mode to V1_Standby mode is controlled by SPI.

To supply the microcontroller in a low-power mode, the V1 voltage regulator remains active.

After the V1 standby command (CSN low to high transition), the device enters V1_Standby mode immediately and the watchdog starts a long open window (t_{LW}). The watchdog is deactivated as soon as the V1 load current drops below the I_{cmp} threshold (Iv1 < I_{cmp}).

The V1 load current monitoring can be deactivated by setting ICMP = 1. In this configuration, the watchdog is deactivated upon transition into V1_Standby mode without monitoring the V1 load current.

Writing ICMP (CR2) = 1 is only possible with the first SPI command after setting ICMP_CONFIG_EN (CR1) = 1. The ICMP_CONFIG_EN bit is reset to ‘0’ automatically with the next SPI command.

Power outputs (except HS15 & HS0), as well as the LIN and CAN transmitters are switched off in V1_Standby mode.

HS15 and HS0 remain in the configuration programmed before the standby command in order to enable (cyclic) supply of external contacts.

Note: Before going to V1_Standby mode, the OL_H1L2, OL_H2L1 and GH_OL_EN bits in control register 12 must be set to 0 to achieve the specified current consumption.

3.3.4 Interrupt

The interrupt signal (linked to RXDL/NINT internally) indicates a wake-up event from V1_Standby mode. This is the only mode in which the pin is configured as NINT, otherwise it works as RXDL. In case of a wake-up by wake-up inputs, valid wake-up frames on LIN or CAN, (activity on LIN or CAN), SPI access or timer interrupt, the NINT pin is pulled low for 56 μs, after a reaction time t_{Int_react} from the related wake-up event.

In case of increasing V1 load current during V1_Standby mode ($I_{V1} > I_{cmp}$), the device remains in standby mode and the watchdog starts with a long open window. No interrupt signal is generated.

3.3.5 VBAT_Standby mode

The transition from active mode to VBAT_Standby mode is initiated by an SPI command.

In VBAT_Standby mode, the voltage regulators V1 and V2, the power outputs (except HS15 and HS0) as well as LIN and CAN transmitters are switched off. An NReset pulse is generated upon wake-up from VBAT_Standby mode.

Note: Before going to VBAT_Standby mode, the OL_H1L2, OL_H2L1 and GH_OL_EN bits in control register 12 must be set to 0 to achieve the specified current consumption.

3.4 Wake-up from standby modes

A wake-up from standby mode switches the device to active mode. This can be initiated by one or more of the following events:

Table 54. **Wake-up sources**

Wake-up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI
Level change of EI	Can be configured or disabled by SPI
$I_{V1} > I_{cmp}$	Device remains in V1_Standby mode but watchdog is enabled (if ICMP = 0). No interrupt is generated.
Timer interrupt / Wake-up of microcontroller by TIMER	Programmable by SPI: - V1_Standby mode: device wakes up and interrupt signal is generated at RXDL/NINT when programmable time-out has elapsed - VBAT_Standby mode: device wakes up after programmable timer expiration. V1 regulator is turned on and NReset signal is generated when programmable time-out has elapsed
SPI access	Always active (except in VBAT_Standby mode) Wake-up event: CSN falling edge

To prevent the system from a deadlock condition (no wake-up from standby possible) a configuration where the wake-up by LIN and HS CAN are both disabled, is not allowed. All wake-up sources are configured to default values in case of such invalid setting. The SPI error bit (SPIE) in the global status register is set.

3.4.1 External interrupts

L99DZ380 has 9 external interrupts EIx (x = 1, 2, ... , 9) that can be used as wake-up sources. Each external interrupt input is sensitive to any level transition (positive and negative edge) and can be configured for static or cyclic monitoring of the input voltage level by the suitable setting of the EIx_FILT_0 and EIx_FILT_1 bits (x = 1, 2, ... , 9) which allows to choose the monitoring among static, cyclic with timer1 or cyclic with timer2.

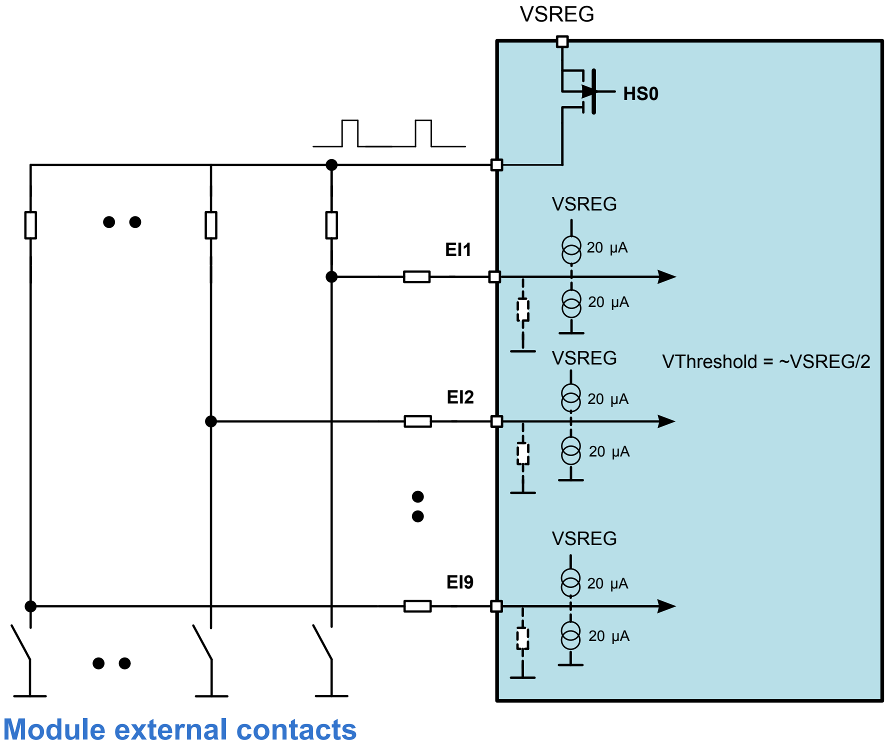
When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.

For static contact monitoring, a filter time of t_{wu_stat} is implemented. The filter is started when the input voltage passes the specified threshold V_{wu_th}. External interrupt status bit is set only if this threshold is passed for more than t_{wu_stat} (EI1_STATE and EI2_STATE in SR4; EIy_STATE with y=3,.. , 9 in SR3).

Cyclic contact monitoring allows instead the periodical (not threshold dependent) activation of the external interrupt input to read the status of the external contact. The periodical activations are driven by timer1 or timer2 whose settings (on time and period) can be configured through CR17 (8...13) and (16...21) bits. The input signal is filtered with a filter time of t_{WU_cyc} after a delay (80% of the configured timer on time). An external interrupt is processed if the status has changed versus the previous cycle, therefore the external interrupt status bit (SR3 and SR4) is set only if the status during the consecutive on time is different, after configuring the delay and t_{WU_cyc}.

The buffered output HS0 can be used to supply the external contacts with the timer setting according to the cyclic monitoring of the external interrupt input.

Figure 15. Cyclic monitoring: the external contacts are supplied periodically by the internal timer



In standby mode, the inputs are configurable with an internal pull-up or pull-down current source according to the setup of the external contact. Moreover, in the case of cyclic sensing, an internal pull-down resistor (R_{WU_act}) is periodically activated on each rising edge of the TIMER_ON.

R_{WU_act} is activated also for static wakeup, but in this case it occurs just after the external interrupt request, keeping this condition for at least the filter time t_{wu_stat} (or more, if the EI is valid and the device enters in active mode).

In active mode the inputs have in fact only the internal pull-down resistor and the input status can be read by SPI.

Static sense should be configured before the read operation has started in order to reflect the actual input level.

As the DIR1_EN enable bit, in CR1 (0x26), is set to 1 by default, the DIR1/EI2 pin is a low voltage direct driving of HS0. Threshold is set in this case at 1.5 V.

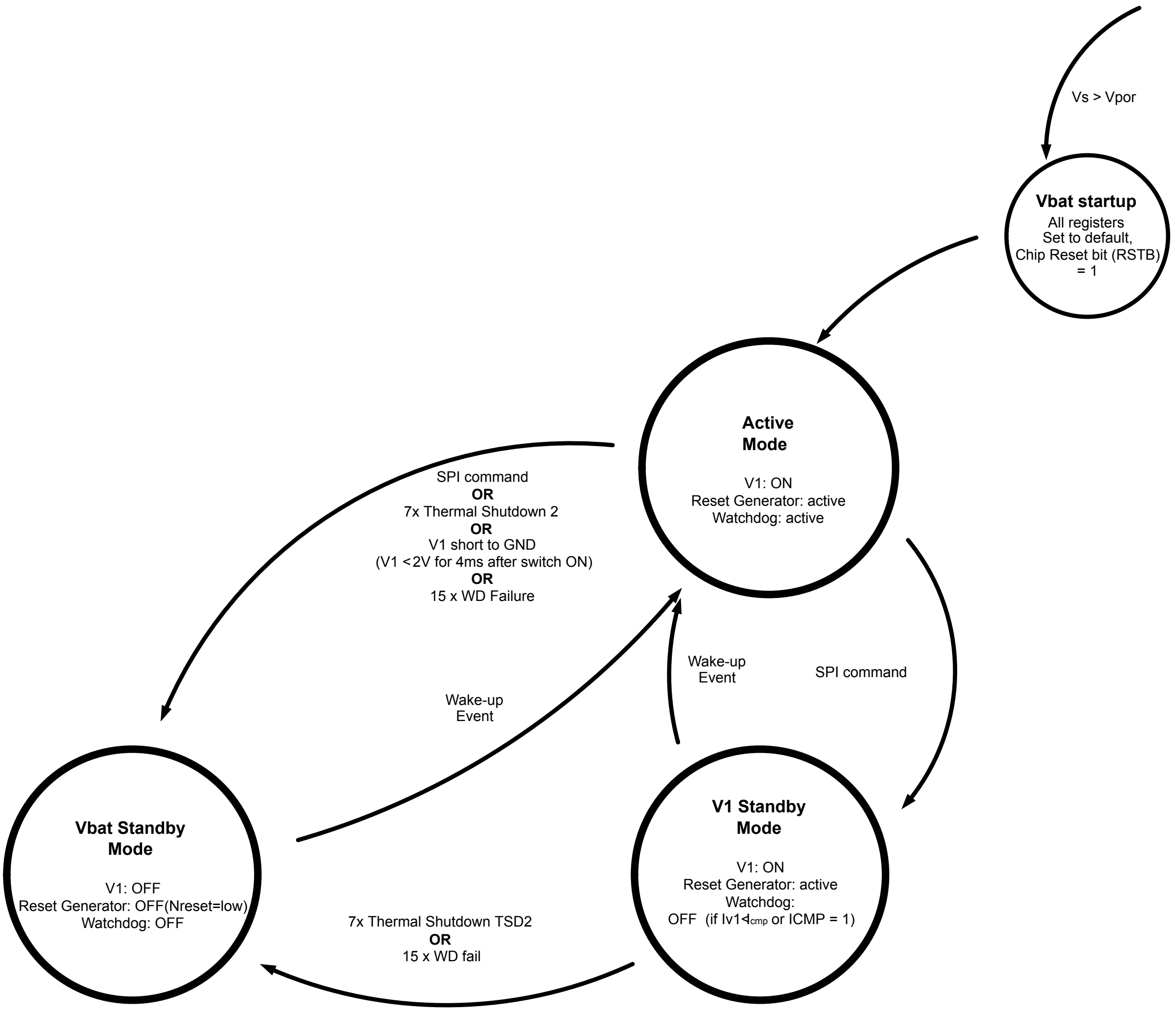
3.5 Functional overview (truth table)

Table 55. Truth table

Function	Comments	Operating modes		
		Active mode	V1_Standby static mode (cyclic sense)	VBAT_Standby static mode (cyclic sense)
Voltage regulator V1	V_{OUT} = 5 V	On	On (1)	Off
Voltage regulator V2	V_{OUT} = 5 V	On/Off (2)	On(2)/Off	Off
Reset generator		On	On	Off
Window watchdog	V1 monitor	On	Off (On if $I_{V1} > I_{cmp}$ and I_{CMP} = 0)	Off
Wake-up		Off	Active (3)	Active(3)
HS cyclic supply	Oscillator time base	On/Off	On(2)/Off	On(2)/Off
LIN	LIN 2.2a	On	Off (4)	Off(4)
CAN FD		On/Off (5)	Off(4)	Off(4)
Oscillator		On	On/Off(6)	On/Off(6)
Vs monitor		On	(7)	(7)
H-bridge gate driver, EC control, bridge drivers, heater driver, all high-side drivers (except HS15 and HS0)		On/Off(2)	Off	Off
HS15 (P-channel HS)		On/Off(2)	On/Off(2)	On/Off(2)
HS0 (P-channel HS)		On/Off(2)	On/Off(2)	On/Off(2)
Charge pump		On	Off	Off
Thermal shutdown TSD2		On	On	Off
Thermal shutdown TSD1x (for P-channel HS)		On	On	On/Off(2)

1. *Supply the processor in low current mode.*
2. *According to SPI setting.*
3. *Unless disabled by SPI.*
4. *The bus state is internally stored when going to standby mode. A change of bus state leads to a wake-up after exceeding the internal filter time (if wake-up by LIN or CAN is not disabled by SPI).*
5. *After power on, the CAN FD transceiver is in 'CAN Trx Standby' Mode. It is activated by SPI command (CAN_ACT = 1).*
6. *ON, if it is enabled at least one of the following: cyclic sense, HS15, HS0, V2.*
7. *Cyclic activation = pulsed ON during cyclic sense.*

Figure 16. Main operating modes



3.6 Configurable window watchdog

During normal operation, the watchdog monitors the microcontroller within a programmable trigger cycle.

After power-on or standby mode, the watchdog starts with a timeout (long open window t_{LW}). The timeout allows the microcontroller to run its own setup and then to start the window watchdog by setting TRIG = 1. Subsequently, the microcontroller has to serve the watchdog by alternating the watchdog trigger bit within the safe trigger area Tswx. The trigger time is configurable by SPI.

A correct watchdog trigger signal immediately starts the next cycle.

After 8 watchdog failures in sequence, the V1 regulator is switched off for tv1off. After 7 additional watchdog failures the V1 regulator is turned off permanently and the device goes into forced VBAT_Standby mode. The status bit FORCED_SLEEP_WD (SR 8) is set. A wake-up is possible by any activated wake-up source.

In case of a watchdog failure, the power outputs and V2 are switched off and the device enters fail-safe mode. All control registers are set to their failsafe values.

The following diagrams illustrate the watchdog behavior of the device. The diagrams are split in 3 parts. The first diagram shows the functional behavior of the watchdog without any error. The second diagram covers the behavior covering all the error conditions, which can affect the watchdog behavior. The third diagram shows the transition in and out of debug mode. All 3 diagrams can be overlapped to get all the possible state transitions under all circumstances. For a better readability, they were split in normal operating, with errors and debug mode.

Figure 17. Watchdog in normal operating mode (no errors)

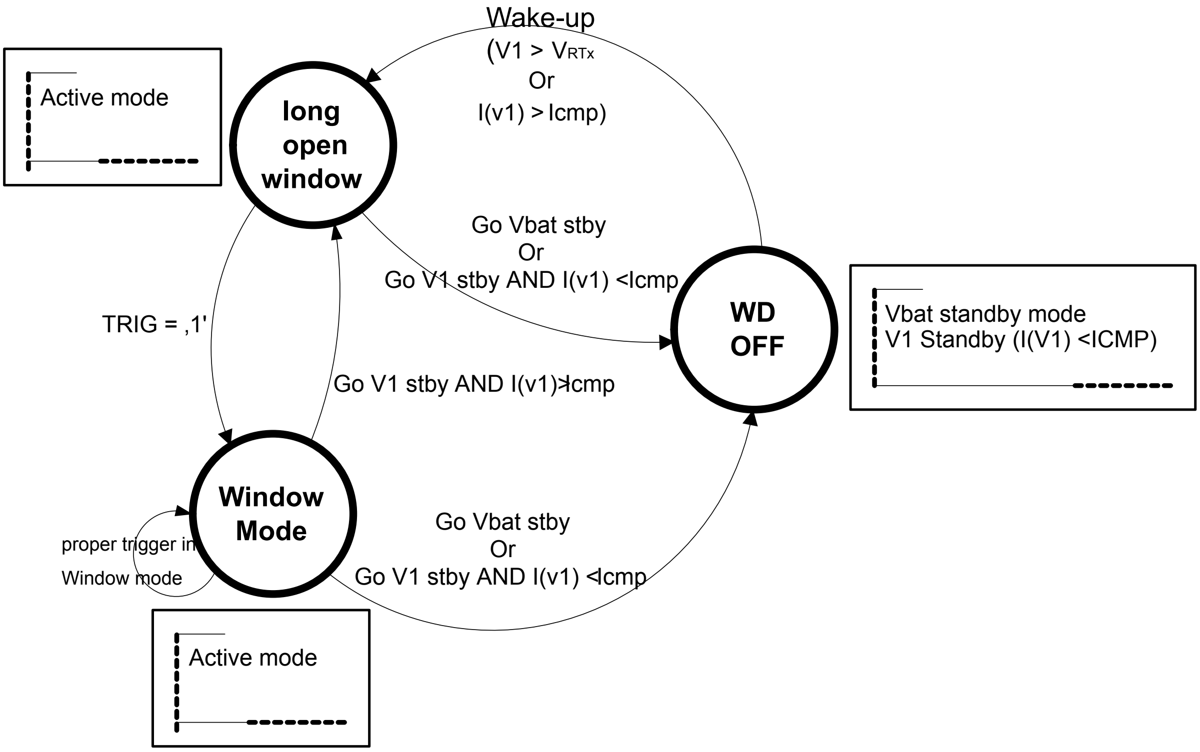
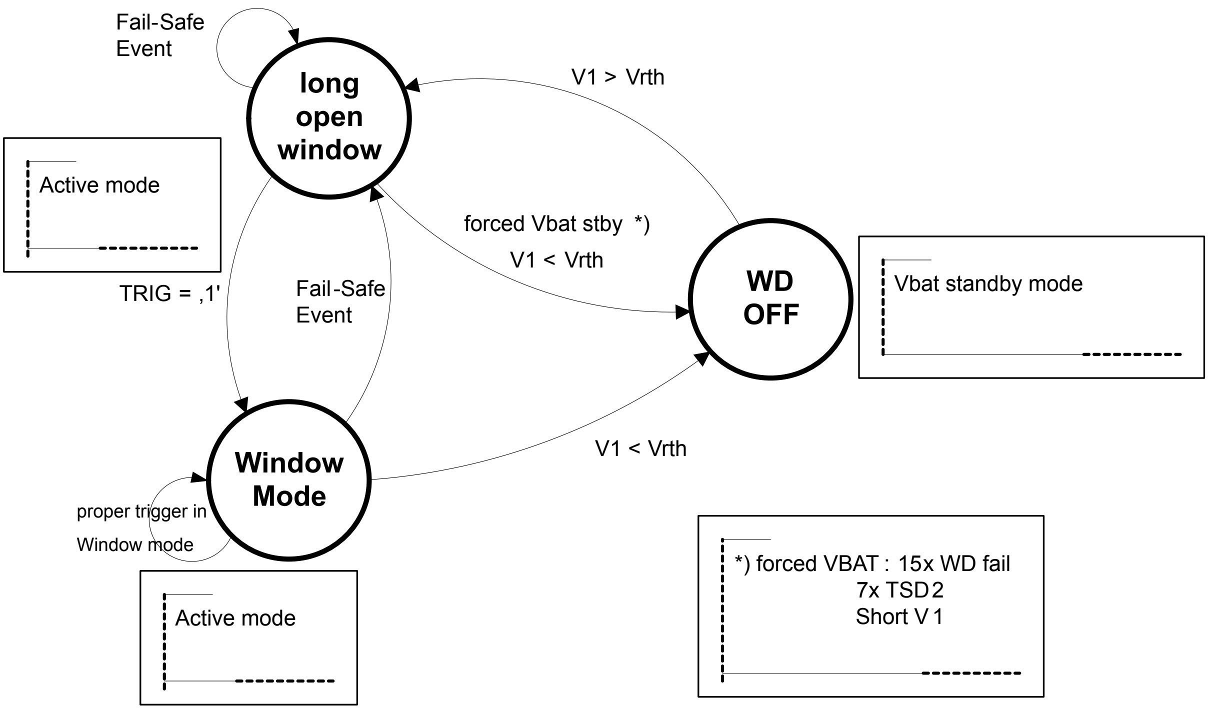


Figure 18. Watchdog with error conditions



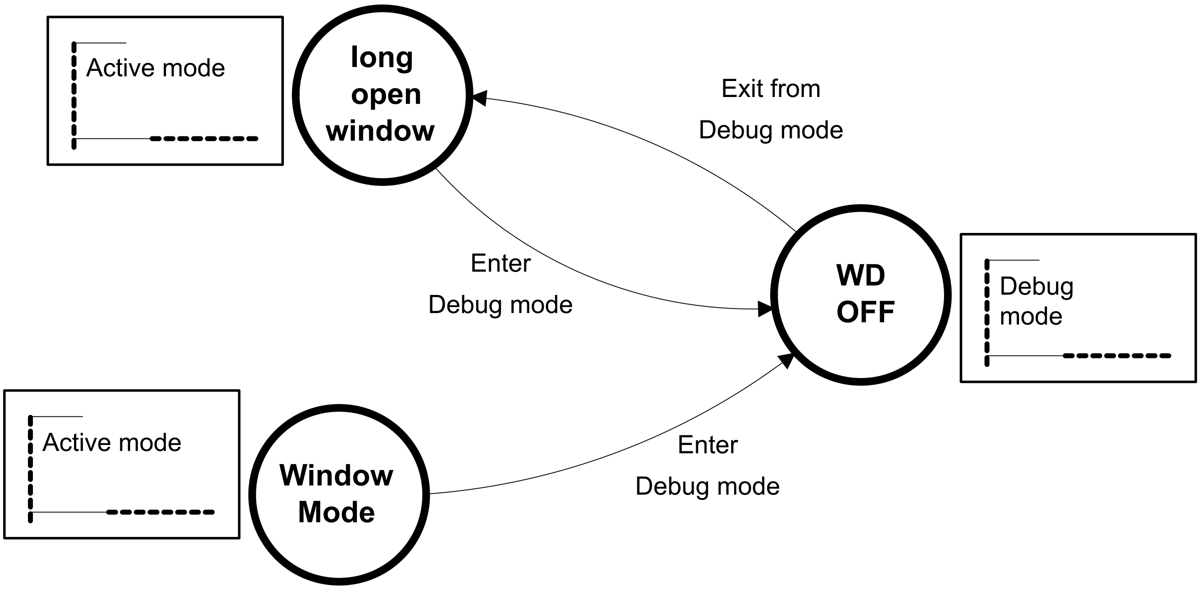


Figure 19. **Watchdog in debug mode**

Note: Whenever the device is operated without servicing the mandatory watchdog trigger events, a sequence of 15 consecutive reset events is performed and the device enters the Forced_Vbat_Stby mode with the bit FORCED_SLEEP_WD in SR8 set. If the device is woken up after such a forced VBAT_Standby condition and the watchdog is still not serviced, the device, after one long open watchdog window reenters the same Forced_Vbat_Stby mode until the next wake-up event. In this case, an additional watchdog failure is generated, but the fail counter is not cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

3.6.1 Change watchdog timing

The watchdog trigger time can be configured by setting the WD_TIME (CR 17) bit. Writing to these bits is only possible with the first SPI command after setting WD_CONFIG_EN = 1. The WD_CONFIG_EN bit is reset to 0 automatically with the next SPI command.

When FAIL_SAFE is active these SPI registers are not accessible and therefore in this case first the FAIL_SAFE status needs to be cleared. In case of WD_FAIL, the clear is performed by trigging in long open window.

When a new configuration has been programmed, the watchdog continues behaving with the old configuration until the next trig event.

The new value of WD_TIME is loaded in the watchdog module on the next trig event after the SPI configuration. The following WD cycle uses the new programmed value.

3.7 Fail-safe mode

3.7.1 Temporary failures

L99DZ380 enters fail-safe mode in case of:

- Watchdog failure
- V1 failure ($V1 < V_{rth}$ for $t > t_{V1FS}$)
- Thermal shutdown TSD2

The fail-safe functionality is also available in V1_Standby mode. During V1_Standby mode the fail-safe mode is entered in the following cases:

- V1 failure ($V1 < V_{rth}$ for $t > t_{V1FS}$)
- Watchdog failure (if watchdog still running due to Iv1 > Icmp)
- Thermal shutdown TSD2

In fail-safe mode the device returns to a fail-safe state. The fail-safe condition is indicated to the system in the global status byte. The conditions during fail-safe mode are:

- All outputs are turned off
- All control registers are set to default values
- Write operations to control registers are blocked until the fail-safe condition is cleared (see table below). Only the following bits are not write protected:
  - CR18 (0x3F):
    - TRIG
    - CAN_ACT
  - CR17 (0x3E):
    - Timer settings (bits 8…23)
  - CR14 (0x3B):
    - HS15_x (bits 8…11)
    - HS0_x (bits 12…15)
  - CR5 (0x32) to CR10 (0x37)
    - PWM frequency and duty cycles
  - CR1 (0x26)
    - TRIG
    - V2_0
    - V2_1
- LIN transmitter remains on
- Corresponding failure bits in status registers are set
- FS bit (bit 0 global status byte) is set

In fail-safe mode the device returns to a fail-safe state until the fail-safe condition is removed and the fail-safe was read by SPI. Depending on the root cause of the fail-safe operation, the actions to exit fail-safe mode are as shown in the following table.

Table 56. Temporary failures conditions

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	Watchdog Early write failure or expired window	FS (global status byte) = 1 WDFAIL (SR8) = 1 WDFAIL_CNT_x (SR8) = n+1	TRIG = 1 during long open window Read&Clear SR8
V1	Short at turn on	FS (global status byte) = 1 V1FAIL = 1 FORCED SLEEP TSD2/V1SC (SR8) = 1	Wake-up Read&Clear SR8
	Undervoltage	FS (global status byte) = 1 V1UV = 1[(1)] V1FAIL (SR7) = 1[(2)]	V1 > V_{rth} Read&Clear SR8
Temperature	T_J > TSD2	FS (global status byte) =1 TW (SR7) = 1 TSD1 (SR8) = 1 TSD2 (SR8) = 1	T_J < TSD2 Read&Clear SR8

1. *Bit SR8/V1UV is set for t > t_{uv1} (16 µs). Fail-safe bit GSR/FS is set only after t_{RD} (NRESET low pulse).*
2. *If V1 < V1fail (for t > t_{v1fail}). The fail-safe bit is located in the global status register.*

3.7.2 Non-recoverable failures - entering force VBAT standby mode

If the fail-safe condition persists and all attempts to return to normal system operation fail, the L99DZ380 enters the forced VBAT standby mode in order to prevent damage to the system. The forced VBAT standby mode can be terminated by any wake-up source. The root cause of the forced VBAT standby mode is indicated in the SPI status registers.

In forced VBAT standby mode, all control registers are set to power on default.

The forced VBAT standby mode is entered in case of:

- Multiple watchdog failures: FORCED_SLEEP_WD = 1 (15x watchdog failure)
- Multiple thermal shutdown 2: FORCED_SLEEP_TSD2_V1SC = 1 (7x TSD2)
- V1 short at turn on (V1 < V1fail for t > $t_{V1short}$): FORCED_SLEEP_TSD2_V1SC (SR8) = 1
- Loss of ground: SGNDLOSS (SR3) = 1

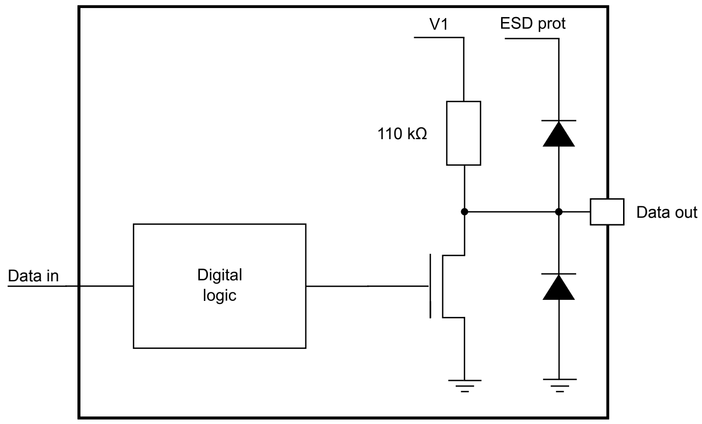
Table 57. Non recoverable failures conditions

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	15 consecutive watchdog failures	FS (global status byte) =1 WDFAIL (SR8) = 1 FORCED_SLEEP_WD (SR8) = 1	Wake-up TRIG = 1 during long open window Read&Clear SR8
V1	Short at turn on	FS (global status byte) = 1 V1FAIL = 1 FORCED_SLEEP_TSD2_V1SC (SR8) = 1	Wake-up Read&Clear SR8
Temperature	7 times TSD2	FS (global status byte) =1 TW (SR7) = 1 TSD1 (SR8) = 1 TSD2 (SR8) = 1 FORCED_SLEEP_TSD2_V1SC (SR8) = 1	Wake-up Read&Clear SR8
SGND	Loss of ground at SGND pin	FS (global status byte) = 1 SGNDLOSS (SR3) = 1	Wake-up Read&Clear SR3

3.8 Reset output

If V1 is turned on and the voltage exceeds the V1 reset threshold, the reset output “NRESET” is pulled up by the internal pull-up resistor to V1 voltage after a reset delay time (t_{RD}). This is necessary for a defined start of the microcontroller when the application is switched on. Since the NRESET output is realized as an open drain output, it is also possible to connect an external NRESET open drain NRESET source to the output. As soon as the NRESET is released, the watchdog timing starts with a long open window.

Figure 20. NRESET pin



A reset pulse is generated in case of:

- V1 drops below Vrth (configurable by SPI) for t > t_{uv1}
- Watchdog failure

After turning on the V1 regulator (V_{SREG} power on or wake-up from VBAT_Standby mode), NReset is kept low for t_{RD} in order to keep the microcontroller in reset until supply voltage is stable.

3.9 LIN bus interface

3.9.1 Features

- 2 LIN ISO 17987-4/2016 compliant transceiver
- Meets hardware requirements for transceivers (version 1.3)
- Data rate up to 20 kbit/s
- GND disconnection fail-safe at module level
- Off mode: does not disturb network
- GND shift operation at system level
- Microcontroller interface with CMOS compatible I/O pins
- Internal pull-up resistor
- ESD and transient immunity according to ISO7637 and EN / IEC61000-4-2
- Matched output slopes and propagation delay
- Wake-up behavior according to LIN2.2a and "Hardware requirements for LIN, CAN and flexray interfaces (version 1.3)"

At V_{SREG} > V_{POR} (that is V_{SREG} Power-on Reset threshold), the LIN transceiver is enabled.

The LIN transmitter is disabled in case of the following errors:

- Dominant TXDL time out
- LIN permanent recessive
- TSD1 on cluster 8 (global) if TSD_CLUSTER_EN = 1
- TSD1 on any clusters if TSD_CLUSTER_EN = 0 (default)

The LIN receiver is not disabled in case of any failure condition (it is reactivated in case of FS by thermal shutdown).

3.9.2 Error handling

The device LIN transceiver provides the following three error handling features:

1. **Dominant TXDL time out**
   If TXDL is in dominant state (low) for t > $t_{dom(TXDL)}$ the transmitter is disabled, the status bit LIN_TXD_DOM (SR7) is set.
   The transmitter remains disabled until the status bit is cleared.
   The TXD dominant timeout detection can be disabled via SPI (LIN_TXD_TOUT = 0).
2. **Permanent recessive**
   If TXDL changes to dominant (low) state but the RXDL signal does not follow within t < t_{LIN} the transmitter is disabled, the status bit LIN_PERM_REC (SR7) is set.
   The transmitter remains disabled until the status bit is cleared.
3. **Permanent dominant**
   If the bus state is dominant (low) for t > $t_{dom(bus)}$ a bus permanent dominant failure is detected. The status bit LIN_PERM_DOM (SR7) is set.
   The transmitter is not disabled.

3.9.3 Wake up from standby modes

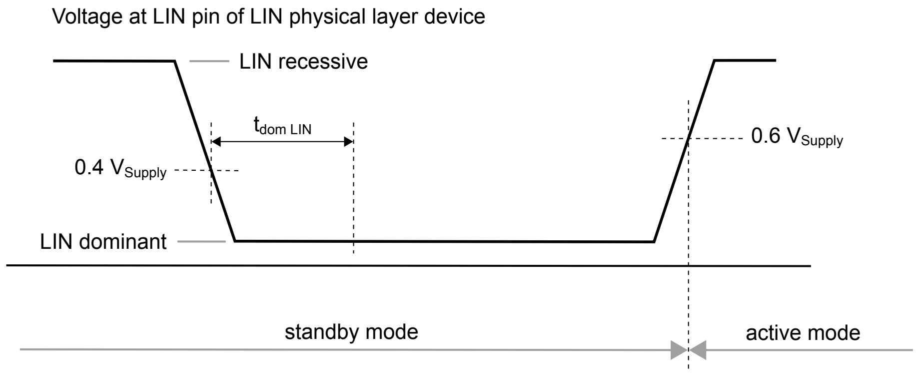
In low-power modes (V1_Standby and VBAT_Standby) the L99DZ380 can receive two types of wake-up signals from the LIN bus (configurable by SPI bit LIN_WU_CONFIG):

- Recessive dominant recessive pattern with t > t_{dom_LIN} (default, according to LIN 2.2a)
- A dominant time of at least 150 µs must be identified as a wake-up. Shorter dominant times may wake-up the device
- State change recessive to dominant or dominant to recessive (according to LIN 2.1)

Note: Dominant levels having duration less than a glitch filter time (it is defined 28 µs minimum, according to OEM requirements version 1.3) have to be filtered and therefore they cannot wake-up the device.

Pattern wake-up (default)

Figure 21. **Wake-up behavior according to LIN 2.2a**



Status change wake-up recessive to dominant

Normal wake-up can occur when the LIN transceiver was set in standby mode while LIN was in recessive (high) state. A dominant level at LIN for t_{LINBUS}, switch the device to active mode.

Status change wake-up dominant to recessive

If the LIN transceiver was set in standby mode while LIN was in dominant (low) state, recessive level at LIN for t_{LINBUS}, switch the device to active mode.

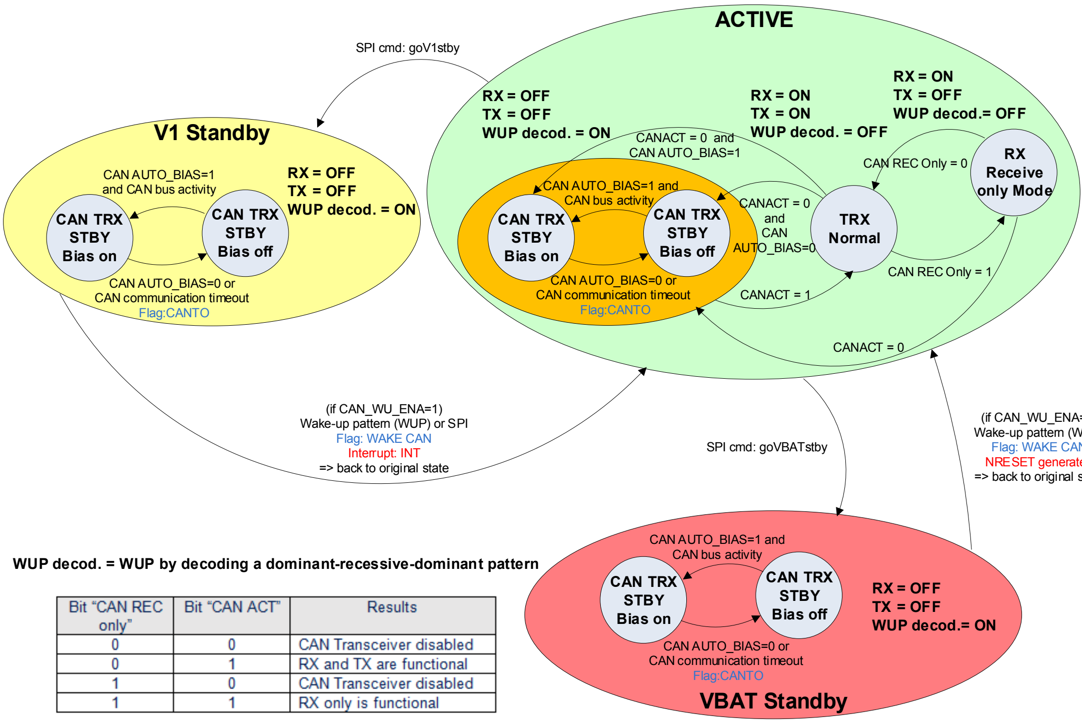
3.10 CAN FD bus transceiver

3.10.1 Features

- ISO 11898-2:2016 compliant
- CAN-FD cell has been designed according to “hardware requirements for transceivers (version 1.3)”
- Listen mode (transmitter disabled)
- SAE J2284 compliant
- Bit rate up to 5 Mbit/s
- Function range from -27 V to 40 V DC at CAN pins
- GND disconnection fail-safe at module level
- GND shift operation at system level
- Microcontroller interface with CMOS compatible I/O pins
- ESD and transient immunity according to ISO7637 and EN/IEC61000-4-2
- Matched output slopes and propagation delay

3.10.2 CAN transceiver operating modes

Figure 22. **Transceiver state diagram**



Bit "CAN REC only"	Bit "CAN ACT"	Results
0	0	CAN Transceiver disabled
0	1	RX and TX are functional
1	0	CAN Transceiver disabled
1	1	RX only is functional

TRX normal mode

Full functionality of the CAN transceiver is available (transmitter and receiver) and the automatic voltage biasing is enabled.

State transitions from TRX normal mode to VBAT_Standby and V1_Standby are possible. No interrupt is generated in this mode.

CAN TRX STBY mode

The CAN transmitter is disabled in this mode and the RXDC pin is kept at high (recessive) level. CAN receiver is capable of detecting a wake-up pattern (WUP). In V1_Standby mode and VBAT_Standby mode, a WUP is indicated to the microcontroller by an interrupt signal.

There is no automatic state transition into TRX normal mode in the case of a detected CAN wake-up signal (WUP). After serving the interrupt, the microcontroller can initiate a state transition into TRX normal mode by setting the SPI bit CAN_ACT to '1'. (This can be done 160 µs after enabling the wake-up through CAN_WU_EN=1).

Moreover, in this mode two further submodes are possible ("Bias ON" or "Bias OFF"), depending on the CAN_AUTO_BIAS bit in CR1 (compliant with ISO 11898-2:2016) or timeout conditions.

3.10.3 CAN error handling

The devices provide the following four error handling features.

After power on reset (VS > VPOR) the CAN transceiver is disabled. The transceiver is enabled by setting CAN_ACT = 1.

The CAN transmitter is disabled automatically in case of the following errors:

- Dominant TXDC time out
- CAN permanent recessive
- RXDC permanent recessive
- TSD1 on cluster 8 (global) if TSD_CLUSTER_EN = 1
- TSD1 on any clusters if TSD_CLUSTER_EN = 0 (default)

The CAN receiver is not disabled in case of any failure condition.

Dominant TXDC time out

If TXDC is in dominant state (low) for t > $t_{dom(TXDC)}$ the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN Bus permanent recessive

If TXDC changes to dominant (low) state but CAN bus does not follow for 4 times, the transmitter is disabled, status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

CAN permanent dominant

If the bus state is dominant (low) for t > t_{CAN} a permanent dominant status is detected. The status is latched and can be read and optionally cleared by SPI. The transmitter is not disabled.

RXDC permanent recessive

If RXDC pin is clamped to recessive (high) state, the controller is not able to recognize a bus dominant state and could start messages at any time, which results in disturbing the overall bus communication. Therefore, if RXDC does not follow TXDC for 4 times the transmitter is disabled. The status bit is latched and can be read and optionally cleared by SPI. The transmitter remains disabled until the status register is cleared.

3.10.4 Wake-up by CAN

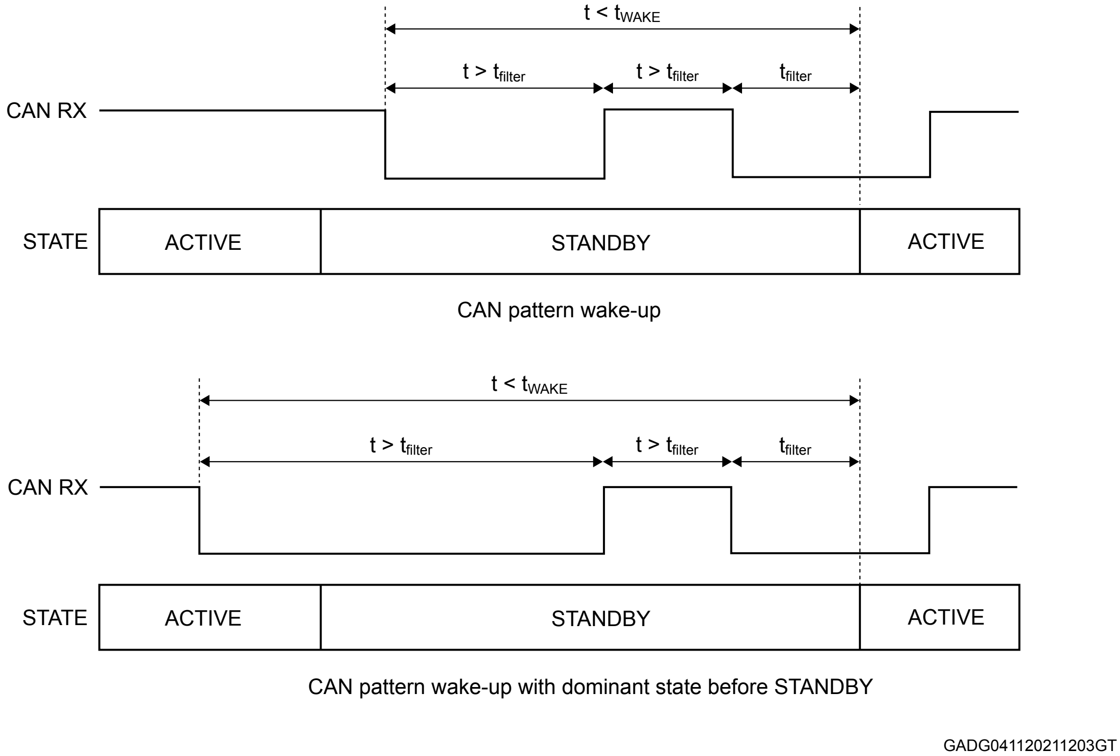
The default setting for the wake-up behavior after Power-on Reset is the wake-up by regular communication on the CAN bus. When the CAN transceiver is in a standby mode (CAN TRX STBY) the device can be woken up by sending 2 consecutive dominant bits separated by a recessive bit.

Normal pattern wake-up can occur when the CAN pattern wake-up option is enabled, and the CAN transceiver was set in standby mode (CAN TRX STBY) while CAN bus was in recessive (high) state or dominant (low) state. In order to wake-up the device, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses, each of which must be longer than t_{filter}.
- The distance between 2 pulses must be longer than t_{filter}.
- The two pulses must occur within a time frame of t_{wake}.
- Wake-up occurs when duration of the second pulse becomes longer than t_{filter}.

Note: A wake-up caused by a message on the bus starts the voltage regulator and the microcontroller to switch the application back to normal operation mode.

Figure 23. CAN wake-up capabilities



Note: The waveforms above illustrate the wake-up behavior from V1_Standby mode. For wake-up from VBAT_Standby mode the NRESET signal (with 2 ms timing) is generated instead of the RXDL (interrupt) signal.

3.10.5 CAN receive only mode

During TRX normal mode, with the CAN_REC_ONLY bit it is possible to disable the CAN transmitter. In this mode it is possible to listen to the bus but not sending to it. The receiver termination network is still activated in this mode.

3.10.6 CAN looping mode

If the CAN_LOOP_EN (CR1) is set the TXDC input is mapped directly to the RXDC pin. This mode can be used in combination with the CAN receive only mode, to run diagnosis for the CAN protocol handler of the microcontroller.

3.11 Serial peripheral interface (ST SPI standard)

A 32-bit SPI is used for bidirectional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in the following mode:

- **CPOL = 0 and CPHA = 0**
  For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.
  This device is not limited to microcontroller with a built in SPI. Only three CMOS compatible output pins and one input pin need to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO pin reflects the global error flag (fault condition) of the device.
- **Chip select not (CSN)**
  The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.
  If CSN = low for t > $t_{CSNfail}$ the DO output is switched to high impedance in order not to block the signal line for other SPI nodes.

- **Serial data in (DI)**
  The input pin is used to transfer serial data into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to the data input register. The writing to the selected data input register is only enabled if exactly 32 bits are transmitted within one communication frame (that is CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

- **Serial data out (DO)**
  The data output driver is activated by a logical low level at the CSN input and switches from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.
- **Serial clock (CLK)**
  The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK frequency up to 4 MHz.

3.12 Power supply fail

3.12.1 VS supply failure

VS overvoltage

If the supply voltage V_S reaches the overvoltage threshold VSOV:

- LIN1 and LIN2 remain enabled
- CAN remains enabled
- HB1, ..., HB6, HB20, HB21 and HS7, .. , HS14, HS16, .. , HS19 are turned off (default)
- The shutdown of outputs may be disabled by SPI (VS_OV_SD_EN = 0)
- Charge pump is disabled (and is switched on automatically in case the supply voltage recovers to normal operating voltage)
- H-bridge gate driver and heater Power MOSFET gate driver are switched into sink condition
- ECV is switched in high impedance state and ECDR is discharged by $R_{ECDRDIS}$ (to ensure the gate of the external Power MOSFET is discharged => EC mode considered as off)
- Recovery of outputs after overvoltage condition is configurable by SPI
  – VS_LOCK_EN (CR16) = 1: outputs are off until Read&Clear VS_OV (SR7)
  – VS_LOCK_EN (CR16) = 0: outputs turned on automatically after V_S overvoltage condition has recovered
- The overvoltage bit VS_OV (SR7) is set and can be cleared with a ‘Read&Clear’ command. The overvoltage bit is reset automatically if VS_ LOCK_EN (CR16) = 0 and the overvoltage condition has recovered

V_S undervoltage

If the supply voltage Vs drops below the undervoltage threshold voltage (VSUV):

- LIN remains enabled
- CAN remains enabled
- HB1, ..., HB6, HB20, HB21 and HS7, .. , HS14, HS16, .. , HS19 are turned OFF (default). The shutdown of outputs may be disabled by SPI (VS_UV_SD_EN (CR16) = 0).[1]
- ECV is switched in high impedance state and ECDR is discharged by RECDRDIS (to ensure the gate of the external Power MOSFET is discharged => EC mode considered as off). This occurs if VS_UV_SD_EN = 1, otherwise remains unchanged until CP_LOW = 1
- Recovery of outputs after undervoltage condition is configurable by SPI:
  – VS_LOCK_EN (CR16) = 1: outputs are off until Read&Clear VS_UV (SR7)
  – VS_LOCK_EN (CR16) = 0: outputs turned on automatically after V_S undervoltage condition has recovered

- The undervoltage bit (V_{SUV}) is set and can be cleared with a ‘Read and Clear’ command. The undervoltage bit is removed automatically if VS_LOCK_EN = 0 and the undervoltage condition has recovered
- H-bridge gate driver passes to resistive low condition. (If VS_UV_SD EN = 1, otherwise remains unchanged until CP_LOW = 1)
- Heater gate driver passes to resistive low condition. (If VS_UV_SD EN = 1, otherwise remains unchanged until CP_LOW = 1)(1)

1. *The functionality is not guaranteed in the range $V_{por} < V_S < V_{SUV}$.*

3.12.2 VSREG supply failure

VSREG overvoltage

If the supply voltages V_{SREG} reaches the overvoltage threshold V_{SREG_OV}:

- LIN1 and LIN2 are switched to high impedance (RX is still on)
- CAN remains enabled
- HS15 and HS0 are turned off (default).
- The shutdown of outputs may be disabled by SPI (VSREG_OV_SD_EN (CR16) = 0)
- ECV is switched in high impedance state and ECDR is discharged by $R_{ECDRDIS}$ (to ensure the gate of the external Power MOSFET is discharged => EC mode considered as off)
- Recovery of outputs after overvoltage condition is configurable by SPI:
  - VSREG_LOCK_EN (CR16) = 1: outputs are off until Read&Clear VSREG_ OV (SR7)
  - VSREG_LOCK_EN (CR16) = 0: outputs turned on automatically after V_{SREG} overvoltage condition has recovered
- The overvoltage bit VSREG_OV (SR7) is set and can be cleared with a ‘Read&Clear’ command. The overvoltage bit is reset automatically if VSREG_ LOCK_EN (CR16) = 0 and the overvoltage condition has recovered.

VSREG undervoltage

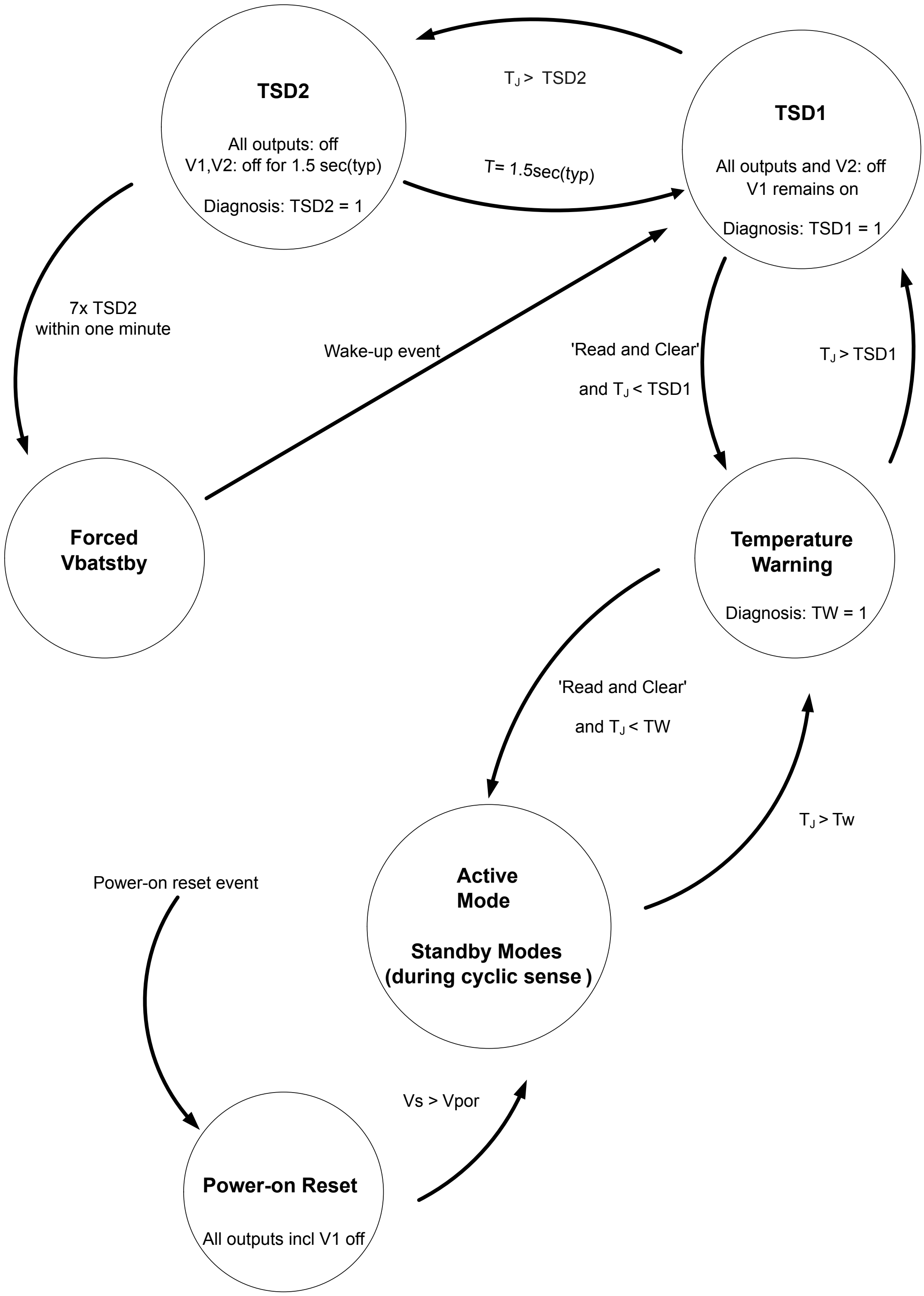
If the supply voltage V_{SREG} drops below the undervoltage threshold voltage (VSREG_UV):

- LIN1 and LIN2 are switched to high impedance (RX is still on(1))
- CAN remains enabled(1)
- HS15 and HS0 are turned off (default).
- The shutdown of outputs may be disabled by SPI (VSREG_UV_SD_EN (CR16) = 0)(1)
- ECV is switched in high impedance state and ECDR is discharged by $R_{ECDRDIS}$ (to ensure the gate of the external Power MOSFET is discharged => EC mode considered as off)
- recovery of outputs after undervoltage condition is configurable by SPI:
  - VSREG_LOCK_EN = 1: outputs are off until Read&Clear VSREG_UV (SR7)
  - VSREG_LOCK_EN = 0: outputs turned on automatically after V_{SREG} undervoltage condition has recovered
- The undervoltage bit (VSREG_UV (SR7) is set and can be cleared with a ‘Read&Clear’ command. The undervoltage bit is removed automatically if VSREG_LOCK_EN (CR16) = 0 and the undervoltage condition has recovered

1. *The functionality is not guaranteed in the range $V_{por} < V_S < V_{SUV}$.*

3.13 Temperature warning and thermal shutdown

Figure 24. Thermal shutdown protection and diagnosis



Note: The thermal state machine recovers the same state where it was before entering standby mode. In case of a TSD2 it is entered in TSD1 state.

3.14 Power outputs HB1,..., HB6, HB20, HB21, HS7,..., HS15, HS0, HS16,..., HS19

The component provides a total of 8 half bridges outputs HB1,…, HB6, HB20 and HB21 to drive motors and 14 stand-alone high-side outputs HS7,…, HS15 and HS0 and HS16,…, HS19 to drive for example LED's, bulbs or to supply contacts. All high-side outputs, except HS15 and HS0, are supplied by the pin VS. HS15 and HS0 are instead supplied by the buffered supply VSREG. HS0 is intended to be used as contact supply.

Only HS15 and HS0 can be activated in standby modes.

All high-side and low-side outputs switch OFF in case of:

- VS overvoltage and undervoltage (depending on configuration, see Section 3.12: Power supply fail)
- Overcurrent (depending on configuration, overcurrent recovery mode, see below)
- Over temperature (TSD1)
- Fail-safe event
- Loss of ground at SGND pin

In case of overcurrent or over temperature (TSD1 bit in SR8) condition, the drivers switch off. The corresponding status bit is latched and can be read and optionally cleared by SPI. The drivers remain off until the status is cleared.

In case overvoltage/undervoltage condition, the drivers are switched off. The corresponding status bit is latched and can be read and optionally cleared by SPI. If the Vlockout bits are set to '1' the drivers remain off until the status is cleared. If the Vlockout bit is set to '0' the drivers switch on automatically if the error condition disappears. Undervoltage and overvoltage shutdown can be disabled by setting <VS_UV_SD_EN> respectively <VS OV SD_EN> to '0'. In case of open-load condition, the corresponding status register is latched. The status can be read and optionally cleared by SPI. The high and low-side outputs are not switched off in case of open-load condition.

For HB1, …, HB6, HB20, HB21 the overcurrent recovery feature can be enabled by setting the HBx_OCR bit in CR13 (x = 1,.., 6); for HS7…HS10 the overcurrent recovery feature can be enabled by setting the HSy_OCR bit in CR13 (y = 7,..,10). If these bits are set to '1' the driver is automatically restarted from an overload condition. This overload recovery feature is intended for loads which have an initial current higher than the overcurrent limit of the output (for example inrush current of cold light bulbs). For HB1, HB5 and HB6 only, overcurrent threshold can be set via SPI (HBxOCTH_y bits in CR16, x = 1, 5, 6 and y = 0, 1) among three different values.

Each of the stand-alone high-side driver outputs HS7, …, HS19 and HS0 can be driven through:

- An internal generated PWM signal
- An internal timer
- One of the two direct drives (DIR1, DIR2)

When L99DZ380 is in V1_Standby or VBAT_Standby modes, HS0 and HS15 can be directly driven with DIR1/EI2 pin or PWM1-6/DIR2 pin.

Moreover, for each high-side driving LEDs, it is also available the "constant current mode" feature, which is configurable by SPI (CR3) and provides a constant current to the related output. This bit can be set only if the related driver is in OFF state and disables also its overcurrent and short-circuit detection (open-load detection remains ON). The "constant current code" is automatically disabled after the expiration time $t_{CCMtimeout}$.

The allowed sequence is the following:

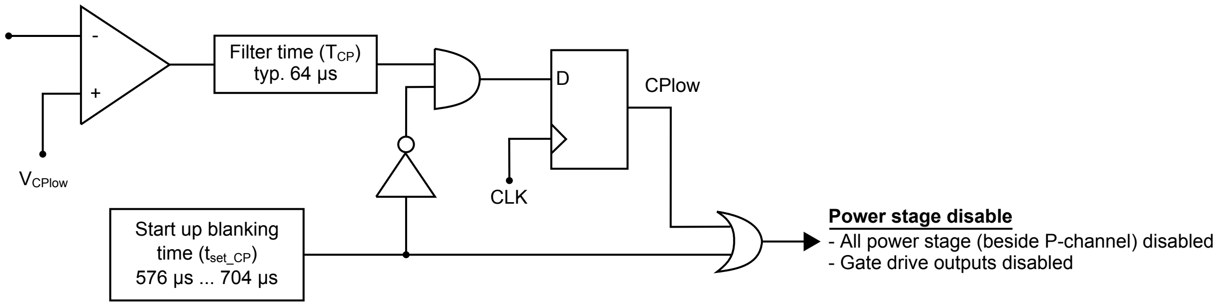
- Set HSx_CCM bit (x = 7, .., 19, 0), then turn ON the driver (other configurations are ignored): driver starts in current mode for $t_{CCMtimeout}$, then switches to ON mode, CCM is cleared by µC
  - If HSx_CCM bit is cleared by µC before timeout then driver is switched to ON mode
  - If CCM bit is set after driver has been started in ON, PWM, timer modes then CCM bit is ignored
- SC and OC are enabled in ON, PWM and timer modes, not in current mode
- Default value for CCM bit is OFF

3.15 Charge pump

The charge pump uses two external capacitors, which are switched with f_{CP}. The output of the charge pump has a current limitation. In standby mode and after a thermal shutdown has been triggered the charge pump is disabled. If the charge pump output voltage remains too low for longer than TCP, the Power MOSFET outputs and the EC-control are switched off. The H-bridge Power MOSFET gate drivers and the Heater Power MOSFET gate driver are switched to resistive low (according to undervoltage setting described in Section 3.12.1: VS supply failure) and the CP_LOW (SR7) bit is set. This bit has to be cleared to reactivate the drivers. In case of reaching the overvoltage shutdown threshold V_{SOV} the charge pump is disabled and automatically restarted after VS has restored to normal operating voltage. Charge pump may be also switched off in normal mode by setting the bits CP_OFF in CR2 only if CP_OFF_EN is set to “1” in CR1.

Note: In order to improve EME performance, the sampling frequency of the charge-pump is modulated (in his functional range) with a triangular function, providing a spreading of its energy spectrum. This “clock dithering” is performed automatically if the bit DISABLE_CP_DITH in CR1 is “0” (default value).

Figure 25. Charge pump low filtering and startup implementation



3.16 Inductive loads

Each of the half bridges is built by internally connecting high-side and low-side power DMOS transistors. Due to the built-in reverse diodes of the output transistors, inductive loads can be driven at the outputs HB1 to HB6 without external freewheeling diodes. The high-side drivers HS7 to HS15 and HS0, HS16 to HS19 are intended to drive resistive loads only. Therefore, only a limited energy (E < 1 mJ) can be dissipated by the internal ESD diodes in the freewheeling condition. For inductive loads (L > 100 µH) an external freewheeling diode connected between GND and the corresponding output is required. The low-side driver at ECV does not have a freewheel diode built into the device.

3.17 Open-load detection

The open-load detection monitors the load current in each activated output stage. If the load current is below the open-load detection threshold for at least t_{FOL} the corresponding open-load bit is set in the status register.

3.18 Overcurrent detection

An overcurrent condition is detected if the output current exceeds the overcurrent threshold (I_{OCXX}). In this case, a status flag (HBx_LS_OC / HBx_HS_OC with x = 1, ..., 6, 20, 21 and HSy_OC with y = 0, 7, .., 19) is set in the corresponding status register and the output is turned OFF to reduce the power dissipation and to protect the integrated circuit. The status flag must be cleared before the output can be turned ON by SPI.

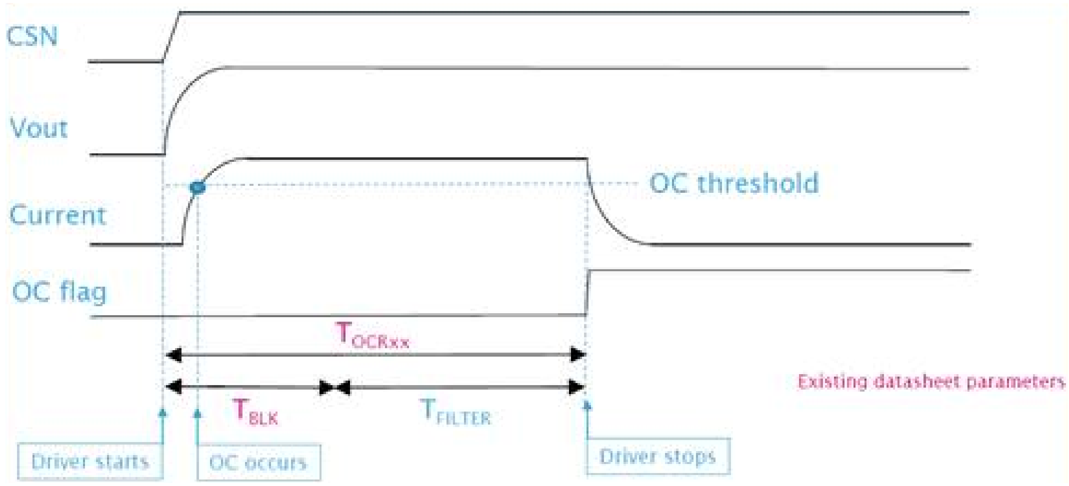
In overcurrent recovery mode (HBx_OCR or HSy_OCR set to 1, see Control register 13 (0x3Ah)) the output is switched OFF, but the correspondent HBx_OC or HSy_OC flag is not set. The output is switched ON automatically according to the configured overcurrent recovery frequency (HBx_OCR_FREQ or HSy_OCR_FREQ, see Control register 4 (CR4, 0x30)).

A blanking time t_{BLK} is applied at turn ON of the output.

The filter time applied is:

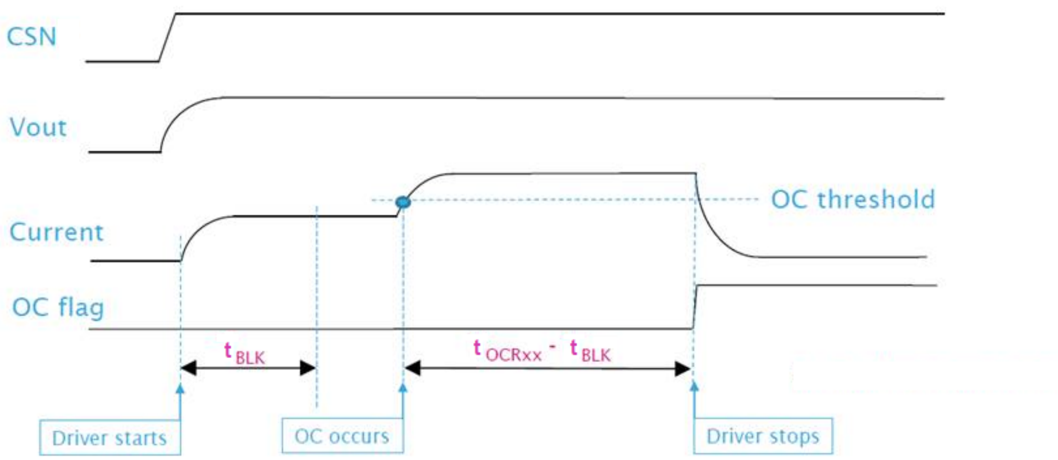
- t_{FOC} for outputs without overcurrent recovery mode (from HS11 to HS19 and HS0)
- t_{OCRxx} (programmable) for outputs with overcurrent recovery mode (from HB1 to HB6, HB20, HB21 and from HS7 to HS10); independent if overcurrent recovery mode is enabled or disabled by bit HBx_OCR / HSy_OCR.

Figure 26. Overcurrent threshold reached during blanking time



In that case, OC is detected and flagged after $T_{OCRxx} = T_{BLK} + T_{ILTER}$
the blanking time is only present after driver start.

Figure 27. OC threshold reached after blanking time (OC filter time is reduced by the blanking time)



For half bridges configured in PWM mode, no blanking time t_{BLK} is applied and the overcurrent filter time is reduced to t_{FOC_PWM}.

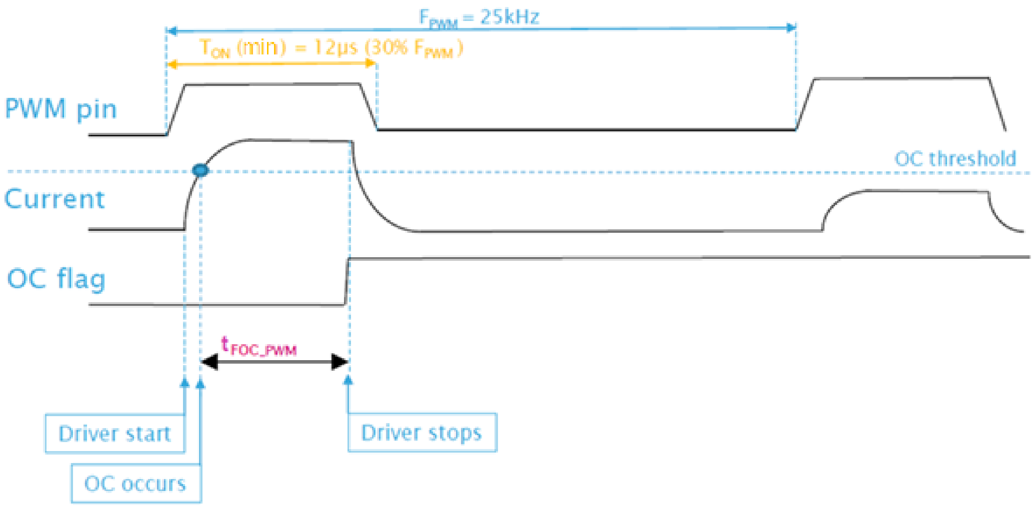


Figure 28. **Half bridges in PWM mode: filter time is t_{FOC_PWM}**

3.19 Short-circuit current detection

To distinguish low resistive short-circuit events from overcurrent conditions (especially in overcurrent recovery mode), a short-circuit current threshold is implemented for all the half bridges (HB1 to HB6, HB20, HB21).

Short-circuit condition is detected if the output current exceeds the short current threshold (I_{SCX}). In this case, a status flag HBx_HS_SC / HBx_LS_SC is set in the corresponding status register and the output is turned OFF. The corresponding overcurrent flag of the out (HBx_HS_OC / HBx_LS_OC) is also set. The HBx_HS_OC / HBx_LS_OC status flag must be cleared before the output can be turned ON by SPI.

A blanking time t_{BLK} is applied at turn on of the output.

The filter time applied is t_{FSC}.

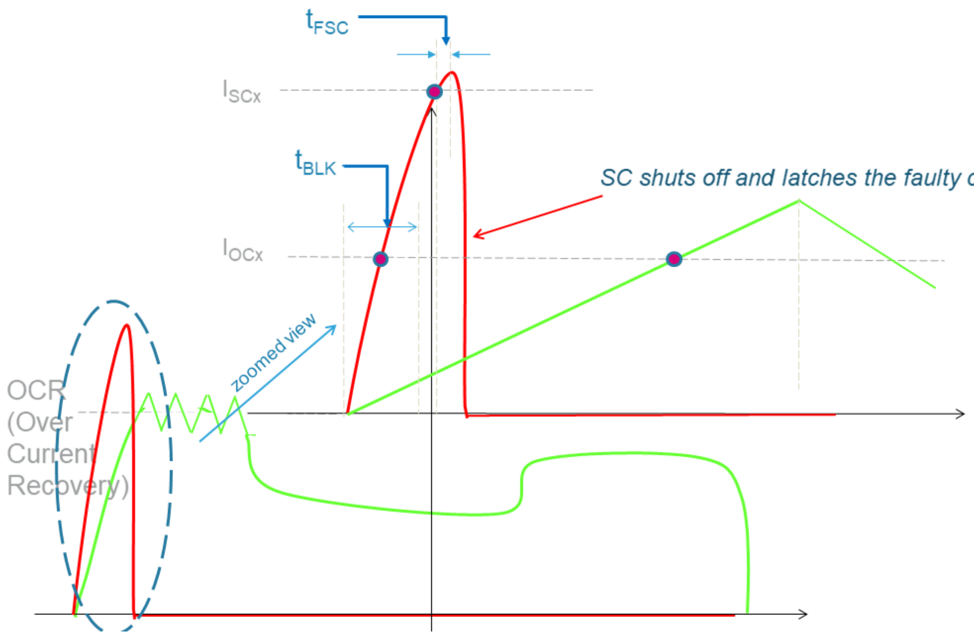
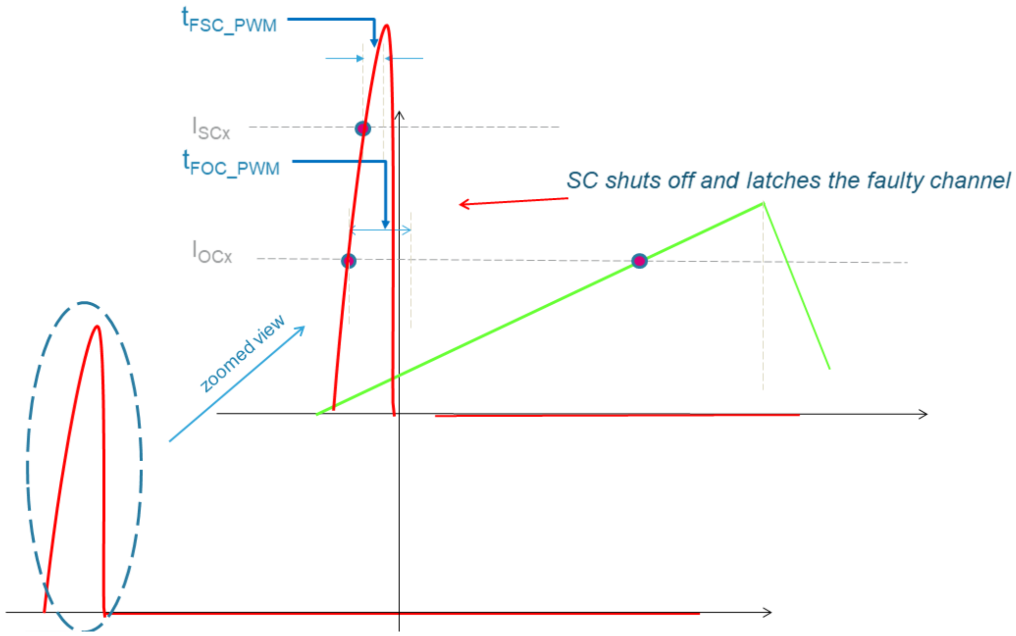


Figure 29. **Half bridge short-circuit detection in latch mode (overcurrent recovery disabled) and OCR mode (overcurrent recovery enabled)**

In PWM mode, no blanking time t_{BLK} is applied and the short-circuit filter time is reduced to t_{FSC_PWM}.

Figure 30. **Half bridge short-circuit detection in PWM mode: filter time is t_{FSC_PWM}**



High-side drivers with overcurrent recovery mode (HS7-HS10) are also short-circuit protected.

A short-circuit condition is detected at turn on of the output if the output voltage level remains low (< 2 V) after the programmed filter time t_{OCRxx}.

If a short-circuit condition is detected, the output is turned OFF and the overcurrent flag HSx_OC is set. This bit must be cleared before the output can be turned ON by SPI.

3.20 Current monitor

The current monitor sources an image of the power stage output current at the CM pin, which has the fixed ratio (I_{CMr} see Section 2.4.8: Current monitor output) of the instantaneous current of the selected high-side driver. The signal at output CM is blanked after switching on the driver until the correct settlement of the circuitry. The bits CM_SEL_x (x = 0, .., 4) in CR13 define which of the outputs is multiplexed to the current monitor output CM. The current monitor output allows a more precise analysis of the actual state of the load rather than the detection of an open-load or overload condition. For example, it can be used to detect the motor state (starting, free running, stalled). The current monitor output is enabled after the current monitor blanking time, when the selected output is switched on. If this output is off, the current monitor output is in high impedance mode. The current monitor can be activated/deactivated by selecting the corresponding setting for CM on/off bit.

3.21 PWM mode of the power outputs

All half bridges (except HB2 and HB3) can be, if suitably configured in CR2 and CR21, directly driven in a 25 kHz PWM mode via pin PWM1-6 and PWM4-5, PWM20 and PWM21. In this case, for the selected output, blanking time t_{BLK} is replaced by t_{FOC_PWM}.

When the PWM mode is activated on a half bridge low-side driver, all the others remain configurable according to the standard output bits (HBx_LS & HBx_HS) in CR16 (see Section 6.4.19: Control register 16 (0x3Dh)).

Note: *Active freewheeling is not implemented in PWM mode.*

3.22 Cross current protection

The eight half bridges of the device are crosscurrent protected by an internal delay time. If one driver (LS or HS) is turned off, the activation of the other driver of the same half bridge is automatically delayed by the crosscurrent protection time. After the crosscurrent protection time has expired the slew rate limited switch off phase of the driver is changed into a fast turn off phase and the opposite driver is turned on with slew rate limitation. Due to this behavior, it is always guaranteed that the previously activated driver is completely turned off before the opposite driver starts to conduct.

3.23 Overcurrent recovery mode

Loads with startup currents higher than the overcurrent limits (for example inrush current of lamps, start current of motors) can be driven by suitably using the programmable overcurrent recovery (OCR) mode. To enable this feature, which is available for HB1-6, HB20, HB21 and HS7-HS10, each of these drivers has a corresponding overcurrent recovery bit. If this bit is set, the output is turned OFF when the overcurrent threshold is reached and turned ON automatically after a programmable recovery time. The PWM modulated current provides sufficient average current to power up the load (for example heat up the bulb) until the load reaches operating condition. The recovery frequency (f_{OCR}) as well as the on time (t_{OCR}) is programmable in CR4.

3.24 H-bridge control

The PWMH and DIRH input controls the drivers of the external H-bridge transistors. In single motor mode the motor direction can be chosen with the direction input (DIRH), the duty cycle and frequency with the PWMH input (single mode). With the SPI-registers SD (CR12) and SDS (CR12) four different slow decay modes (via drivers and via diode) can be selected using the high-side or the low-side transistors. Unconnected inputs are defined by internal pull-down current. Alternatively, the bridge can be driven in half bridge mode (dual mode). By setting the dual mode bit DM = 1, both half bridges can be used for two separated motors, using the same control pins DIRH and PWMH.

Table 58. H-bridge control truth table

Nb	Control pins		Control bits				Failure bits					Output pin				Mode	Description
	DIRH	PWMH	HEN	SD	SDS	DM	CP_LOW	VS_OV	VS_UV	DS	TSD1	GH1	GL1	GH2	GL2		
1	x	x	0	x	x	x	x	x	x	x	x	RL	RL	RL	RL	Single	H-bridge disabled
2	x	x	1	x	x	x	1	0	0	0	0	RL	RL	RL	RL		Charge pump voltage too low
3	x	x	1	x	x	x	0	x	x	x	1	RL	RL	RL	RL		Thermal shutdown
4	x	x	1	x	x	x	0	1	0	0	0	L	L	L	L		Overvoltage
5	x	x	1	x	x	x	0	0	0	1	0	L[1]	L[1]	L[1]	L[1]		Short-circuit[1]
6	0	1	1	x	x	0	0	0	0	0	0	L	H	H	L		Bridge H2/L1 on
7	x	0	1	0	0	0	0	0	0	0	0	L	H	L	H		Slow-decay mode LS1 and LS2 on
8	0	0	1	0	1	0	0	0	0	0	0	L	H	L	L		Slow-decay mode LS1 on
9	1	0	1	0	1	0	0	0	0	0	0	L	L	L	H		Slow-decay mode LS2 on
10	1	1	1	x	x	0	0	0	0	0	0	H	L	L	H		Bridge H1/L2 on
11	x	0	1	1	0	0	0	0	0	0	0	H	L	H	L		Slow-decay mode HS1 and HS2 on
12	0	0	1	1	1	0	0	0	0	0	0	L	L	H	L		Slow-decay mode HS2 on

Nb	Control pins		Control bits				Failure bits					Output pin				Mode	Description
	DIRH	PWMH	HEN	SD	SDS	DM	CP_LOW	VS_OV	VS_UV	DS	TSD1	GH1	GL1	GH2	GL2		
13	1	0	1	1	1	0	0	0	0	0	0	H	L	L	L	Single	Slow-decay mode HS1 on
14	0	0	1	1	0	1	0	0	0	0	0	L	L	L	L	Dual	Half bridge mode
15	0	1	1	1	0	1	0	0	0	0	0	L	L	L	H		
16	1	0	1	1	0	1	0	0	0	0	0	L	H	L	L		
17	1	1	1	1	0	1	0	0	0	0	0	L	H	L	H		
18	0	0	1	0	1	1	0	0	0	0	0	L	L	L	L		
19	0	1	1	0	1	1	0	0	0	0	0	L	L	H	L		
20	1	0	1	0	1	1	0	0	0	0	0	H	L	L	L		
21	1	1	1	0	1	1	0	0	0	0	0	H	L	H	L		
22	0	0	1	1	1	1	0	0	0	0	0	H	L	H	L		
23	0	1	1	1	1	1	0	0	0	0	0	H	L	L	H		
24	1	0	1	1	1	1	0	0	0	0	0	L	H	H	L		
25	1	1	1	1	1	1	0	0	0	0	0	L	H	L	H		

1. *Only the half bridge (low-side and high-side), in which one Power MOSFET is in short-circuit condition is switched off. Both Power MOSFETs of the other half bridge remain active and driven by DIRH and PWMH.*

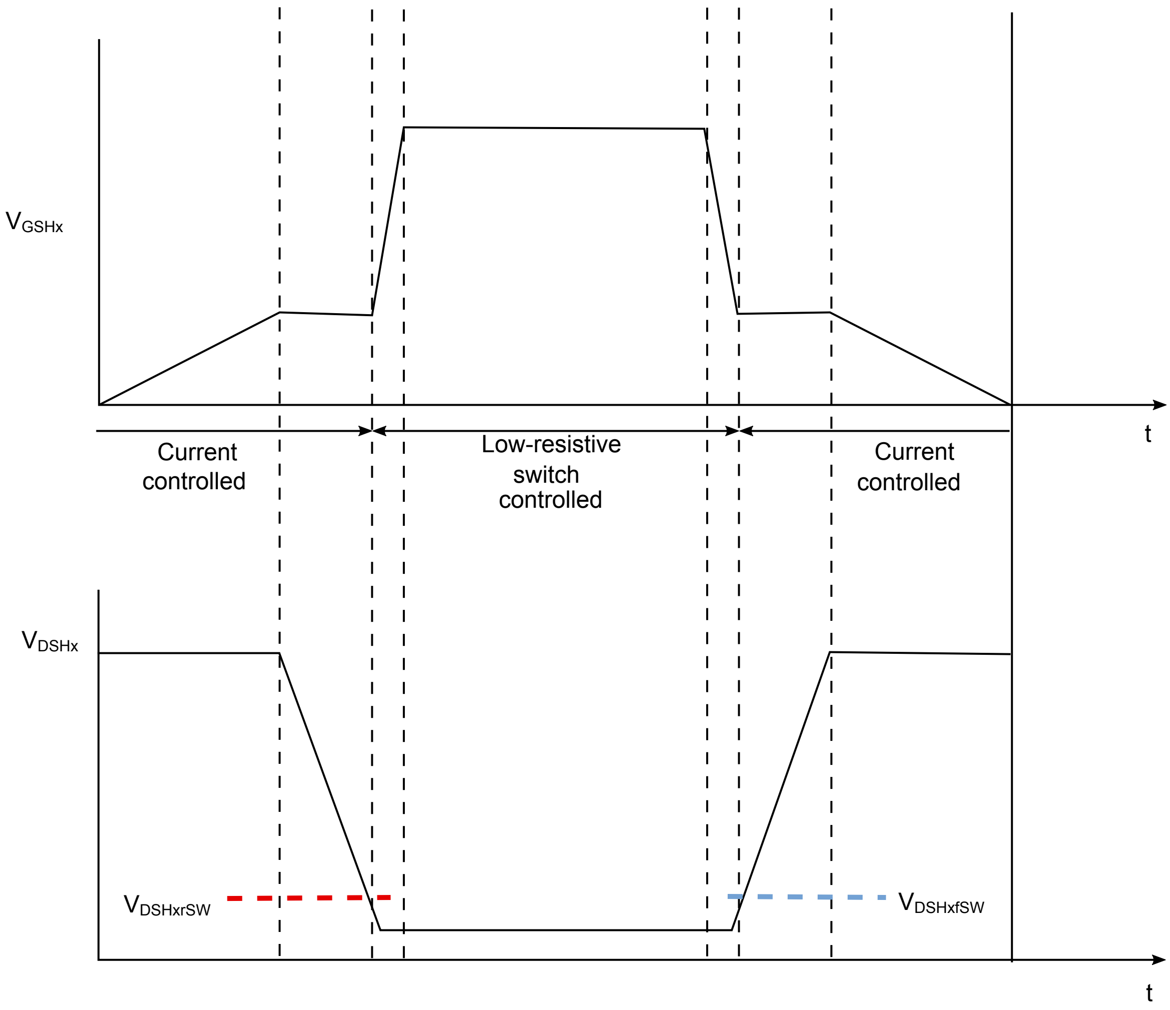
H-bridge is forced off during long open window until watchdog kicks in short window, keeping control bits accessible in the meanwhile.

3.25 H-bridge driver slew rate control

The rising and falling slope of the drivers for the external high-side Power MOSFET can be slew rate controlled. If this mode is enabled the gate of the external high-side Power MOSFET is driven by a current source instead of a low impedance output driver switch as long as the drain-source voltage over this Power MOSFET is above the switch threshold. The current is programmed using the bits SLEW<4:0>, which represent a binary number. This number is multiplied by the minimum current step. This minimum current step is the maximum source/sink current ($I_{GHxrmax}$/$I_{GHxfmax}$) divided by 31. Programming SLEW<4:0> to 0 disables the slew rate control and the output is driven by the low impedance output driver switch.

Note: *To avoid crosscurrent conduction, it must be avoided the usage of the lowest slew rate configurations.*

Figure 31. Half bridge GSHx slope



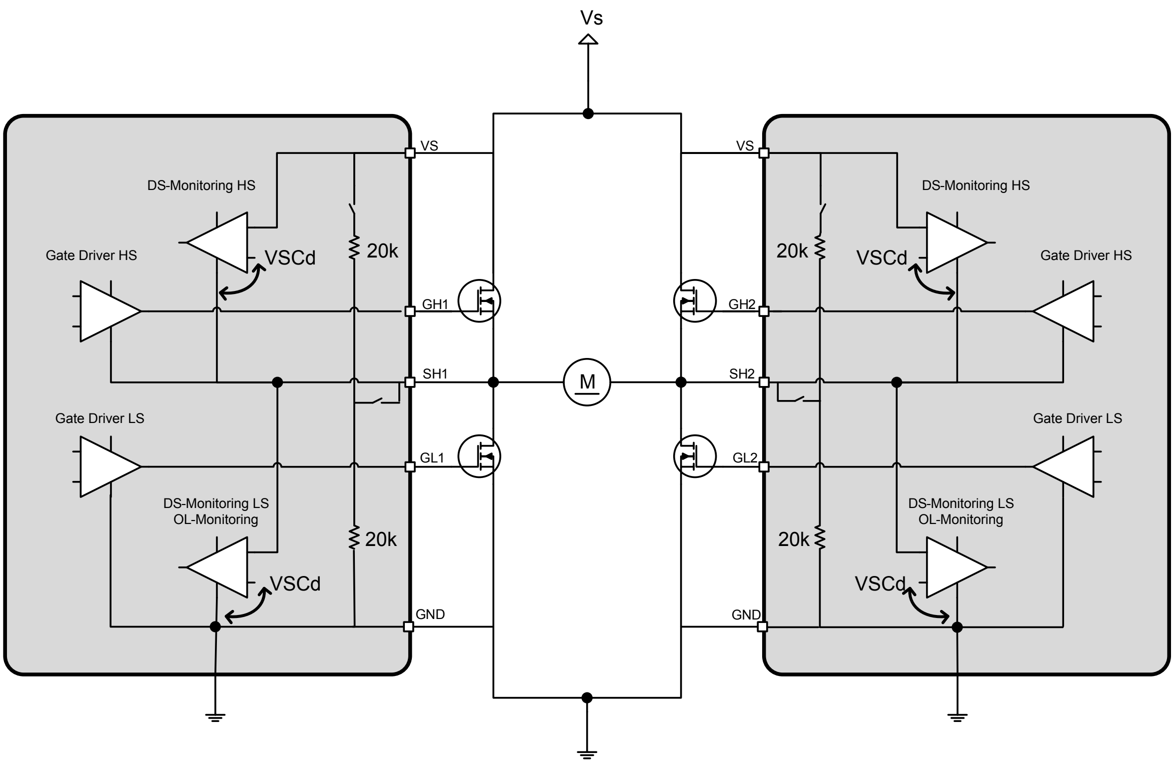
3.26 Resistive low

The resistive output mode protects the device and the H-bridge in the standby mode and in some failure modes (thermal shutdown (TSD), charge pump low (CP_LOW, see also undervoltage setting described in Section 3.12.1: VS supply failure) and stuck at ‘1’ at DI pin). When a gate driver changes into the resistive output mode due to a failure a sequence is started. In this sequence the concerning driver is switched into sink condition for 32 μs to 64 μs to ensure a fast switch off of the H-bridge transistor. If slew rate control is enabled, the sink condition is slew rate controlled. Afterwards the driver is switched into the resistive output mode (resistive path to source).

3.27 Short-circuit detection/ drain-source monitoring

The drain-source voltage of each activated external Power MOSFET of the H-bridge is monitored by comparators to detect shorts to ground or battery. If the voltage drop over the external Power MOSFET exceeds the threshold voltage V_{SCd} for longer than the short current detection time t_{SCd} plus the comparator settling time t_{scs}, the corresponding gate driver switches the external Power MOSFET off and the corresponding drain-source monitoring flag (DS MON LS1, DS MON LS2, DS MON HS1, DS MON HS2) is set. The DSMON_x bits have to be cleared through the SPI to reactivate the gate drivers. This monitoring is only active while the corresponding gate driver is activated. If a drain-source monitor event is detected (in Table 59. H-bridge monitoring in off mode is generically indicated as DS=1, meaning an OR among all four DSMON bits), the corresponding gate driver remains activated for at maximum the filter time t_{SCd} plus comparator settling time t_{SCs}. The threshold voltage V_{SCd} can be programmed using the SPI.

Figure 32. **H-bridge diagnosis**



3.28 H-bridge monitoring in OFF mode

The drain-source voltages of the H-bridge driver external transistors can be monitored, while the transistors are switched off. If either bit OL_H1L2 (CR12) or OL_H2L1 (CR12) is set to ‘1’, while bit HEN (CR 18) = ‘1’, the H-drivers enter resistive low mode and the drain-source voltages can be monitored. Since the pull-up resistance is equal to the pull-down resistance on both sides of the bridge a voltage of 2/3VS on the pull-up high-side and 1/3VS on the low-side is expected, if they drive a low-resistive inductive load (for example motor). If the drain-source voltage on each of these Power MOSFET is less than 1/6 VS, the drain-source monitor bit of the associated driver is set. In off-mode monitoring DSMON_HS1 and DSMON_HS2 are not used and set to 0, being relevant only DSMON_LS1and DSMON_LS2. In case of a short to ground the drain-source monitor bits of both low-side gate drivers are set. A short to V_S can be diagnosed by setting the “H-bridge OL high threshold (H OLTH High)” bit to one. The open-load filter time (t_{fOL}) is 2 ms typical.

Figure 33. H-bridge off state diagnosis (no open-load detected)

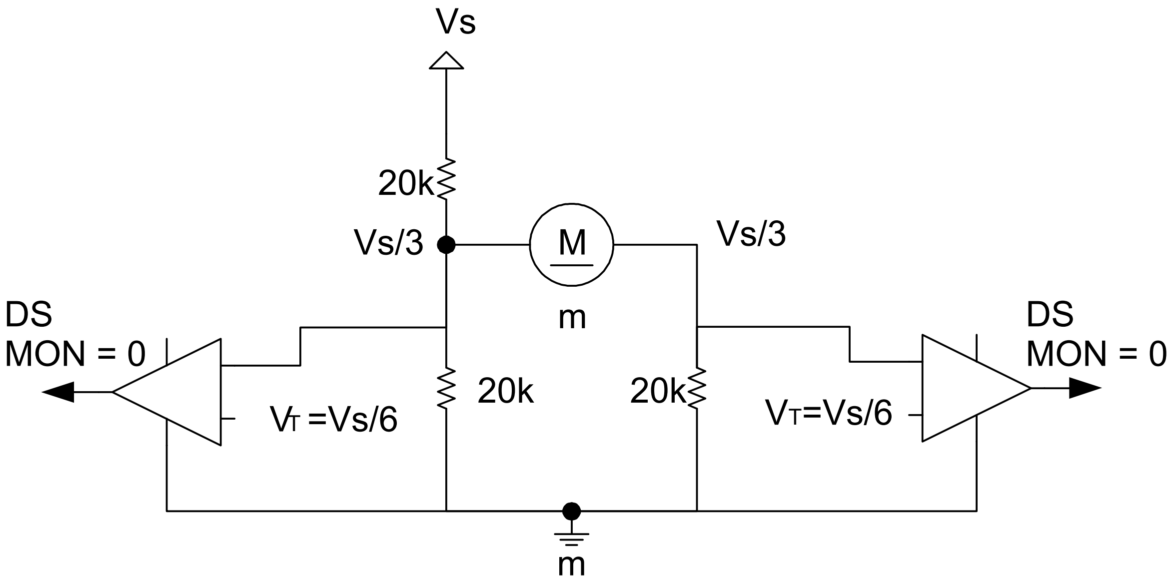


Figure 34. H-bridge off state diagnosis (open-load detected)

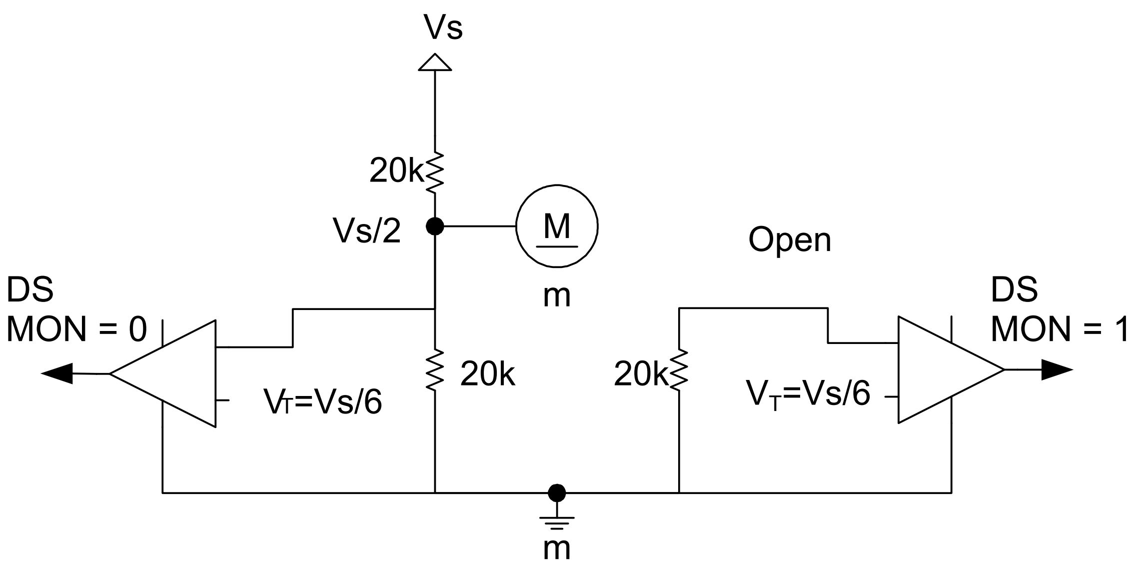


Figure 35. H-bridge off state diagnosis (short to ground detected)

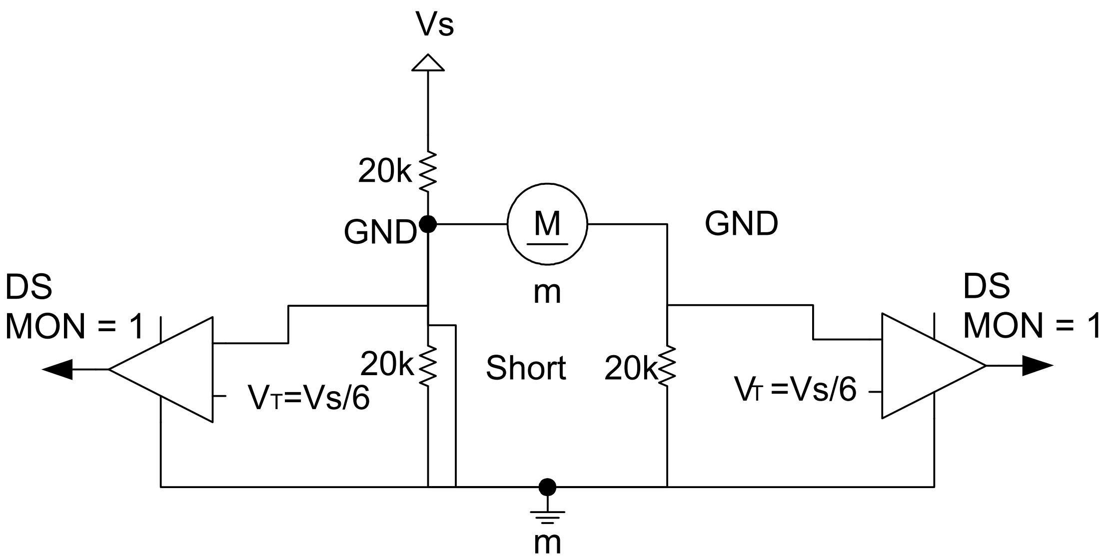
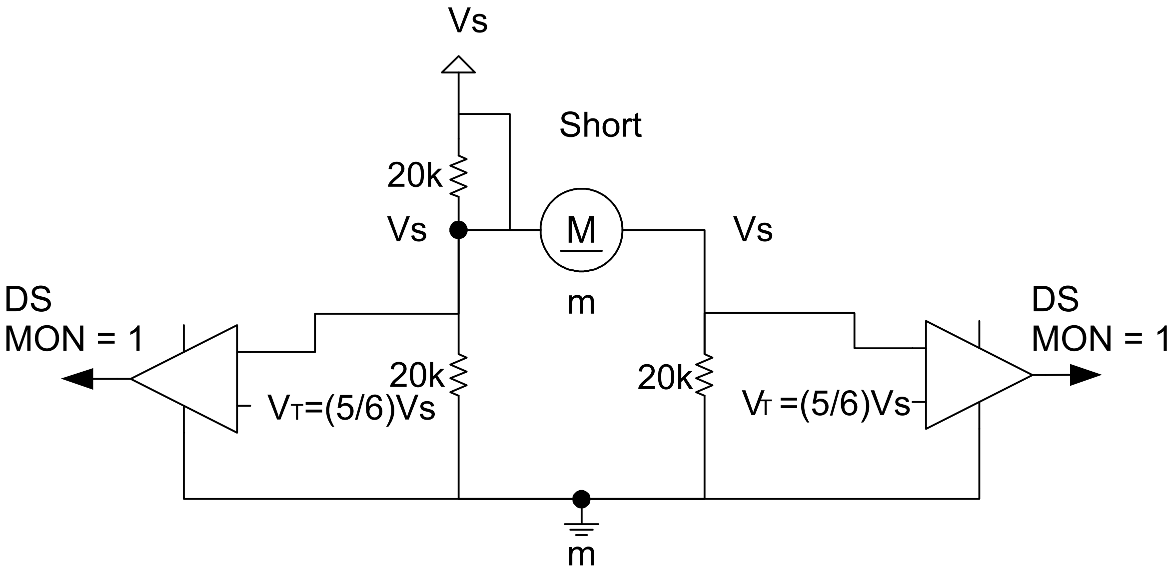


Figure 36. H-bridge off state diagnosis (short to Vs detected)



In this specific case (H_OLTH_high = 1) the outputs of the 2 comparators are inverted to be compliant to Table 58. H-bridge control truth table (Nb = 5 and 9).

Table 59. **H-bridge monitoring in off mode**

Nb	Control bits			Failure bits		Comments
	OL H1L2	OL H2L1	H OLTH High	DSMON LS1	DSMON LS2	
1	0	0	0	0	0	Drain-source monitor disabled
2	1	0	x	0	0	No open-load detected
3	1	0	0	0	1	Open-load
4	1	0	0	1	1	Short to GND
5	1	0	1	1	1	Short to VS
6	0	1	x	0	0	No open-load detected
7	0	1	0	1	0	Open-load
8	0	1	0	1	1	Short to GND
9	0	1	1	1	1	Short to VS

3.29 Programmable cross current solution

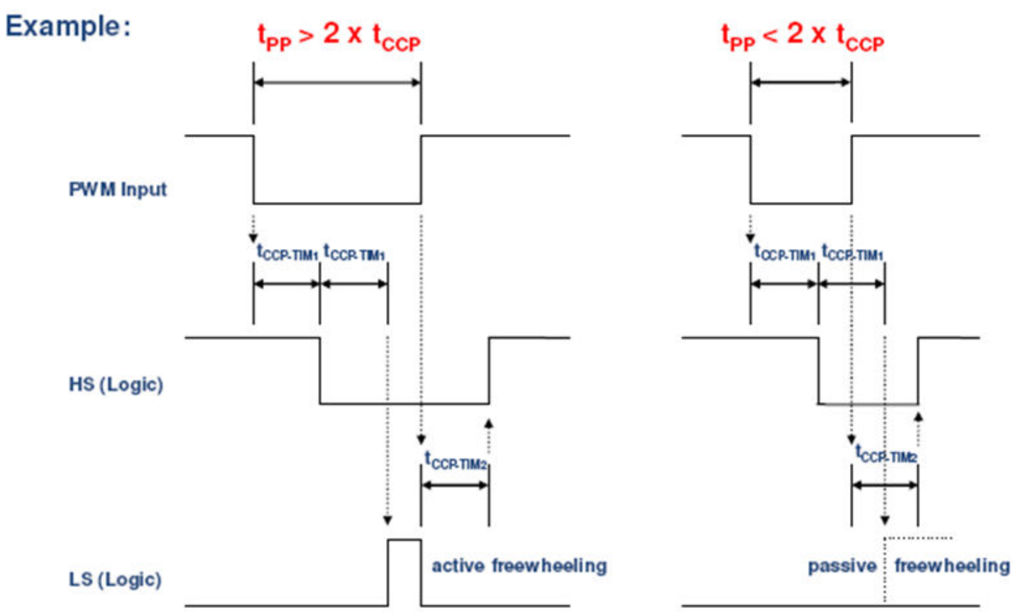
The external Power MOSFETs transistors in H-bridge (two half bridges) configuration are switched on with an additional delay time t_{CCP} to prevent cross current in the half bridge. The cross current protection time t_{CCP} can be programmed with the SPI using bits COPT<3:0> (CR12). The timer is started when the gate driver is switched on in the device.

The PWMH module has 2 timers to configure locking time for high-side and freewheeling low-side.

The programmable time $t_{CCP\text{-}TIM1/CCP\text{-}TIM2}$ is the same. Sequence for switching in PWM mode is as follows:

- HS switches off after locking $t_{CCP\text{-}TIM1}$
- LS switches on after 2nd locking $t_{CCP\text{-}TIM1}$
- HS switches on after locking $t_{CCP\text{-}TIM2}$ which starts with rising edge on PWMH input

Figure 37. **PWMH cross current protection time implementation**



3.30 Heater Power MOSFET driver

The heater Power MOSFET driver stage is controlled by control bit (GH on/off). The driver contains two diagnosis features to indicate SC in active mode (external Power MOSFET switched on) and OL in off state (external Power MOSFET switched off).

Short circuit detection in ON state is realized by monitoring the drain-source voltage of the activated external Power MOSFET by a comparator to detect a SC of SHheater to ground. If the voltage-drop over the external Power MOSFET exceeds the programmed threshold voltage (V_{SCdx}) for longer than the drain-source monitor filter time (t_{SCdx}) the gate driver switches off the external Power MOSFET and the corresponding drain-source monitoring flag DSMON_HEAT(SR6) is set. The drain-source monitoring bit has to be cleared by SPI to reactivate the gate driver. The drain-source monitoring is only active while the gate driver is activated. If a drain-source monitor event is detected, the gate-driver remains activated for the maximum filter time. The threshold voltage can be programmed using the SPI bits GH_THx (CR12).

Open-load detection in off state is realized by monitoring the voltage difference between SHheater and GND and supplying SHheater by a pull-up current source that can be controlled by the SPI bit GH_OL_EN (CR12). When no load is connected to the external Power MOSFET source, the voltage is pulled to VS and in case of exceeding the threshold VOLheater for a time longer than the open-load filter time TOL the open-load bit GH_OL (SR5) is set.

A 15 kΩ resistor is present to discharge the gate capacitor of the external Power MOSFET.

In case of VS undervoltage, behavior and settings are also described in Section 3.12.1: VS supply failure.

Figure 38. Heater Power MOSFET open-load and short-circuit to GND detection

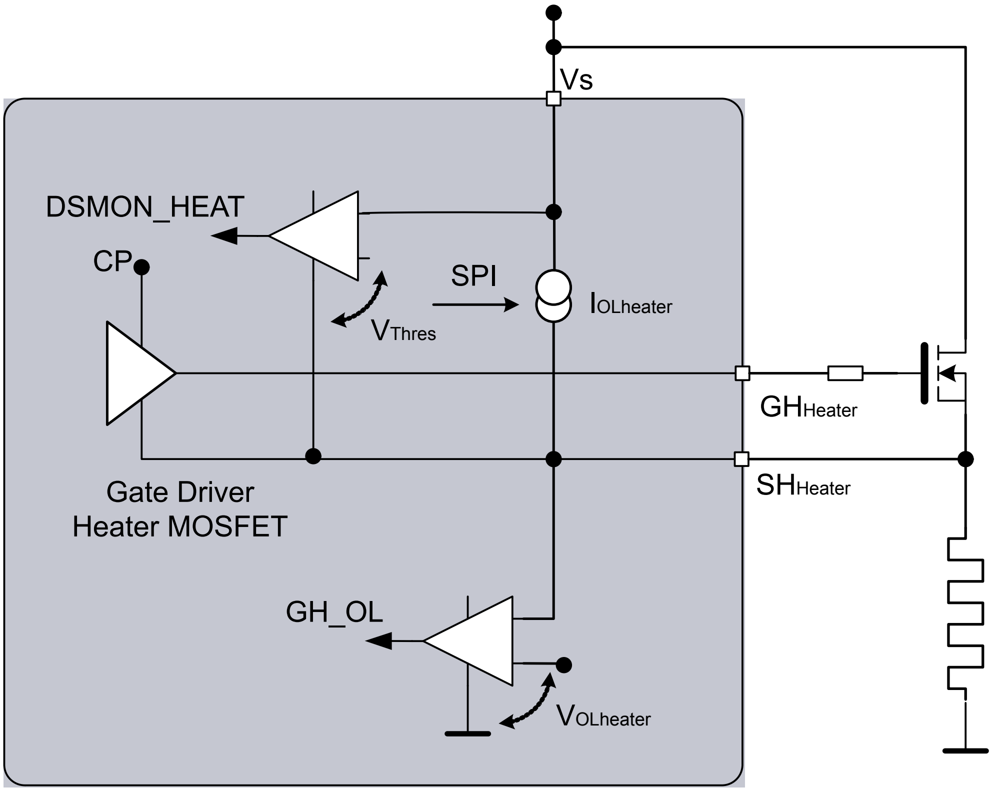


Table 60. **Heater Power MOSFET control truth table**

Nb	Control bit	Failure bits					Output pin	Comment
	GH ON/OFF	CP_LOW	VS_OV	VS_UV	DS	TSD1	GHheater	
1	x	1	x	x	x	x	RL	Charge pump voltage too low
2	x	0	x	x	x	1	RL	Thermal shutdown
3	x	0	1	x	x	0	RL	Overload
4	1	0	0	x	1	0	RL	Short-circuit condition
5	x	0	0	1	0	0	RL	Undervoltage
6	1	0	0	0	0	0	H	Heater Power MOSFET driver enabled
7	0	0	0	0	0	0	RL	Heater Power MOSFET driver disabled

Note: RL = resistive low, H = active high.

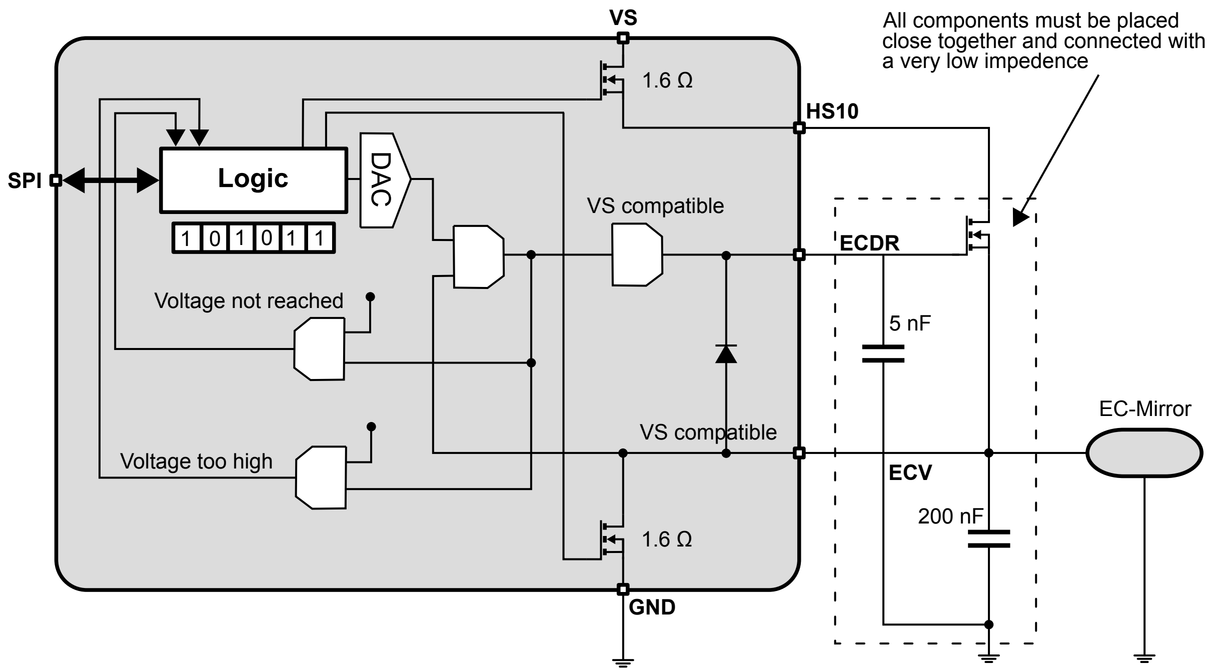
3.31 Control of electrochromic glass

The voltage of an electrochromic element connected at pin ECV can be controlled to a target value, which is set by the bits EC_x<5:0> (CR11). Setting bit ECON (CR11) enables this function. A control loop enables the driving of the electro-chrome mirror voltage on pin ECV thanks to an on-chip differential amplifier and to an external Power MOSFET source follower with its gate connected to pin ECDR. The drain of the external Power MOSFET transistor (the recommended one is STD17NF03L) is supplied by HS10. A diode from pin ECV (anode) to pin ECDR (cathode) has been placed on the chip to protect the external Power MOSFET source follower. A capacitor of at least 5 nF has to be added to pin ECDR for loop stability.

The target voltage is binary coded with a full-scale range of 1.5 V. If Bit ECV HV is set to 0, the maximum controller output voltage is clamped to 1.2 V without changing the resolution of bits EC_x<5:0>. When programming the ECV low-side driver ECV_LS (CR11) to on-state, the voltage at pin ECV is pulled to ground by a 1.6 Ω low-side switch until the voltage at pin ECV is less than d_{VECVhi} higher than the target voltage (fast discharge). The status of the voltage control loop is reported via SPI. Bit ECV_VHI (SR4) is set, if the voltage at pin ECV is higher, whereas Bit ECV_VNR (SR4) is set, if the voltage at pin ECV is lower than the target value. Both status bits are valid, if they are stable for at least the ECVHI/ECVNR filter time and are not latched. Since HS10 is the output of a high-side driver, it contains the same diagnose functions as the other high-side drivers (for example during an overcurrent detection, the control loop is switched off). Also, ECV overcurrent and open-load are monitored through ECV_OC and ECV_OL in SR6 and SR5. In particular, open-load of electro chrome can be also detected by HS10 OL when ECON and HS10 are enabled1. In case of failure detection on HS10_OC; UV; OV, but in general when HS10 is switched off, the ECHR DAC control register is forced to 00000 and DAC code is reprogrammed another time (details of overvoltage and undervoltage behavior are reported in Section 3.12: Power supply fail).

In electrochrome mode, HS10 cannot be controlled by PWM mode. For EMS reasons, the loop capacitor at pin ECDR as well as the capacitor between ECV and GND have to be placed to the respective pins as close as possible (see Figure 39. Electrochrome control block).

Figure 39. Electrochrome control block



Pin ECDR is pulled resistively ($R_{ECDRDIS}$) to ground while not in electro chrome mode. Otherwise, when EC<5:0>=0, it is digitally controlled through the ECV_LS bit.

Note: It is possible to detect an OL on HS10 between the transition of HS10 driver enable and ECON enable. In this case external MOSFET is OFF so there is no current inside HS10 (HS10 OL bit has to be cleared after ECON enable).

3.32 Temperature warning and shutdown

If any of the cluster (see Section 3.33: Digital thermal clusters) junction temperatures rise above the temperature warning threshold (T_{jTW}), a temperature warning flag is set after the temperature warning filter time (t_{fTjTW}) and can be read via SPI. If the junction temperature increases above the temperature shutdown threshold (T_{jTS}), the thermal shutdown bit is set and the power transistors of all output stages are switched off to protect the device after the thermal shutdown filter time. The gates of the H-bridge and the heater MOSFET are discharged by the ‘resistive low’ mode. The temperature warning and thermal shutdown flags are latched and must be cleared by the microcontroller. This is done by a read and clear command on an arbitrary register, because both bits are part of the global status register (TSD1 is bit 4 in SR 8 while TW is in bit 8 in SR 7).

After these bits have been cleared, the output stages are reactivated. If the temperature is still above the thermal warning threshold, the thermal warning bit is set after t_{fTjTW}. Once this bit is set, and the temperature is still above the shutdown threshold, temperature shutdown is detected after t_{fTjTW} and the outputs are switched off. Therefore, the minimum time after which the outputs are switched off in this case, is twice the thermo warning/ thermo shutdown filter time t_{fTjTW}.

3.33 Digital thermal clusters

In order to provide an advanced on chip temperature control, the power outputs are grouped in eight clusters with dedicated thermal sensors. The sensors are suitably located on the device (see Figure 40. Digital thermal clusters identification). In case the temperature of an output cluster reaches the thermal shutdown threshold, the outputs assigned to this cluster are shutdown (all other outputs remain active). Each output cluster has a dedicated temperature warning and shutdown flag (SR1 and SR2). Hence, the thermal cluster concept allows to identify a group of outputs in which one or more channels are in the overload condition.

Thermal clusters can be configured using the bit TSD_CLUSTER_EN (CR3):

- Standard mode (default): as soon as any cluster reaches thermal threshold the device is switched off. V1 regulator remains on and it is switched off reaching TSD2. All the thermal sensors are put in “OR”. In fact, if one of these sensors reaches TSD1:
  - All outputs drivers, charge-pump and V2 are turned OFF
  - V1 remains on until TSD2
  - LIN and CAN transmitters are turned OFF (but they are forced in "receive only" mode)
- Cluster mode: only the cluster that reaches shutdown temperature is switched off.
  In case cluster Th_CL7 reaches TSD1:
  - HS0, HS15, V2 are turned OFF
  - V1 remains ON until TSD2

  In case cluster Th_CL8 reaches TSD1:
  - all outputs drivers, charge pump and V2 are turned OFF
  - V1 remains on until TSD2
  - LIN and CAN transmitters are turned OFF (they are forced in "receive only" mode)

Figure 40. Digital thermal clusters identification

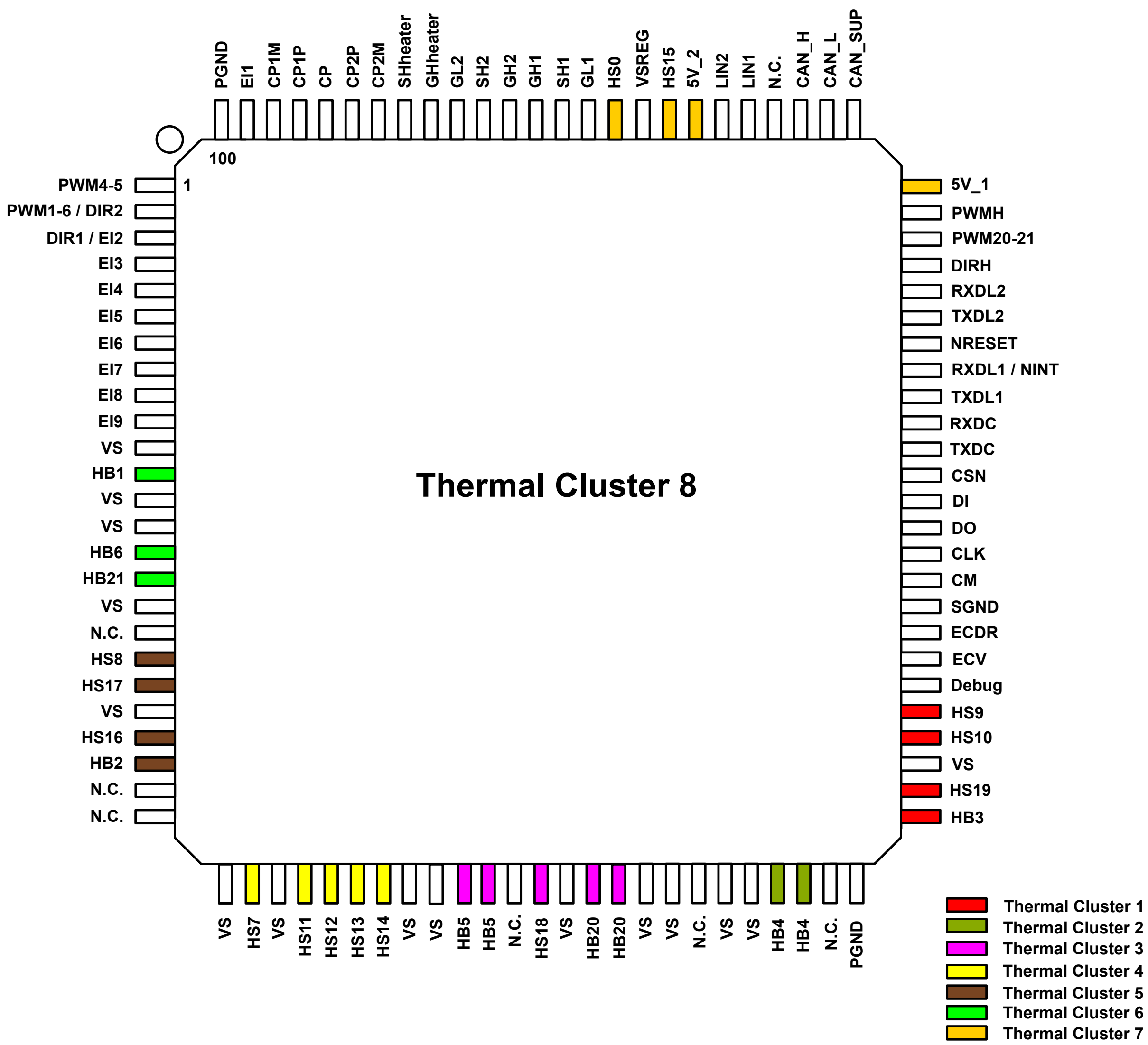


Table 61. Digital thermal clusters definition

Th_CL1	Th_CL2	Th_CL3	Th_CL4	Th_CL5	Th_CL6	Th_CL7	Th_CL8
HB3 HS9-HS10 HS19	HB4	HB5 HS18, HB20	HS7 HS11-HS14	HB2 HS8 HS16, HS17	HB1 HB6 HB21	VREG 1 VREG 2 HS15 HS0	Global
TW & TSD1	TW & TSD1	TW & TSD1	TW & TSD1	TW & TSD1	TW & TSD1	TW &TSD1. TSD2 for VREG1 only (1)	TW, TSD1

1. *In default V1_Standby mode, only TSD2 is available for this cluster.*

4 Serial peripheral interface (SPI)

A 32-bit SPI is used for bidirectional communication with the microcontroller.

The SPI is driven by a microcontroller with its SPI peripheral running in the following mode:

CPOL = 0 and CPHA = 0.

For this mode input data is sampled by the low to high transition of the clock CLK, and output data is changed from the high to low transition of CLK.

This device is not limited to microcontroller with a built-in SPI. Only three CMOS compatible output pins and one input pin are needed to communicate with the device. A fault condition can be detected by setting CSN to low. If CSN = 0, the DO-pin reflects the global error flag (fault condition) of the device.

Chip select not (CSN)

The input pin is used to select the serial interface of this device. When CSN is high, the output pin (DO) is in high impedance state. A low signal activates the output driver and a serial communication can be started. The state during CSN = 0 is called a communication frame.

If CSN = low for $t > t_{CSNfail}$ the DO output is switched to high impedance in order to not block the signal line for other SPI nodes.

Serial data in (DI)

The input pin is used to transfer data serial into the device. The data applied to the DI is sampled at the rising edge of the CLK signal and shifted into an internal 32-bit shift register. At the rising edge of the CSN signal the content of the shift register is transferred to the data input register. The writing to the selected data input register is only enabled if exactly 32 bits are transmitted within one communication frame (that is CSN low). If more or less clock pulses are counted within one frame the complete frame is ignored. This safety function is implemented to avoid an activation of the output stages by a wrong communication frame.

Note: due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected IC's is recommended.

Serial data out (DO)

The data output driver is activated by a logical low level at the CSN input and go from high impedance to a low or high level depending on the global error flag (fault condition). The first rising edge of the CLK input after a high to low transition of the CSN pin transfers the content of the selected status register into the data out shift register. Each subsequent falling edge of the CLK shifts the next bit out.

Serial clock (CLK)

The CLK input is used to synchronize the input and output serial bit streams. The data input (DI) is sampled at the rising edge of the CLK and the data output (DO) changes with the falling edge of the CLK signal. The SPI can be driven with a CLK frequency up to 4 MHz.

4.1 ST SPI 4.0

The ST SPI is a standard used in ST Automotive ASSP devices.

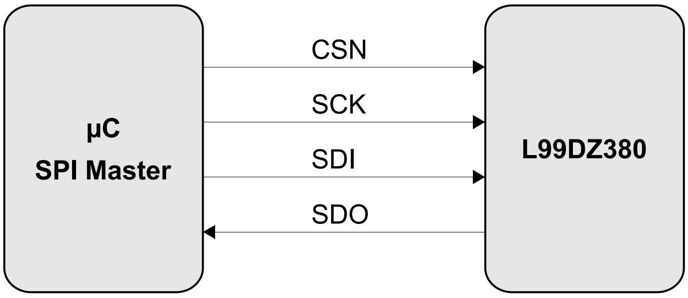
This chapter describes the SPI protocol standardization. It defines a common structure of the communication frames and defines specific addresses for product and status information.

The ST SPI allows the usage of generic software to operate the devices while maintaining the required flexibility to adapt it to the individual functionality of a particular product. In addition, failsafe mechanisms are implemented to protect the communication from external influences and a wrong or unwanted usage.

The device serial peripheral interface is compliant to the ST SPI standard rev. 4.0.

4.1.1 Physical layer

Figure 41. SPI pin description



4.2 Signal description

- **Chip select not (CSN)**

The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame is sent. During communication start and stop the serial clock (SCK) has to be logically low. The serial data out (SDO) is in high impedance when CSN is high or a communication timeout was detected.

- **Serial clock (SCK)**

This SCK provides the clock of the SPI. Data present at serial data input (SDI) is latched on the rising edge of serial clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to serial data out (SDO).

- **Serial data input (SDI)**

This input is used to transfer data serially into the device. Data is latched on the rising edge of serial clock (SCK).

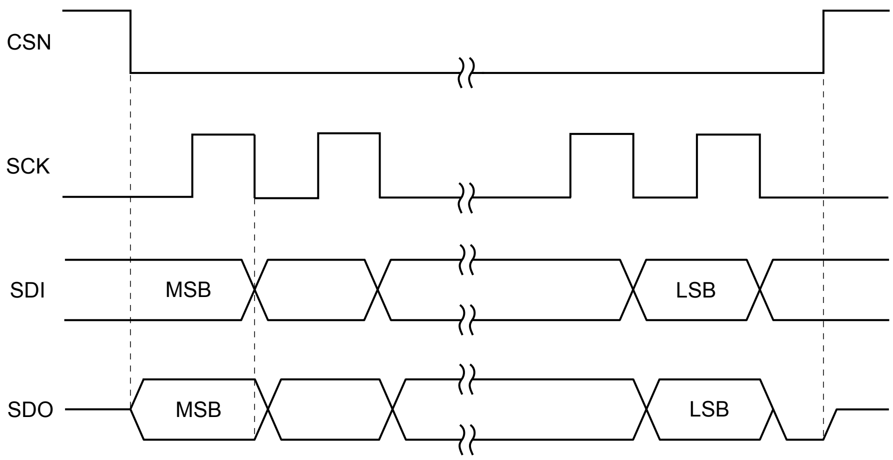
- **Serial data output (SDO)**

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of serial clock (SCK).

4.2.1 Clock and data characteristics

The ST SPI can be driven by a microcontroller with its SPI peripheral running in the following mode:

Figure 42. SPI signal description



The communication frame starts with the falling edge of the CSN (communication start). SCK has to be low.

The SDI data is then latched at all the following rising SCK edges into the internal shift registers.

After communication start the SDO leaves 3-state mode and presents the MSB of the data shifted out to SDO. At all the following falling SCK edges data is shifted out through the internal shift registers to SDO.

The communication frame is finished with the rising edge of CSN. If a valid communication takes place (for example a correct number of SCK cycles, access to a valid address), the requested operation according to the operating code is performed (write or clear operation).

4.2.2 Communication protocol

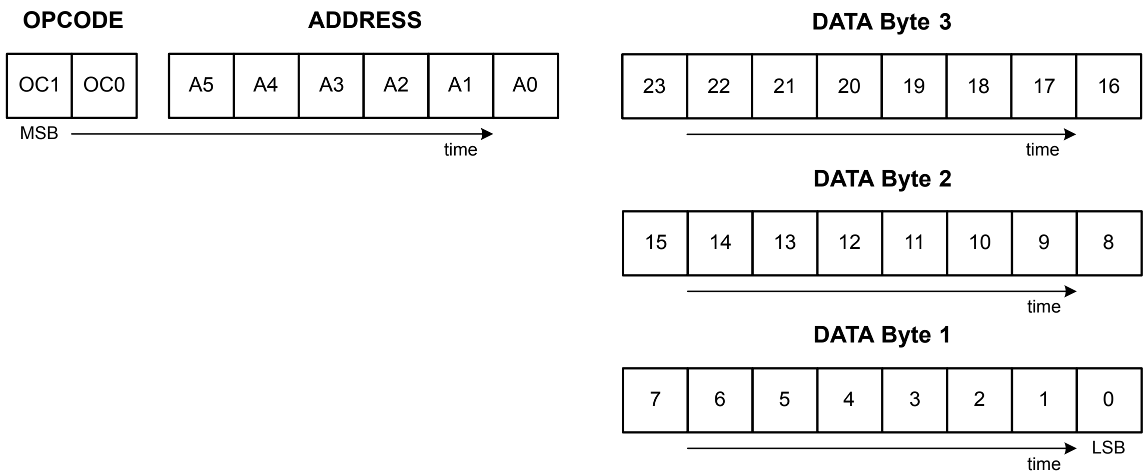
SDI frame

The devices data in the frame consists of 32 bits (OpCode (2 bits) + address (6 bits) + data byte 3 + data byte 2 + data byte 1).

The first two transmitted bits (MSB, MSB-1) contain the operation code that represents the instruction that is performed. The following 6 bits (MSB-2 to MSB-7) represent the address on which the operation is performed.

The subsequent bytes contain the payload.

Figure 43. SDI frame



Operating code

The operating code is used to distinguish between different access modes to the registers of the slave device.

Table 62. Operation codes

OC1	OC0	Description
0	0	Write operation
0	1	Read operation
1	0	Read and clear operation
1	1	Read device information

A "Write operation" leads to a modification of the addressed data by the payload if a write access is allowed (for example, control register, valid data). Besides this, a shift out of the registers content (data present at the communication start) is performed.

A "Read operation" shifts out the data present in the addressed register at the communication start. The payload data is ignored and internal data is not modified. In addition, a burst read can be performed.

A "Read and clear operation" leads to a clear of addressed status bits. The bits to be cleared are defined first by address, second by payload bits set to ‘1’. Besides this, a shift out of the registers content (data present at the communication start) is performed.

Note: Status registers that change status during communication could be cleared by the actual read and clear operation and are not reported in actual communication or in the following communications. To avoid a loss of any reported status, it is recommended just to clear the status registers that are already reported in the previous communication (selective bitwise clear).

Advanced operation codes

To provide besides the separate write of all the control registers and the bitwise clear of all the status registers, two advanced operation codes can be used to set all the control registers to the default value and to clear all the status registers

A 'set all control registers to default' command is performed when an OpCode ‘11’ at address b’111111 is performed.

Note: Consider that potential device specific write-protected registers cannot be cleared with this command as therefore a device power-on reset is needed.

A ‘clear all status registers’ command is performed when an OpCode ‘10’ at address b’111111 is performed.

Data in payload

The payload (data byte 1 to data byte 3) is the data transferred to the device with every SPI communication. The payload always follows the OpCode and the address bits.

For write access the payload represents the new data written to the addressed register. For read and clear operations the payload defines which bit of the addressed status register is cleared. In the case of a ‘1’ at the corresponding bit position the bit is cleared.

For a read operation the payload is not used. For functional safety reasons it is recommended to set the unused payload to ‘0’.

SDO frame

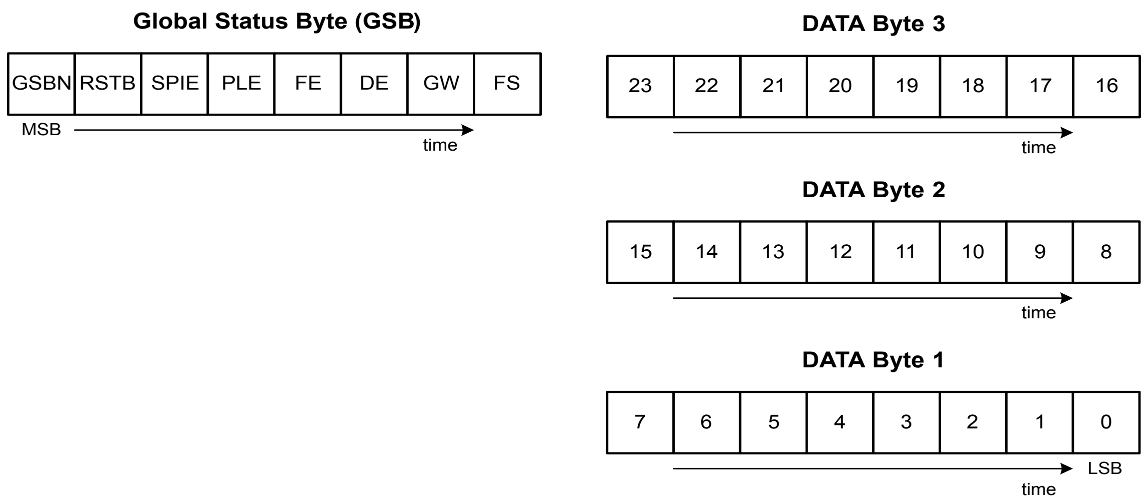
The data out frame consists of 32 bits (GSB + data bytes 1 to 3).

The first eight transmitted bits contain the device-related status information and are latched into the shift register at the time of the communication starts. These 8 bits are transmitted at every SPI transaction.

The subsequent bytes contain the payload data and are latched into the shift register with the eight positive SCK edges.

This could lead to an inconsistency of data between the GSB and the payload due to different shift register load times. Anyway, no unwanted status register clear should appear, as status information should just be cleared with a dedicated bit clear.

Figure 44. SDO frame



Global status byte (GSB)

The bits (Bit 0 to Bit 4) represent a logical OR combination of bits located in the status registers. Therefore, no direct read & clear can be performed on these bits inside the GSB.

Table 63. **Global status byte**

Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS

Global status bit not (GSBN)

The GSBN is a logical NOR combination of Bit 24 to Bit 30. This bit can also be used as a global status flag without starting a complete communication frame as it is present directly after pulling CSN low.

- **Reset bit (RSTB)**

The RSTB indicates a device reset. In case this bit is set, specific internal control registers are set to default and kept in that state until the bit is cleared.

The RSTB bit is cleared after a read and clear of all the specific bits in the status registers that caused the reset event.

- **SPI error (SPIE)**

The SPIE is a logical OR combination of errors related to a wrong SPI communication.

- **Physical layer error (PLE)**

The PLE is a logical OR combination of errors related to the LIN and CAN FD transceivers.

- **Functional error (FE)**

The FE is a logical OR combination of errors coming from functional blocks (for example high-side overcurrent).

- **Device error (DE)**

The DE is a logical OR combination of errors related to device specific blocks (for example VS overvoltage, over temperature).

- **Global warning (GW)**

The GW is a logical OR combination of warning flags (for example thermal warning).

- **Fail-safe (FS)**

The FS bit indicates that the device was forced into a safe state due to mistreatment or fundamental internal errors (for example watchdog failure, voltage regulator failure).

Data out payload

The payload (data bytes 1 to 3) is the data transferred from the slave device with every SPI communication to the master device. The payload always follows the OpCode and the address bits of the actual shifted in data (in frame response).

4.2.3 Address definition

Table 64. **Address definition - device application access**

Device application access	
Operating code	
OC1	OC0
0	0
0	1
1	0

Table 65. **Address definition - device information read access**

Device information read access	
Operating code	
OC1	OC0
1	1

Table 66. Address definition - RAM access

RAM address	Description	Access
3FH	Configuration register	R/W
...	...	...
3DH	Status register 13	R/C
...	...	
32H	Status register 2	R/C
31H	Status register 1	R/C
...	...	
22H	Control register 34	R/W
1DH	Control register 29	R/W
...	...	
02H	Control register 2	R/W
01H	Control register 1	R/W
00H	Reserved	

Table 67. Address definition - ROM access

ROM Address	Description	Access
3FH	<Advanced op.>	W
3EH	<GSB options>	R
...		
20H	<SPI CPHA test>	R
16H	<WD bit pos. 4>	R
15H	<WD bit pos. 3>	R
14H	<WD bit pos. 2>	R
13H	<WD bit pos. 1>	R
12H	<WD type 2>	R
11H	<WD type 1>	R
10H	<SPI mode>	R
...		
0AH	<Silicon ver.>	R
...		
05H	<Device n.4>	R
04H	<Device n.3>	R
03H	<Device n.2>	R
02H	<Device n.1>	R
01H	<Device family>	R
00H	<Company code>	R

Information registers

The device information registers can be read by using OpCode ‘11’. After shifting out the GSB the 8-bit wide payload is transmitted. By reading device information registers a communication width which is minimum 16 bits plus a multiple by 8 can be used. After shifting out the GSB followed by the 8-bit wide payload a series of ‘0’ is shifted out at the SDO.

Table 68. L99DZ380 information register map

ROM address	Description	Access	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FH	<Advanced op.>									
3EH	<GSB options>	R	0	0	0	0	0	0	0	0
…										
20H	<SPI CPHA test>	R	0	1	0	1	0	1	0	1
16H	<WD bit pos. 4>	R	C0H							
15H	<WD bit pos. 3>	R	7FH							
14H	<WD bit pos. 2>	R	C0H							
13H	<WD bit pos. 1>	R	66H							
12H	<WD type 2>	R	91H							
11H	<WD type 1>	R	3CH							
10H	<SPI mode>	R	B0H							
…										
0AH	<Silicon ver.>	R	major revision				minor revision			
…										
05H	<Device n.4>	R	44H							
04H	<Device n.3>	R	35H							
03H	<Device n.2>	R	52H							
02H	<Device n.1>	R	44H							
01H	<Device family>	R	01H							
00H	<Company code>	R	00H							

Device identification registers

These registers represent a unique signature to identify the device and silicon version.

<Company code>: 00H (STMicroelectronics)

<Device family>: 01H (BCD power management)

<Device n. 1>: 44H (ASCII code for D)

<Device n. 2>: 52H (ASCII code for R)

<Device n. 3>: 35H (ASCII code for 5)

<Device n. 4>: 44H (ASCII code for D)

SPI modes

By reading out the <SPI mode> register general information of SPI usage of the device application registers can be read.

Table 69. SPI mode registers

Bit7	Bit6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit0
BR	DL2	DL1	DL0	0	0	S1	S0
1	0	1	1	0	0	0	0

<SPI mode>: B0H (burst mode read available, 32-bit, no data consistency check)

SPI burst read

Table 70. Burst read bit

Bit 7	Description
0	BR not available
1	BR available

The SPI burst read bit indicates if a burst read operation is implemented. The intention of a burst read is for example used to perform a device internal memory dump to the SPI master.

The start of the burst read is like a normal read operation. The difference is that after the SPI data length the CSN is not pulled high and the SCK is continuously clocked. When the normal SCK max count is reached (SPI data length) the consecutive addressed data is latched into the shift register. This procedure is performed every time when the SCK payload length is reached.

In case the automatic incremented address is not used by the device, undefined data is shifted out. An automatic address overflow is implemented when address 3FH is reached.

The SPI burst read is limited by the CSN low timeout.

SPI data length

The SPI data length value indicates the length of the SCK count monitor which is running for all accesses to the device application registers. In case a communication frame with an SCK count is not equal to the reported one it will lead to a SPI error and the data will be rejected.

Table 71. SPI data length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	Invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
0	1	1	32-bit SPI
1	1	1	64-bit SPI

Table 72. Data consistency check (parity-check)

Bit 1	Bit 0	Description
S1	S0	
0	0	Not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

Watchdog definition

(see also Section 2.4.7: Watchdog)

In case a watchdog is implemented the default settings can be read out via the device information registers.

Table 73. WD type/timing

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WD1	WD0						
<WD type 1/2>	0	0			Register is not used			

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
<WD type 1>	0	1	WT5	WT4	WT3	WT2	WT1	WT0
		1	1	1	1	1	0	0
			Watchdog timeout/long open window WT[5:0] * 5 ms					
<WD type 2>	1	0	OW2	OW1	OW0	CW2	CW1	CW0
	1	0	0	1	0	0	0	1
			Open window OW[2:0] *			Closed window CW[2:0] *		
				5 ms			5 ms	
<WD type 1/2>	1	1	Invalid					

<WD type 1>: 3CH (long open window: 300 ms)

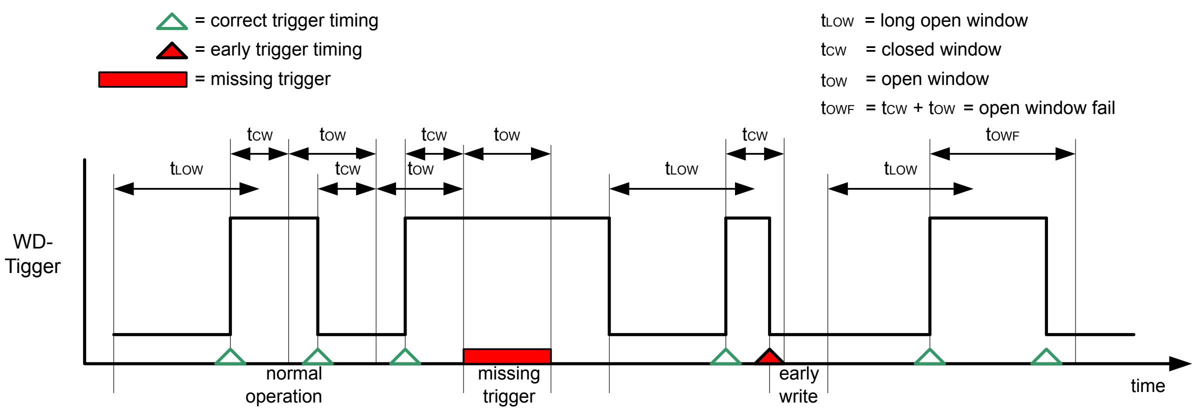
<WD type 2>: 91H (open window: 10 ms, closed window: 5 ms)

<WD type 1> indicates the long open window (timeout) which is opened at the start of the watchdog. The binary value of WT [5:0] times 5 ms indicates the typical value of the timeout time.

<WD type 2> describes the default timing of the window watchdog.

The binary value of CW [2:0] times 5 ms defines the typical closed window time (t_{CW}) and OW [2:0] times 5 ms defines the typical open window time (t_{OW}). See Figure 45. Window watchdog operation, which recalls with Figure 3. Watchdog timing $t_{CW} = T_{EFW}$ and $t_{OW} = T_{LFW} - T_{EFW}$

Figure 45. Window watchdog operation



The watchdog trigger bit location is defined by the <WD bit pos. X> registers.

Table 74. WD bit position

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	WB1	WB0						
<WD bit pos. X>	0	0			Register is not used			
<WD bit pos. X>	0	1	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
<WD bit pos. 1>	0	1	0	0	0	0	0	1
<WD bit pos. 3>	0	1	1	1	1	1	1	1
			Defines the register addresses of the WD trigger bits					
<WD bit pos. X>	1	0	WBA5	WBA4	WBA3	WBA2	WBA1	WBA0
			Defines the stop address of the address range (previous<WD bit pos. X> is a WB = ‘01’). The consecutive <WD bitpos. X> has to be a WB = ‘11’					
<WD bit pos. X>	1	1	0	WBP 4	WBP3	WBP2	WBP1	WBP0
<WD bit pos. 2>	1	1	0	0	0	0	0	0
<WD bit pos. 4>	1	1	0	0	0	0	0	0
				Defines the binary bit position of the WD trigger				
					bit within the register			

<WD bit pos 1>: 41H; watchdog trigger bit located at address 01H (CR18)

<WD bit pos 2>: C0H; watchdog trigger bit location is bit0

<WD bit pos 3>: 7FH; watchdog trigger bit located at address 3FH (CR1)

<WD bit pos 4>: C0H; watchdog trigger bit location is bit0

Device application registers (DAR)

The device application registers are all accessible using OpCode ‘00’, ‘01’ and ‘10’. The functions of these registers are defined in the device specification.

4.2.4 Protocol failure detection

To realize a protocol which covers certain failsafe requirements a basic set of failure detection mechanisms is implemented.

Clock monitor

During communication (CSN low to high phase) a clock monitor counts the valid SCK clock edges. If the SCK edges do not correlate with the SPI data length an SPIE is reported with the next command and the actual communication is rejected.

By accessing the device information registers (OpCode = ‘11’) the clock monitor is set to a minimum of 16 SCK edges plus a multiple by 8 (for example 16, 25, 32, ...).

Providing no SCK edge during a CSN low to high phase is not recognized as a SPIE. For a SPI burst read also the SPI data length plus multiple numbers of payloads SCK edges are assumed as a valid communication.

SCK polarity (CPOL) check

To detect the wrong polarity access via SCK the internal clock monitor is used. Providing first a negative edge on SCK during communication (CSN low to high phase) or a positive edge at last leads to an SPI error reported in the next communication and the actual data is rejected.

SCK phase (CPHA) check

To verify, that the SCK Phase of the SPI master is set correctly a special device information register is implemented. By reading this register the data must be 55 H. In case AAH is read the CPHA setting of the SPI master is wrong and a proper communication cannot be guaranteed.

CSN timeout

By pulling CSN low the SDO is set active and leaves its tristate condition. To ensure communication between other SPI devices within the same bus even in case of CSN stuck at low a CSN timeout is implemented. By pulling CSN low an internal timer is started. After timer end is reached the actual communication is rejected and the SDO is set to tristate condition.

SDI stuck at GND

As a communication with data all -'0' and OpCode '00' on address b'000000 cannot be distinguished between a valid command and a SDI stuck at GND this communication is not allowed. Nevertheless, in case a stuck at GND is detected the communication is rejected and the SPIE is set with the next communication.

SDI stuck at HIGH

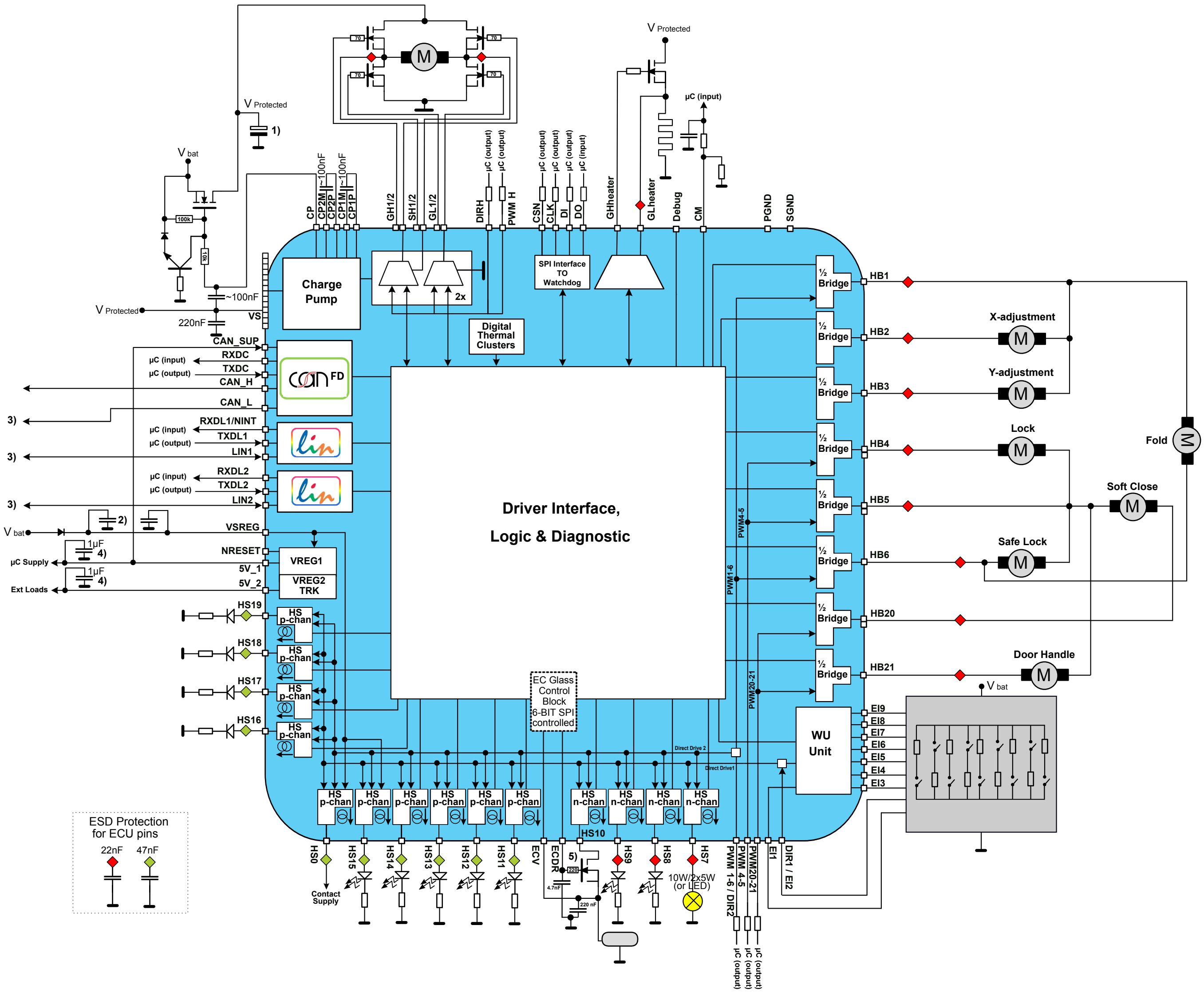
As a communication with data all -'1' and OpCode '11' on address b'111111 cannot be distinguished between a valid command and a SDI stuck at HIGH this communication is not allowed. In case a stuck at HIGH is detected the communication is rejected and the SPIE is set with the next communication.

SDO stuck at

The SDO stuck at GND and stuck at HIGH has to be detected by the SPI master. As the definition of the GSB guarantees at least one toggle, a GSB with all -'0' or all -'1' reports a stuck at error.

5 Application circuit

Figure 46. Application circuit



1) Capacitance to be dimensioned according to load current (rule of thumb 500µF each 10A)
2) Capacitance to be dimensioned e.g. according to voltage drop out requirements
3) OEM requirements and external components for LIN resp CAN to be fulfilled.
4) For EMC optimization purposes, capacitance could be redimensioned (2.2µF recommended)
5) Optional resistance may be needed for improving stability; value has to be selected according to external EC circuitry. A suitable range is between 120 .. 220 Ω

6 SPI Registers

6.1 Global status byte (GSB)

Table 75. **Global status byte (GSB)**

Global status byte (GSB)							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
1 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)	0 (R)
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS
Global status bit inverted	Reset	SPI error	Physical layer error (CAN,LIN)	Functional error	Device error	Global warning	Fail-safe

Table 76. **Global status byte (GSB) description**

Bit	Name	Description
31	GSBN	**Global status bit inverted** The GSBN is a logically NOR combination of GSB Bits 24 to Bit 30 [1]. This bit can also be used as global status flag without starting a complete communication frame as it is present at SDO directly after pulling CSN low. 0 = error detected (1 or several GSB bits from 24 to 30 are set) 1 = no error detected (default after Power on)
30	RSTB	**Reset** The RSTB indicates a device reset and is set in case of the following events: SR8 (0x8) • VPOR • WDFAIL • V1UV (when UV is more than 16 µs) • FORCED_SLEEP_TSD2_V1SC 0 = no reset signal has been generated (default) 1 = Reset signal has been generated RSTB is cleared by a read & clear command to all bits in status register 8 causing the reset event.
29	SPIE [2]	**SPI error bit** The SPIE indicates errors related to a wrong SPI communication. SR7 (0x7) • SPI_INV_CMD • SPI_SCK_CNT The bit is also set in case of an SPI CSN Time-out detection 0 = no error (default) 1 = error detected
28	PLE[2]	**Physical layer error** The PLE is a logical OR combination of errors related to the LIN and CAN transceivers. SR7 (0x7): • LIN_PERM_DOM • LIN_TXD_DOM • LIN_PERM_REC • CAN_RXD_REC • CAN_PERM_REC • CAN_PERM_DOM

Bit	Name	Description
		• CAN_TXD_DOM 0 = no error (default) 1 = error detected PLE is cleared by a read & clear command to all related bits in status registers 7.
27	FE	**Functional error bit** The FE is a logical OR combination of errors coming from functional blocks. SR7 (0x7): • V2SC • DSMONx SR6 (0x6): • HSx_OC (x = 0, 7, .., 15) • HBx_LS_OC / HBx_HS_OC (x = 1, .., 6) • ECV_OC • DSMON_HEAT SR5 (0x5)[(3)]: • HSx_OL (x = 0, 7, .., 15) • HBx_LS_OL / HBx_HS_OL (x = 1, .., 6) • ECV_OL • GH_OL 0 = no error (default) 1 = error detected FE is cleared by a read & clear command to all related bits in status registers 5, 6, 7
26	DE	**Device error bit** DE is a logical OR combination of global errors related to the device. SR8 (0x8): • TSD1 SR7 (0x7): • VS_OV • VS_UV • VSREG_OV • VSREG_UV • CP_LOW 0 = no error (default) 1 = error detected DE is cleared by a read and clear command to all related bits in status registers 7 and 8
25	GW [(2)]	**Global warning bit** GW is a logical OR combination of warning flags. Warning bits do not lead to any device state change or switch OFF of functions. SR7 (0x7): • V1FAIL • V2FAIL • CAN_RXD_REC • TW [(3)] • SPI_INV_CMD • SPI_SCK_CNT SR3 (0x3): • CAN_SUP_LOW 0 = no error (default) 1 = error detected GW is cleared by a read & clear command to all related bits in status registers 7 and 3.

Bit	Name	Description
24	FS	**Fail-safe** The FS bit indicates the device was forced into a safe state due to the following failure conditions: SR8 (0x8): • WDFAIL • V1UV(when UV is more than 2 ms) • TSD2 • FORCED_SLEEP_TSD2_V1SC SR3 (0x03): • SGNDLOSS All control registers are set to default Control registers are blocked for WRITE access except the following bits: CR18 (0x3F): • TRIG • CAN_ACT CR17 (0x3E): • Timer settings (bits 8…21) CR14 (0x3B): • HS15_x (bits 8…11) • HS0_x (bits 12…15) CR5 (0x32) to CR10 (0x37) • PWM frequency and duty cycles CR1 (0x26) • V2_0 • V2_1 0 = failsafe inactive (default) 1 = failsafe active FS is cleared upon exit from failsafe mode (refer to chapter Section 3.7: Fail-safe mode)

1. *Individual failure flags may be masked in the CR1 (0x26).*
2. *Bit may be masked in the CR1 (0x26), that is the bit is not included in the global status bit (GSB).*
3. *The open-load status flags may be masked in the CR1 (0x26), that is the open-load flag is included in the FE flag but it does not set the GSB. TW failure status flags may be masked in the CR1 (0x26), that is the TW flag is included in the GW flag, but it does not set the GSB.*

6.2 Control registers overview

Table 77. Global control registers

Bit								Mode
31	30	29	28	27	26	25	24	
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS	R

Table 78. Control registers overview

Addr./ DZ380	CR#	Bits	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0	Mode
0x26	CR1	MSB	CAN_LOOP_EN	LIN_TXD_TOUT	LIN_WU_CONFIG	-	ECV_HV	DISABLE_CP_DITH	ICMP_CONFIG_EN	WD_CONFIG_EN	R/W
			MASK_OL_HS1	MASK_OL_LS1	MASK_TW	MASK_EC_OL	MASK_OL	MASK_SPIE	MASK_PLE	MASK_GW	
		LSB	CP_OFF_EN	-	-	CAN_AUTO_BIAS	DIR1_EN	V2_1	V2_0	TRIG	
0x27	CR2	MSB	-	-	-	-	-	-	-	-	R/W
			-	-	-	-	-	-	-	-	
		LSB	-	PWM1-6_1	PWM1-6_0	PWM4-5_1	PWM4-5_0	CP_OFF	ICMP	-	
0x28	CR21	MSB	-	-	-	-	-	-	-	-	R/W
			-	-	-	-	-	-	-	-	
		LSB	-	-	-	-	PWM21	PWM20	-	-	
0x29	CR22	MSB	-	-	PWM14DC_9	PWM14DC_8	PWM14DC_7	PWM14DC_6	PWM14DC_5	PWM14DC_4	R/W
			PWM14DC_3	PWM14DC_2	PWM14DC_1	PWM14DC_0	-	-	PWM13DC_9	PWM13DC_8	
		LSB	PWM13DC_7	PWM13DC_6	PWM13DC_5	PWM13DC_4	PWM13DC_3	PWM13DC_2	PWM13DC_1	PWM13DC_0	
0x2A	CR23	MSB	-	-	PWM12DC_9	PWM12DC_8	PWM12DC_7	PWM12DC_6	PWM12DC_5	PWM12DC_4	R/W
			PWM12DC_3	PWM12DC_2	PWM12DC_1	PWM12DC_0	-	-	PWM11DC_9	PWM11DC_8	
		LSB	PWM11DC_7	PWM11DC_6	PWM11DC_5	PWM11DC_4	PWM11DC_3	PWM11DC_2	PWM11DC_1	PWM11DC_0	
0x2B	CR24	MSB	-	-	-	-	-	-	-	-	R/W
			-	-	-	-	-	-	-	-	
		LSB	-	-	-	-	PWM14FREQ	PWM13FREQ	PWM12FREQ	PWM11FREQ	
0x2C	CR3	MSB	-	-	-	TSD_CLUSTER_EN	-	-	-	-	R/W

Addr./ DZ380	CR#	Bits	23 15 7	22 14 6	21 13 5	20 12 4	19 11 3	18 10 2	17 9 1	16 8 0	Mode
0x2C	CR3		-	-	HS0_CCM	-	-	-	-	HS15_CCM	R/W
		LSB	HS14_CCM	HS13_CCM	HS12_CCM	HS11_CCM	HS10_CCM	HS9_CCM	HS8_CCM	HS7_CCM	
0x2D	CR31	MSB	-	-	HB21OCR	HB20OCR	HB21HS	HB21LS	HB20HS	HB20LS	R/W
			-	HS19_2	HS19_1	HS19_0	-	HS18_2	HS18_1	HS18_0	
		LSB	-	HS17_2	HS17_1	HS17_0	-	HS16_2	HS16_1	HS16_0	
0x2E	CR32	MSB	-	-	-	-	-	LIN2_TXD_TOUT_EN	LIN2_WU_CONFIG	-	R/W
			-	-	-	-	-	-	-	-	
		LSB	-	EI9_PU	EI8_PU	EI7_PU	EI6_PU	EI5_PU	EI4_PU	EI3_PU	
0x2F	CR33	MSB	LIN2_WU_EN	EI9_EN	EI8_EN	EI7_EN	EI6_EN	EI5_EN	EI4_EN	EI3_EN	R/W
			-	-	EI9_FILT_1	EI9_FILT_0	EI8_FILT_1	EI8_FILT_0	EI7_FILT_1	EI7_FILT_0	
		LSB	EI6_FILT_1	EI6_FILT_0	EI5_FILT_1	EI5_FILT_0	EI4_FILT_1	EI4_FILT_0	EI3_FILT_1	EI3_FILT_0	
0x30	CR4	MSB	-	-	-	-	-	-	-	-	R/W
			-	-	-	-	HS7_OCR_TON_1	HS7_OCR_TON_0	HS_OCR_TON_1	HS_OCR_TON_0	
		LSB	HB_OCR_TON_1	HB_OCR_TON_0	HS7_OCR_FREQ_1	HS7_OCR_FREQ_0	HS_OCR_FREQ_1	HS_OCR_FREQ_0	HB_OCR_FREQ_1	HB_OCR_FREQ_0	
0x32	CR5	MSB	-	-	PWM9_DC_9	PWM9_DC_8	PWM9_DC_7	PWM9_DC_6	PWM9_DC_5	PWM9_DC_4	R/W
			PWM9_DC_3	PWM9_DC_2	PWM9_DC_1	PWM9_DC_0	-	-	PWM10_DC_9	PWM10_DC_8	
		LSB	PWM10_DC_7	PWM10_DC_6	PWM10_DC_5	PWM10_DC_4	PWM10_DC_3	PWM10_DC_2	PWM10_DC_1	PWM10_DC_0	
0x33	CR6	MSB	-	-	PWM7_DC_9	PWM7_DC_8	PWM7_DC_7	PWM7_DC_6	PWM7_DC_5	PWM7_DC_4	R/W
			PWM7_DC_3	PWM7_DC_2	PWM7_DC_1	PWM7_DC_0	-	-	PWM8_DC_9	PWM8_DC_8	
		LSB	PWM8_DC_7	PWM8_DC_6	PWM8_DC_5	PWM8_DC_4	PWM8_DC_3	PWM8_DC_2	PWM8_DC_1	PWM8_DC_0	
0x34	CR7	MSB	-	-	PWM5_DC_9	PWM5_DC_8	PWM5_DC_7	PWM5_DC_6	PWM5_DC_5	PWM5_DC_4	R/W
			PWM5_DC_3	PWM5_DC_2	PWM5_DC_1	PWM5_DC_0	-	-	PWM6_DC_9	PWM6_DC_8	
		LSB	PWM6_DC_7	PWM6_DC_6	PWM6_DC_5	PWM6_DC_4	PWM6_DC_3	PWM6_DC_2	PWM6_DC_1	PWM6_DC_0	
0x35	CR8	MSB	-	-	PWM3_DC_9	PWM3_DC_8	PWM3_DC_7	PWM3_DC_6	PWM3_DC_5	PWM3_DC_4	R/W
			PWM3_DC_3	PWM3_DC_2	PWM3_DC_1	PWM3_DC_0	-	-	PWM4_DC_9	PWM4_DC_8	
		LSB	PWM4_DC_7	PWM4_DC_6	PWM4_DC_5	PWM4_DC_4	PWM4_DC_3	PWM4_DC_2	PWM4_DC_1	PWM4_DC_0	
0x36	CR9	MSB	-	-	PWM1_DC_9	PWM1_DC_8	PWM1_DC_7	PWM1_DC_6	PWM1_DC_5	PWM1_DC_4	R/W

Addr./ DZ380	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x36	CR9		PWM1_DC_3	PWM1_DC_2	PWM1_DC_1	PWM1_DC_0	-	-	PWM2_DC_9	PWM2_DC_8	R/W
		LSB	PWM2_DC_7	PWM2_DC_6	PWM2_DC_5	PWM2_DC_4	PWM2_DC_3	PWM2_DC_2	PWM2_DC_1	PWM2_DC_0	
0x37	CR10	MSB	-	-	-	-	-	-	-	-	R/W
			-	-	-	-	-	-	PWM10_FREQ	PWM9_FREQ	
		LSB	PWM8_FREQ	PWM7_FREQ	PWM6_FREQ	PWM5_FREQ	PWM4_FREQ	PWM3_FREQ	PWM2_FREQ	PWM1_FREQ	
0x38	CR11	MSB	-	-	-	-	-	-	-	-	R/W
			-	-	ECV_LS	ECV_OCR	-	-	-	ECON	
		LSB	-	-	EC_5	EC_4	EC_3	EC_2	EC_1	EC_0	
0x39	CR12	MSB	-	DIAG_1	DIAG_0	GH_OL_EN	GH	GH_TH_3	GH_TH_2	GH_TH_1	R/W
			GH_TH_0	SD	SDS	DM	COPT_3	COPT_2	COPT_1	COPT_0	
		LSB	H_OLTH_HIGH	OL_H1L2	OL_H2L1	SLEW_4	SLEW_3	SLEW_2	SLEW_1	SLEW_0	
0x3A	CR13	MSB	HS7_RDSON	-	-	-	-	-	HS10_OCR	HS9_OCR	R/W
			HS8_OCR	HS7_OCR	HB6_OCR	HB5_OCR	HB4_OCR	HB3_OCR	HB2_OCR	HB1_OCR	
		LSB	-	-	CM	CM_SEL_4	CM_SEL_3	CM_SEL_2	CM_SEL_1	CM_SEL_0	
0x3B	CR14	MSB	-	-	-	-	-	-	-	-	R/W
			HS0_3	HS0_2	HS0_1	HS0_0	HS15_3	HS15_2	HS15_1	HS15_0	
		LSB	HS14_3	HS14_2	HS14_1	HS14_0	HS13_3	HS13_2	HS13_1	HS13_0	
0x3C	CR15	MSB	HS12_3	HS12_2	HS12_1	HS12_0	HS11_3	HS11_2	HS11_1	HS11_0	R/W
			HS10_3	HS10_2	HS10_1	HS10_0	HS9_3	HS9_2	HS9_1	HS9_0	
		LSB	HS8_3	HS8_2	HS8_1	HS8_0	HS7_3	HS7_2	HS7_1	HS7_0	
0x3D	CR16	MSB	VSREG_LOCK_ ENA	VS_LOCK_ENA	VSREG_OV_SD _ENA	VSREG_UV_SD_ ENA	VS_OV_SD_ENA	VS_UV_SD_ENA	HB6OCTH_1	HB6OCTH_0	R/W
			HB5OCTH_1	HB5OCTH_0	HB1OCTH_1	HB1OCTH_0	HB6_HS	HB6_LS	HB5_HS	HB5_LS	
		LSB	HB4_HS	HB4_LS	HB3_HS	HB3_LS	HB2_HS	HB2_LS	HB1_HS	HB1_LS	
0x3E	CR17	MSB	-	-	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	R/W
			-	-	T1_ON_2	T1_ON_1	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	
		LSB	V1_RESET_1	V1_RESET_0	-	WD_TIME	-	-	STBY_SEL	GO_STBY	
0x3F	CR18	MSB	EI2_PU	-	-	EI1_PU	EI2_EN	-	-	EI1_EN	R/W
			EI2_FILT_1	EI2_FILT_0	-	-	-	-	EI1_FILT_1	EI1_FILT_0	

Addr./ DZ380	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x3F	CR18	LSB	HEN	CAN_REC_ONLY	CAN_ACT	LIN_WU_EN	CAN_WU_EN	TIMER_NINT_WAKE_SEL	TIMER_NINT_EN	TRIG	R/W

6.3 Status register overview

Table 79. Global status registers

Bit								Mode
31	30	29	28	27	26	25	24	
GSBN	RSTB	SPIE	PLE	FE	DE	GW	FS	R

Table 80. Status registers overview

Addr./ DZ380	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x01	SR1	MSB	TW_CL8	TW_CL7	TW_CL6	TW_CL5	TW_CL4	TW_CL3	TW_CL2	TW_CL1	R
			HB21_LS_SC	HB20_LS_SC	HB6_LS_SC	HB5_LS_SC	HB4_LS_SC	HB3_LS_SC	HB2_LS_SC	HB1_LS_SC	
		LSB	HS19_OL	HS18_OL	HS17_OL	HS16_OL	HB21_LS_OL	HB21_HS_OL	HB20_LS_OL	HB20_HS_OL	
0x02	SR2	MSB	TSD1_CL8	TSD1_CL7	TSD1_CL6	TSD1_CL5	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1	R
			HB21_HS_SC	HB20_HS_SC	HB6_HS_SC	HB5_HS_SC	HB4_HS_SC	HB3_HS_SC	HB2_HS_SC	HB1_HS_SC	
		LSB	HS19_OC	HS18_OC	HS17_OC	HS16_OC	HB21_LS_OC	HB21_HS_OC	HB20_LS_OC	HB20_HS_OC	
0x03	SR3	MSB	WAKE_LIN2	EI9_WAKE	EI8_WAKE	EI7_WAKE	EI6_WAKE	EI5_WAKE	EI4_WAKE	EI3_WAKE	R
			-	EI9_STATE	EI8_STATE	EI7_STATE	EI6_STATE	EI5_STATE	EI4_STATE	EI3_STATE	
		LSB	-	-	SGNDLOSS	IP_SUP_LOW	CAN_SUP_LOW	LIN2_PERM_DOM	LIN2_TXD_DOM	LIN2_PERM_REC	
0x04	SR4	MSB	WD_TIMER_STATE_1	WD_TIMER_STATE_0	EI2_STATE	-	-	EI1_STATE	ECV_VNR	ECV_VHI	R
			-	-	-	-	-	-	-	-	
		LSB	-	-	-	-	-	-	-	-	
0x05	SR5	MSB	ECV_OL	GH_OL	HS0_OL	HS15_OL	HS14_OL	HS13_OL	HS12_OL	HS11_OL	R
			HS10_OL	HS9_OL	HS8_OL	HS7_OL	HB6_LS_OL	HB6_HS_OL	HB5_LS_OL	HB5_HS_OL	
		LSB	HB4_LS_OL	HB4_HS_OL	HB3_LS_OL	HB3_HS_OL	HB2_LS_OL	HB2_HS_OL	HB1_LS_OL	HB1_HS_OL	
0x06	SR6	MSB	ECV_OC	DSMON_HEAT	HS0_OC	HS15_OC	HS14_OC	HS13_OC	HS12_OC	HS11_OC	R
			HS10_OC	HS9_OC	HS8_OC	HS7_OC	HB6_LS_OC	HB6_HS_OC	HB5_LS_OC	HB5_HS_OC	
		LSB	HB4_LS_OC	HB4_HS_OC	HB3_LS_OC	HB3_HS_OC	HB2_LS_OC	HB2_HS_OC	HB1_LS_OC	HB1_HS_OC	
0x07	SR7	MSB	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC	CAN_RXD_REC	CAN_PERM_REC	CAN_PERM_DOM	CAN_TXD_DOM	CANTO	R

Addr./ DZ380	CR#	Bits	23	22	21	20	19	18	17	16	Mode
			15	14	13	12	11	10	9	8	
			7	6	5	4	3	2	1	0	
0x07	SR7		DSMON_HS2	DSMON_HS1	DSMON_LS2	DSMON_LS1	SPI_INV_CMD	SPI_SCK_CNT	CP_LOW	TW	R
		LSB	V2SC	V2FAIL	V1FAIL	-	VSREG_OV	VSREG_UV	VS_OV	VS_UV	
0x08	SR8	MSB	EI2_WAKE	-	-	EI1_WAKE	WAKE_CAN	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	R
			V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	
		LSB	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2_V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR	

6.4 Control registers

6.4.1 Control register 1 (CR1, 0x26)

Table 81. **Control register 1**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	CAN_LOOP_EN	LIN_TXD_TOUT	LIN_WU_CONFIG	RESERVED	ECV_HV	DISABLE_CP_DITH	ICMP_CONFIG_EN	WD_CONFIG_EN	MASK_OL_HS1	MASK_OL_LS1	MASK_TW	MASK_EC_OL	MASK_OL	MASK_SPIE	MASK_PLE	MASK_GW	CP_OFF_EN	RESERVED	RESERVED	CAN_AUTO_BIAS	DIR1_EN	V2_1	V2_0	TRIG
Reset value	0	1	0														1	0			1	0		
Access	RW			R	RW													R		RW				

Table 82. **CR1 signals description**

Bit	Name	Description
23	CAN_LOOP_EN	CAN looping of TXDC to RXDC 0: CAN looping disabled (default) 1: CAN looping enabled
22	LIN_TXD_TOUT	LIN TXD timeout detection 0: LIN TXD timeout detection disabled 1: LIN TXD timeout detection enabled (default)
21	LIN_WU_CONFIG	Configuration of LIN wake-up behavior 0: wake-up at recessive-dominant-recessive with t_dom > 28 µs (default) (according to LIN 2.2a and hardware requirements for transceivers version 1.3) 1: wake-up at recessive-dominant transition
20	RESERVED	-
19	ECV_HV	Electro chrome controller voltage 0: electro chrome controller voltage set to minimum value (default) 1: electro chrome controller voltage set to maximum value
18	DISABLE_CP_DITH	Charge pump dithering 0: charge pump dithering enabled (default) 1: charge pump dithering disabled
17	ICMP_CONFIG_EN	ICMP configuration enable 0: writing ICMP = 1 is blocked (writing ICMP = 0 is possible); (default) 1: writing ICMP = 1 is possible with next SPI command bit is automatically reset to 0 after next SPI command
16	WD_CONFIG_EN	Watchdog configuration enable 0: writing to WD configuration (CR17 [0:1]) is blocked (default) 1: writing to WD configuration bits is possible with next SPI command bit is automatically reset to 0 after next SPI command
15	MASK_OL_HS1	0: open-load condition at HS1 (half bridge HB1) is not masked (default) 1: open-load condition at HS1 (half bridge HB1) is masked that is reported as a functional error (GSB bit 27) but not as a global error (GSB bit 31)
14	MASK_OL_LS1	0: open-load condition at LS1 (half bridge HB1) is not masked (default)

Bit	Name	Description
		1: open load condition at LS1 (half bridge HB1) is masked that is reported as a functional error (GSB bit 27) but not as a global error (GSB bit 31)
13	MASK_TW	0: thermal warning is not masked (default) 1: thermal warning is masked that is reported as a global warning (GSB bit 25) but not as a global error (GSB bit 31)
12	MASK_EC_OL	0: open-load condition at ECV is not masked (default) 1: open-load condition at ECV is masked that is reported as a functional error (GSB bit 27), but not as a global error (GSB bit 31)[1]
11	MASK_OL	0: open-load condition at all outputs are not masked (default) 1: open-load condition at all outputs are masked except HB1 (see bit 14,15 CR1 for HB1) that is reported as a functional error (GSB bit 27), but not as a global error (GSB bit 31)
10	MASK_SPIE	0: SPI errors are not masked (default) 1: SPI errors are masked that are reported as am SPI error (GSB bit 29) but not as a global error (GSB bit 31)
9	MASK_PLE	0: physical layer errors are not masked (default) 1: physical layer errors are masked that are reported as a physical layer error (GSB bit 28) but not as a global error (GSB bit 31)
8	MASK_GW	0: global warning conditions are not masked (default) 1: global warning conditions are masked that are reported as a global warning (GSB bit 25) but not as a global error (GSB bit 31)
7	CP_OFF_EN	Charge pump OFF enable 0: writing CP_OFF = 1 is blocked (writing CP_OFF = 0 is possible) 1: writing CP_OFF = 1 is possible (default)
6	RESERVED	-
5	RESERVED	-
4	CAN_AUTO_BIAS	CAN automatic biasing activation 0: auto biasing disabled (default) 1: auto biasing enabled
3	DIR1_EN	Enable DIR1 input or EI2 0: EI2 configured as wake-up input 1: DIR1 function enabled (default)
2	V2_1	Voltage regulator V2 configuration 00: V2 OFF in all modes (default) 01: V2 ON in active mode; V2 OFF in standby modes 10: V2 ON in active and V1_Standby mode; V2 OFF in VBAT_Standby mode 11: V2 ON in active and V1_Standby mode; V2 OFF in VBAT_Standby mode
1	V2_0	
0	TRIG	Watchdog trigger bit

1. *Open-load condition at HS10 can be masked by writing MASK_OL = 1.*

6.4.2 Control register 2 (CR2, 0x27)

Table 83. **Control register 2**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM1-6_1	PWM1-6_0	PWM4-5_1	PWM4-5_0	CP_OFF	ICMP	RESERVED
Reset value	0																							
Access	R																	RW						R

Table 84. **CR2 signals description**

Bit	Name	Description
23:7	RESERVED	-
6	PWM1-6_1	PWM control for HB1 and HB6
5	PWM1-6_0	**PWM1-6/DIR2 control** 00: PWM1-6 disabled, DIR2 function enabled (default) 01: PWM1-6 applied to HB1 LS 10: PWM1-6 applied to HB6 LS 11: PWM1-6 applied to both HB1 and HB6 low-sides at the same time
4	PWM4-5_1	PWM control for HB4 and HB5
3	PWM4-5_0	**PWM4-5 control** 00: OFF, PWM4-5 not applied (default) 01: PWM4-5 applied to HB4 LS 10: PWM4-5 applied to HB5 LS 11: PWM4-5 applied to both HB4 and HB5 low-sides at the same time
2	CP_OFF	Switch OFF the charge pump 0: charge pump ON (default) 1: charge pump OFF *Note: Setting CP_OFF = 1 is possible only if CP_OFF_EN is set to “1” in CR1.*
1	ICMP	V1 load current supervision 0: enabled; watchdog is disabled in V1_Standby when IV1< ICMP (default) 1: disabled; watchdog is disabled upon transition into V1_Standby mode *Note: Setting ICMP = 1 is only possible when ICMP_CONFIG_EN = 1 in CR1.*
0	RESERVED	-

6.4.3 Control register 21 (CR21, 0x28)

Table 85. Control register 21

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM21	PWM20	RESERVED	RESERVED
Reset value	0																							
Access	R																				RW		R	

Table 86. CR21 signals description

Bit	Name	Description
23:4	RESERVED	-
3	PWM21	PWM control for HB21: 0: PWM21 disabled (default) 1: PWM21 applied to HB21 LS
2	PWM20	PWM control for HB20: 0: PWM20 disabled (default) 1: PWM20 applied to HB20 LS
1:0	RESERVED	-

6.4.4 Control register 22 (CR22, 0x29)

Table 87. Control register 22

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	PWM14_DC_9	PWM14_DC_8	PWM14_DC_7	PWM14_DC_6	PWM14_DC_5	PWM14_DC_4	PWM14_DC_3	PWM14_DC_2	PWM14_DC_1	PWM14_DC_0	RESERVED	RESERVED	PWM13_DC_9	PWM13_DC_8	PWM13_DC_7	PWM13_DC_6	PWM13_DC_5	PWM13_DC_4	PWM13_DC_3	PWM13_DC_2	PWM13_DC_1	PWM13_DC_0
Reset value	0																							
Access	R		RW										R		RW									

Table 88. CR22 signals description

Bit	Name	Description
23:22	RESERVED	-
21	PWM14_DC_9	PWM14_DC_[21:12]: binary coded on-duty cycle of PWM channel PWM14 (see Duty cycle coding for channel PWMx(y))
20	PWM14_DC_8	
19	PWM14_DC_7	
18	PWM14_DC_6	
17	PWM14_DC_5	
16	PWM14_DC_4	
15	PWM14_DC_3	
14	PWM14_DC_2	
13	PWM14_DC_1	
12	PWM14_DC_0	
11:10	RESERVED	-
9	PWM13_DC_9	PWM13_DC_[9:0]: binary coded on-duty cycle of PWM channel PWM13 (see Duty cycle coding for channel PWMx(y))
8	PWM13_DC_8	
7	PWM13_DC_7	
6	PWM13_DC_6	
5	PWM13_DC_5	
4	PWM13_DC_4	
3	PWM13_DC_3	
2	PWM13_DC_2	
1	PWM13_DC_1	
0	PWM13_DC_0	

6.4.5 Control register 23 (CR23, 0x2A)

Table 89. Control register 23

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	PWM12_DC_9	PWM12_DC_8	PWM12_DC_7	PWM12_DC_6	PWM12_DC_5	PWM12_DC_4	PWM12_DC_3	PWM12_DC_2	PWM12_DC_1	PWM12_DC_0	RESERVED	RESERVED	PWM11_DC_9	PWM11_DC_8	PWM11_DC_7	PWM11_DC_6	PWM11_DC_5	PWM11_DC_4	PWM11_DC_3	PWM11_DC_2	PWM11_DC_1	PWM11_DC_0
Reset value	0																							
Access	R		RW										R		RW									

Table 90. CR23 signals description

Bit	Name	Description
23:22	RESERVED	-
21	PWM12_DC_9	PWM12_DC_[21:12]: binary coded on-duty cycle of PWM channel PWM12 (see Duty cycle coding for channel PWMx(y))
20	PWM12_DC_8	
19	PWM12_DC_7	
18	PWM12_DC_6	
17	PWM12_DC_5	
16	PWM12_DC_4	
15	PWM12_DC_3	
14	PWM12_DC_2	
13	PWM12_DC_1	
12	PWM12_DC_0	
11:10	RESERVED	-
9	PWM11_DC_9	PWM11_DC_[9:0]: binary coded on-duty cycle of PWM channel PWM11 (see Duty cycle coding for channel PWMx(y))
8	PWM11_DC_8	
7	PWM11_DC_7	
6	PWM11_DC_6	
5	PWM11_DC_5	
4	PWM11_DC_4	
3	PWM11_DC_3	
2	PWM11_DC_2	
1	PWM11_DC_1	
0	PWM11_DC_0	

6.4.6 Control register 24 (CR24, 0x2B)

Table 91. **Control register 24**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM14_FREQ	PWM13_FREQ	PWM12_FREQ	PWM11_FREQ
Reset value	0								1								0							
Access	R																				RW			

Table 92. **CR24 signals description**

Bit	Name	Description
23:4	RESERVED	-
3	PWM14_FREQ	Select PWM14 frequency: 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
2	PWM13_FREQ	Select PWM13 frequency: 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
1	PWM12_FREQ	Select PWM12 frequency: 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
0	PWM11_FREQ	Select PWM11 frequency: 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz

6.4.7 Control register 3 (CR3, 0x2C)

Table 93. Control register 3

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	TSD_CLUSTER_EN	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	HS0_CCM	RESERVED	RESERVED	RESERVED	RESERVED	HS15_CCM	HS14_CCM	HS13_CCM	HS12_CCM	HS11_CCM	HS10_CCM	HS9_CCM	HS8_CCM	HS7_CCM
Reset value	0																							
Access	R			RW	R						RW	R				RW								

Table 94. CR3 signals description

Bit	Name	Description
23:21	RESERVED	-
20	TSD_CLUSTER_EN	Enables thermal warning and shutdown of outputs by cluster 0: TSD and TW by cluster OFF (default) 1: TSD and TW by cluster ON
19:14	RESERVED	-
13	HS0_CCM	Constant current mode on HS0 enable (1) 0: disabled (default) 1: enabled
12:9	RESERVED	-
8	HS15_CCM	Constant current mode on HS15 enable (1) 0: disabled (default) 1: enabled
7	HS14_CCM	Constant current mode on HS14 enable (1) 0: disabled (default) 1: enabled
6	HS13_CCM	Constant current mode on HS13 enable (1) 0: disabled (default) 1: enabled
5	HS12_CCM	Constant current mode on HS12 enable (1) 0: disabled (default) 1: enabled
4	HS11_CCM	Constant current mode on HS11 enable (1) 0: disabled (default) 1: enabled
3	HS10_CCM	Constant current mode on HS10 enable (1) 0: disabled (default) 1: enabled
2	HS9_CCM	Constant current mode on HS9 enable (1) 0: disabled (default) 1: enabled
1	HS8_CCM	Constant current mode on HS8 enable (1)

Bit	Name	Description
		0: disabled (default) 1: enabled
0	HS7_CCM	Constant current mode on HS7 enable (1) 0: disabled (default) 1: enabled

1. Refer to Section 3.14: Power outputs HB1,..., HB6, HB20, HB21, HS7,..., HS15, HS0, HS16,..., HS19 for the correct sequence of constant current mode activation.

6.4.8 Control register 31 (CR31, 0x2D)

Table 95. Control register 31

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	HB21_OCR	HB20OCR	HB21HS	HB21LS	HB20HS	HB20LS	RESERVED	HS19_2	HS19_1	HS19_0	RESERVED	HS18_2	HS18_1	HS18_0	RESERVED	HS17_2	HS17_1	HS17_0	RESERVED	HS16_2	HS16_1	HS16_0
Reset value	0																							
Access	R		RW						R	RW			R	RW			R	RW			R	RW		

Table 96. CR31 signals description

Bit	Name	Description
23:22	RESERVED	-
21	HB21_OCR	LIN TXD timeout detection 0: LIN TXD timeout detection disabled 1: LIN TXD timeout detection enabled (default)
20	HB20_OCR	Configuration of LIN wake-up behavior 0: wake-up at recessive-dominant-recessive with t_dom > 28 µs (default) (according to LIN 2.2a and hardware requirements for transceivers version 1.3) 1: wake-up at recessive-dominant transition
19	HB21_HS	-
18	HB21_LS	Electro chrome controller voltage 0: electro chrome controller voltage set to minimum value (default) 1: electro chrome controller voltage set to maximum value
17	HB20_HS	Charge pump dithering 0: charge pump dithering enabled (default) 1: charge pump dithering disabled
16	HB20_LS	ICMP configuration enable 0: writing ICMP = 1 is blocked (writing ICMP = 0 is possible); (default) 1: writing ICMP = 1 is possible with next SPI command bit is automatically reset to 0 after next SPI command

Bit	Name	Description
15	RESERVED	-
14	HS19_2	High-side driver HS19 configuration:
13	HS19_1	000: OFF (default)
12	HS19_0	001: ON 010: Timer 1 011: Timer 2 100: PWM14 101: OFF 110: DIR1 111: DIR2
11	RESERVED	-
10	HS18_2	High-side driver HS18 configuration:
9	HS18_1	000: OFF (default)
8	HS18_0	001: ON 010: Timer 1 011: Timer 2 100: PWM13 101: OFF 110: DIR1 111: DIR2
7	RESERVED	-
6	HS17_2	High-side driver HS17 configuration:
5	HS17_1	000: OFF (default)
4	HS17_1	001: ON 010: Timer 1 011: Timer 2 100: PWM12 101: OFF 110: DIR1 111: DIR2
3	RESERVED	-
2	HS16_2	High-side driver HS16 configuration:
1	HS16_1	000: OFF (default)
0	HS16_1	001: ON 010: Timer 1 011: Timer 2 100: PWM11 101: OFF 110: DIR1 111: DIR2

6.4.9 Control register 32 (CR32, 0x2E)

Table 97. **Control register 32**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LIN2_TXD_TOUT_EN	LIN2_WU_CONFIG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	EI9_PU	EI8_PU	EI7_PU	EI6_PU	EI5_PU	EI4_PU	EI3_PU
Reset value	0						1	0																
Access	R					RW		R										RW						

Table 98. **CR32 signals description**

Bit	Name	Description
23:19	RESERVED	-
18	LIN2_TXD_TOUT_EN	LIN TXD timeout detection: 0: LIN TXD timeout detection disabled 1: LIN TXD timeout detection enabled (default)
17	LIN2_WU_CONFIG	Configuration of LIN2 wake-up behavior: 0: wake-up at recessive-dominant-recessive with t_dom > 28 μs (default) (according to LIN 2.2a and hardware requirements for transceivers version 1.3) 1: wake-up at recessive-dominant transition
16:7	RESERVED	-
6	EI9_PU	External interrupt 9: configuration of internal current source 0: pull-down (default) 1: pull-up
5	EI8_PU	External interrupt 8: configuration of internal current source 0: pull-down (default) 1: pull-up
4	EI7_PU	External interrupt 7: configuration of internal current source 0: pull-down (default) 1: pull-up
3	EI6_PU	External interrupt 6: configuration of internal current source 0: pull-down (default) 1: pull-up
2	EI5_PU	External interrupt 5: configuration of internal current source 0: pull-down (default) 1: pull-up
1	EI4_PU	External interrupt 4: configuration of internal current source 0: pull-down (default) 1: pull-up
0	EI3_PU	External interrupt 3: configuration of internal current source 0: pull-down (default) 1: pull-up

6.4.10 Control register 33 (CR33, 0x2F)

Table 99. Control register 33

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	LIN2_WU_EN	EI9_EN	EI8_EN	EI7_EN	EI6_EN	EI5_EN	EI4_EN	EI3_EN	RESERVED	RESERVED	EI9_FILT_1	EI9_FILT_0	EI8_FILT_1	EI8_FILT_0	EI7_FILT_1	EI7_FILT_0	EI6_FILT_1	EI6_FILT_0	EI5_FILT_1	EI5_FILT_0	EI4_FILT_1	EI4_FILT_0	EI3_FILT_1	EI3_FILT_0
Reset value	1								0															
Access	RW								R		RW													

Table 100. CR33 signals description

Bit	Name	Description
23	LIN2_WU_EN	Enable wake-up by LIN2: 0: disabled 1: enabled (default)
22	EI9_EN	External interrupt 9 enable: 0: EI9 disabled 1: EI9 enabled (default)
21	EI8_EN	External interrupt 8 enable: 0: EI8 disabled 1: EI8 enabled (default)
20	EI7_EN	External interrupt 7 enable: 0: EI7 disabled 1: EI7 enabled (default)
19	EI6_EN	External interrupt 6 enable: 0: EI6 disabled 1: EI6 enabled (default)
18	EI5_EN	External interrupt 5 enable: 0: EI5 disabled 1: EI5 enabled (default)
17	EI4_EN	External interrupt 4 enable: 0: EI4 disabled 1: EI4 enabled (default)
16	EI3_EN	External interrupt 3 enable: 0: EI3 disabled 1: EI3 enabled (default)
15:14	RESERVED	-
13	EI9_FILT_1	External interrupt 9: input filter configuration
12	EI9_FILT_0	00: external interrupt 9 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 9 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)

Bit	Name	Description
		10: external Interrupt 9 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set
11	EI8_FILT_1	External interrupt 8: input filter configuration
10	EI8_FILT_0	00: external interrupt 8 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 8 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 10: external interrupt 8 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set
9	EI7_FILT_1	External interrupt 7: input filter configuration
8	EI7_FILT_0	00: external interrupt 7 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 7 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 10: external interrupt 7 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set
7	EI6_FILT_1	External interrupt 6: input filter configuration
6	EI6_FILT_0	00: external interrupt 6 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 6 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 10: external interrupt 6 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set
5	EI5_FILT_1	External interrupt 5: input filter configuration
4	EI5_FILT_0	00: external interrupt 5 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 5 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 10: external interrupt 5 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set
3	EI4_FILT_1	External interrupt 4: input filter configuration
2	EI4_FILT_0	00: external interrupt 4 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 4 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 10: external interrupt 4 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set
1	EI3_FILT_1	External interrupt 3: input filter configuration
0	EI3_FILT_0	00: external interrupt 3 monitored in static mode (filter time t_{wu_stat}) (default) 01: external interrupt 3 monitored in cyclic mode with timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 10: external interrupt 3 monitored in cyclic mode with timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time) 11: invalid setting; command is ignored and SPI INV CMD id set

6.4.11 Control register 4 (CR4, 0x30)

Table 101. **Control register 4**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	HS7_OCR_TON_1	HS7_OCR_TON_0	HS_OCR_TON_1	HS_OCR_TON_0	HB_OCR_TON_1	HB_OCR_TON_0	HS7_OCR_FREQ_1	HS7_OCR_FREQ_0	HS_OCR_FREQ_1	HS_OCR_FREQ_0	HB_OCR_FREQ_1	HB_OCR_FREQ_0
Reset value	0													1	0	1	0	1	0					
Access	R												RW											

Table 102. **CR4 signals description**

Bit	Name	Description
23:12	RESERVED	-
11	HS7_OCR_TON_1	Overcurrent recovery programmable ON time for HS7 ON time also includes the blanking time t_{BLK} 00: ON time = 88 µs 01: ON time = 80 µs (default) 10: ON time = 72 µs 11: ON time = 64 µs
10	HS7_OCR_TON_0	
9	HS_OCR_TON_1	Overcurrent recovery programmable ON time for HS8, HS9, HS10 and electro chrome ON time also includes the blanking time t_{BLK} 00: ON time = 88 µs 01: ON time = 80 µs (default) 10: ON time = 72 µs 11: ON time = 64 µs
8	HS_OCR_TON_0	
7	HB_OCR_TON_1	Overcurrent recovery programmable ON time for HB1, HB2, HB3, HB4, HB5, HB6, HB20, HB21 ON time also includes the blanking time t_{BLK} 00: ON time = 88 µs 01: ON time = 80 µs (default) 10: ON time = 72 µs 11: ON time = 64 µs
6	HB_OCR_TON_0	
5	HS7_OCR_FREQ_1	Overcurrent recovery programmable frequency for HS7 00: frequency = 1.7 kHz (default) 01: frequency = 2.2 kHz 10: frequency = 3.0 kHz 11: frequency = 4.4 kHz
4	HS7_OCR_FREQ_0	
3	HS_OCR_FREQ_1	Overcurrent recovery programmable frequency for HS8, HS9, HS10 and electro chrome 00: frequency = 1.7 kHz (default) 01: frequency = 2.2 kHz 10: frequency = 3.0 kHz 11: frequency = 4.4 kHz
2	HS_OCR_FREQ_0	
1	HB_OCR_FREQ_1	Overcurrent recovery programmable frequency for HB1, HB2, HB3, HB4, HB5, HB6, HB20, HB21 00: frequency = 1.7 kHz (default)

Bit	Name	Description
0	HB_OCR_FREQ_0	01: frequency = 2.2 kHz 10: frequency = 3.0 kHz 11: frequency = 4.4 kHz

6.4.12 Control register 5-9 (from CR5 to CR9, [0x32, 0x36])

Table 103. Control register 5-9

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	PWMx_DC_9	PWMx_DC_8	PWMx_DC_7	PWMx_DC_6	PWMx_DC_5	PWMx_DC_4	PWMx_DC_3	PWMx_DC_2	PWMx_DC_1	PWMx_DC_0	RESERVED	RESERVED	PWMy_DC_9	PWMy_DC_8	PWMy_DC_7	PWMy_DC_6	PWMy_DC_5	PWMy_DC_4	PWMy_DC_3	PWMy_DC_2	PWMy_DC_1	PWMy_DC_0
Reset value	0																							
Access	R		RW										R		RW									

Table 104. From CR5 to CR9 signals description

Bit	Name	Description
23:22	RESERVED	-
21	PWMx_DC_9	Binary coded on duty cycle of PWM channel PWMx (x = 9, 7, 5, 3, 1) (see Table 105. Duty cycle coding for channel PWMx(y))
20	PWMx_DC_8	
19	PWMx_DC_7	
18	PWMx_DC_6	
17	PWMx_DC_5	
16	PWMx_DC_4	
15	PWMx_DC_3	Binary coded on duty cycle of PWM channel PWMx (x = 9, 7, 5, 3, 1) (see Table 105. Duty cycle coding for channel PWMx(y))
14	PWMx_DC_2	
13	PWMx_DC_1	
12	PWMx_DC_0	
11:10	RESERVED	-
9	PWMy_DC_9	Binary coded on duty cycle of PWM channel PWMy (y = x + 1) (see Table 105. Duty cycle coding for channel PWMx(y))
8	PWMy_DC_8	
7	PWMy_DC_7	Binary coded on duty cycle of PWM channel PWMy (y = x + 1) (see Table 105. Duty cycle coding for channel PWMx(y))
6	PWMy_DC_6	
5	PWMy_DC_5	
4	PWMy_DC_4	
3	PWMy_DC_3	
2	PWMy_DC_2	
1	PWMy_DC_1	
0	PWMy_DC_0	

Table 105. Duty cycle coding for channel PWMx(y)

PWMx(y)_DC_10	PWMx(y)_DC_9	PWMx(y)_DC_8	PWMx(y)_DC_7	PWMx(y)_DC_6	PWMx(y)_DC_5	PWMx(y)_DC_4	PWMx(y)_DC_3	PWMx(y)_DC_2	PWMx(y)_DC_9	Duty cycle %
0	0	0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	0	0	1	1*100/1024
0	0	0	0	0	0	0	0	1	0	2*100/1024
										...
1	1	1	1	1	1	1	1	0	1	1021*100/1024
1	1	1	1	1	1	1	1	1	0	1022*100/1024
1	1	1	1	1	1	1	1	1	1	1023*100/1024

Note: To have a duty cycle equal to 100%, the output configuration shall be set in ON mode.

6.4.13 Control register 10 (0x37)

Table 106. **Control register 10**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM10_FREQ	PWM9_FREQ	PWM8_FREQ	PWM7_FREQ	PWM6_FREQ	PWM5_FREQ	PWM4_FREQ	PWM3_FREQ	PWM2_FREQ	PWM1_FREQ
Reset value	0																							
Access	R														RW									

Table 107. **CR10 signals description**

Bit	Name	Description
23:10	RESERVED	-
9	PWM10_FREQ	Select PWM10 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
8	PWM9_FREQ	Select PWM9 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
7	PWM8_FREQ	Select PWM8 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
6	PWM7_FREQ	Select PWM7 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
5	PWM6_FREQ	Select PWM6 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
4	PWM5_FREQ	Select PWM5 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
3	PWM4_FREQ	Select PWM4 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
2	PWM3_FREQ	Select PWM3 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz
1	PWM2_FREQ	Select PWM2 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz

Bit	Name	Description
0	PWM1_FREQ	Select PWM1 frequency 0: f_{PWM1} = 100 Hz (default) 1: f_{PWM2} = 200 Hz

6.4.14 Control register 11 (0x38)

Table 108. **Control register 11**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ECV_LS	ECV_OCR	RESERVED	RESERVED	RESERVED	ECON	RESERVED	RESERVED	EC_5	EC_4	EC_3	EC_2	EC_1	EC_0
Reset value	0																							
Access	R										RW		R			RW	R		RW					

Table 109. **CR11 signals description**

Bit	Name	Description
23:14	RESERVED	-
13	ECV_LS	Control of ECV low-side switch 0: ECV low-side switch OFF (default) 1: ECV low-side switch ON
12	ECV_OCR	Overcurrent recovery for output ECV 0: overcurrent recovery is turned OFF (default) 1: overcurrent recovery is turned ON
11:9	RESERVED	-
8	ECON	Electro chrome control; the electro chrome control enables the driver at pin ECDR and switches HS10 directly ON ignoring the control bits HS10_x (x = 3, 2, 1, 0) in CR15 0: electro chrome control OFF (default) 1: electro chrome control ON
7:6	RESERVED	-
5	EC_5	000000: voltage value is 0 V (default) 000001: voltage value is 1/63*1.5 V 000010: voltage value is 2/63*1.5 V ... 111110: voltage value is 62/63*1.5 V 111111: voltage value is 1.5 V
4	EC_4	
3	EC_3	
2	EC_2	
1	EC_1	
0	EC_0	

Note: The reference voltage for the electro chrome voltage controller at pin ECV is binary coded. If the ECV_HV bit (CR1) is "0" all codes higher than 110011 are clamped to reach 1.2 V max on ECV pin.

6.4.15 Control register 12 (0x39)

Table 110. Control register 12

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	DIAG_1	DIAG_0	GH_OL_EN	GH	GH_TH_3	GH_TH_2	GH_TH_1	GH_TH_0	SD	SDS	DM	COPT_3	COPT_2	COPT_1	COPT_0	H_OLTH_HIGH	OL_H1L2	OL_H2L1	SLEW_4	SLEW_3	SLEW_2	SLEW_1	SLEW_0
Reset value	0	1		0		1	0		1	0			1				0							
Access	R	RW																						

Table 111. CR12 signals description

Bit	Name	Description
23	RESERVED	-
22	DIAG_1	Drain-source monitoring threshold for external H-bridge
21	DIAG_1	**Monitoring threshold voltage** 00 V_{SCd1} 01 V_{SCd2} 10 V_{SCd3} 11 V_{SCd4} (default)
20	GH_OL_EN[(1)]	Control open-load diagnosis for gate heater output 0: open-load diagnosis OFF (default) 1: open-load diagnosis ON
19	GH	Gate heater enable 0: gate heater disabled (default) 1: gate heater enabled
18	GH_TH_3	Drain-source monitoring threshold voltage for external heater Power MOSFET. Invalid setting is ignored; SPI error bit (SPIE) in global status register is set 0000 V_{SCd1} 0001 V_{SCd2} 0010 V_{SCd3} 0011 V_{SCd4} 0100 V_{SCd5} 0101 V_{SCd6} 0110 V_{SCd7} 0111 V_{SCd8} 1000 V_{SCd9} 1001 V_{SCd10} (default) 1010 invalid configuration ... 1111 invalid configuration
17	GH_TH_2	
16	GH_TH_1	
15	GH_TH_0	
14	SD	Slow decay 0: slow decay mode low-side ON (default, LS1 or LS2 depending only on DIRH pin)

Bit	Name	Description
		1: slow decay mode high-side ON (HS1 or HS2 depending only on DIRH pin)
13	SDS	Slow decay single 0: slow decay mode both legs ON (default) 1: slow decay mode single leg ON
12	DM	Dual motor H-bridge configuration 0: single motor mode (default) 1: dual motor mode
11	COPT_3	Cross current protection time(2) 0010 $tccp_{0010}$ 0011 $tccp_{0011}$ 0100 $tccp_{0100}$ 0101 $tccp_{0101}$ 0110 $tccp_{0110}$ 0111 $tccp_{0111}$ 1000 $tccp_{1000}$ 1001 $tccp_{1001}$ 1010 $tccp_{1010}$ 1011 $tccp_{1011}$ 1100 $tccp_{1100}$ 1101 $tccp_{1101}$ 1110 $tccp_{1110}$ 1111 $tccp_{1111}$ (default)
10	COPT_2	
9	COPT_1	
8	COPT_0	
7	H_OLTH_HIGH	H-bridge OL high threshold (5/6 * V_S) select 0: V_{SCd} threshold low (default, 1/6 * V_S) 1: V_{SCd} threshold high (5/6 * V_S)
6	OL_H1L2(3)	Test open-load condition between H1 and L2 0: no pull-up on H1 (default, no test on H1 L2) 1: pull-up resistor on H1 (test on H1 L2)
5	OL_H2L1(3)	Test open-load condition between H2 and L1 0: no pull-up on H2 (default, no test on H1 L2) 1: pull-up resistor on H2 (test on H2 L1)
4	SLEW_4	Binary coded slew rate of the H-bridge **Slew rate value** 00000: control disabled (default) 00001: 1/31 00010: 2/31 ... 11110: 30/31 11111: 1
3	SLEW_3	
2	SLEW_2	
1	SLEW_1	
0	SLEW_0	

1. *Before going to standby mode, GH_OL_EN must be set to 0 to achieve the specified current consumption.*
2. *t_{ccp} values “0000” and “0001” are not allowed.*
3. *Before going to standby mode, OL_H1L2 and OL_H2L1 must be set to 0 to achieve the specified current consumption.*

6.4.16 Control register 13 (0x3A)

Table 112. Control register 13

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	HS7_RDSON	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	HS10_OCR	HS9_OCR	HS8_OCR	HS7_OCR	HB6_OCR	HB5_OCR	HB4_OCR	HB3_OCR	HB2_OCR	HB1_OCR	RESERVED	RESERVED	CM	CM_SEL_4	CM_SEL_3	CM_SEL_2	CM_SEL_1	CM_SEL_0
Reset value	0																		1	0				
Access	RW	R					RW										R		RW					

Table 113. CR13 signals description

Bit	Name	Description
23	HS7_RDSON	Select R_{dson} for HS7 0 r_{ON1} (0.3 Ω) (default) 1 r_{ON2} (1.6 Ω)
22:18	RESERVED	-
17	HS10_OCR	Overcurrent recovery for HS10 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
16	HS9_OCR	Overcurrent recovery for HS9 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
15	HS8_OCR	Overcurrent recovery for HS8 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
14	HS7_OCR	Overcurrent recovery for HS7 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
13	HB6_OCR	Overcurrent recovery for HB6 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
12	HB5_OCR	Overcurrent recovery for HB5 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
11	HB4_OCR	Overcurrent recovery for HB4 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
10	HB3_OCR	Overcurrent recovery for HB3 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
9	HB2_OCR	Overcurrent recovery for HB2 0 overcurrent recovery is turned OFF (default)

Bit	Name	Description
		1 overcurrent recovery is turned ON
8	HB1_OCR	Overcurrent recovery for HB1 0 overcurrent recovery is turned OFF (default) 1 overcurrent recovery is turned ON
7:6	RESERVED	-
5	CM	Current monitor 0 OFF (tristate) 1 ON (default)
4	CM_SEL_4	A current image of the selected binary coded output is multiplexed to the CM output. If a corresponding output does not exist, the current monitor is deactivated. **Selected output** 00000 tristate (default) 00001 HB1 00010 HB2 00011 HB3 00100 HB4 00101 HB5 00110 HB6 00111 HS7 01000 HS8 01001 HS9 01010 HS10 01011 HS11 01100 HS12 01101 HS13 01110 HS14 01111 HS15 10000 HS0 10001 HS16 10010 HS17 10011 HS18 10100 HS19 10101 HB20 10110 HB21 10111 tristate … … tristate 11111 tristate
3	CM_SEL_3	
2	CM_SEL_2	
1	CM_SEL_1	
0	CM_SEL_0	

6.4.17 Control register 14 (0x3B)

Table 114. Control register 14

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	HS0_3	HS0_2	HS0_1	HS0_0	HS15_3	HS15_2	HS15_1	HS15_0	HS14_3	HS14_2	HS14_1	HS14_0	HS13_3	HS13_2	HS13_1	HS13_0
Reset value	0																							
Access	R								RW															

Table 115. CR14 signals description

Bit	Name	Description
23:16	RESERVED	-
15	HS0_3	High-side driver HS0 configuration
14	HS0_2	**HS0 config**
13	HS0_1	0000: OFF (default)
12	HS0_0	0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
11	HS15_3	High-side driver HS15 configuration
10	HS15_1	**HS15 config**
9	HS15_1	0000: OFF (default)
8	HS15_0	0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6

Bit	Name	Description
		1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
7	HS14_3	High-side driver HS14 configuration **HS14 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
6	HS14_2	
5	HS14_1	
4	HS14_0	
3	HS13_3	High-side driver HS13 configuration **HS13 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
2	HS13_2	
1	HS13_1	
0	HS13_0	

6.4.18 Control register 15 (0x3C)

Table 116. Control register 15

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	HS12_3	HS12_2	HS12_1	HS12_0	HS11_3	HS11_2	HS11_1	HS11_0	HS10_3	HS10_2	HS10_1	HS10_0	HS9_3	HS9_2	HS9_1	HS9_0	HS8_3	HS8_2	HS8_1	HS8_0	HS7_3	HS7_2	HS7_1	HS7_0
Reset value	0																							
Access	RW																							

Table 117. CR15 signals description

Bit	Name	Description
23	HS12_3	High-side driver HS12 configuration **HS12 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
22	HS12_2	
21	HS12_1	
20	HS12_0	
19	HS11_3	High-side driver HS11 configuration **HS11 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1011: PWM8
18	HS11_2	
17	HS11_1	
16	HS11_0	

Bit	Name	Description
		1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
15	HS10_3	High-side driver HS10 configuration **HS10 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
14	HS10_2	
13	HS10_1	
12	HS10_0	
11	HS9_3	High-side driver HS9 configuration **HS9 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
10	HS9_2	
9	HS9_1	
8	HS9_0	
7	HS8_3	High-side driver HS8 configuration **HS8 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2
6	HS8_2	
5	HS8_1	
4	HS8_0	

Bit	Name	Description
		0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
3	HS7_3	High-side driver HS7 configuration **HS7 config** 0000: OFF (default) 0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2
2	HS7_2	
1	HS7_1	
0	HS7_0	

6.4.19 Control register 16 (0x3D)

Table 118. **Control register 16**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	VSREG_LOCK_ENA	VS_LOCK_ENA	VSREG_OV_SD_ENA	VSREG_UV_SD_ENA	VS_OV_SD_ENA	VS_UV_SD_ENA	HB6OCTH_1	HB6OCTH_0	HB5OCTH_1	HB5OCTH_0	HB1OCTH_1	HB1OCTH_0	HB6_HS	HB6_LS	HB5_HS	HB5_LS	HB4_HS	HB4_LS	HB3_HS	HB3_LS	HB2_HS	HB2_LS	HB1_HS	HB1_LS
Reset value	1						0																	
Access	RW																							

Table 119. **CR16 signals description**

Bit	Name	Description
23	VSREG_LOCK_ENA	Lockout of VSREG related outputs after VSREG over/undervoltage shutdown: 0 VSREG related outputs are turned ON automatically and status bits (VSREG_UV, VSREG_OV) are cleared 1 VSREG related outputs remain turned OFF until status bits (VSREG_UV, VSREG_OV) are cleared (default) *Note: lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions.*
22	VS_LOCK_ENA	Lockout of V_S related outputs after V_S over/undervoltage shutdown: 0 V_S related outputs are turned ON automatically and status bits (VS_UV, VS_OV) are cleared 1 V_S related outputs remain turned OFF until status bits (VS_UV, VS_OV) are cleared (default) *Note: lockout is always disabled in standby modes in order to ensure supply of external contacts and detect wake-up conditions.*
21	VSREG_OV_SD_ENA	Shutdown of VSREG related outputs in case of VSREG overvoltage: 0 no shutdown of VSREG related outputs in case of VSREG overvoltage 1 shutdown of VSREG related outputs in case of VSREG overvoltage (default)
20	VSREG_UV_SD_ENA	Shutdown of VSREG related outputs in case of VSREG undervoltage: 0 no shutdown of VSREG related outputs in case of VSREG undervoltage 1 shutdown of VSREG related outputs in case of VSREG undervoltage (default) *Note: in case of V1 undervoltage due to VSREG UV, the device enters failsafe mode and the related outputs are turned OFF.*
19	VS_OV_SD_ENA	Shutdown of V_S related outputs in case of $V_S$overvoltage: 0 no shutdown of V_S related outputs in case of V_S overvoltage if charge pump output voltage is still sufficient (until CPLOW threshold is reached) 1 shutdown of V_S related outputs in case of V_S overvoltage (default)
18	VS_UV_SD_ENA	Shutdown of V_S related outputs in case of V_S undervoltage: 0 no shutdown of V_S related outputs in case of V_S UnderVoltage 1 shutdown of V_S related outputs in case of V_S UnderVoltage (default) *Note: In case of V1 UnderVoltage due to VS UV, the device enters fail-safe mode and the related outputs are turned OFF.*
17	HB6OCTH_1	Selectable overcurrent threshold on HB6: 00 I_{OC6th3}(default) 01 I_{OC6th1}
16	HB6OCTH_0	

Bit	Name	Description
		10 I_{OC6th2} 11 I_{OC6th3}
15	HB5OCTH_1	Selectable overcurrent threshold on HB5: 00 I_{OC5th3} (default) 01 I_{OC5th1} 10 I_{OC5th2} 11 I_{OC5th3}
14	HB5OCTH_0	
13	HB1OCTH_1	Selectable overcurrent threshold on HB1: 00 I_{OC1th3} (default) 01 I_{OC1th1} 10 I_{OC1th2} 11 I_{OC1th3}
12	HB1OCTH_0	
11	HB6_HS	HB6 high-side driver control: 0 HB6 HS is turned off (default) 1 HB6 HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB6 are switched on simultaneously
10	HB6_LS	HB6 low-side driver control: 0 HB6 LS is turned off (default) 1 HB6 LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB6 are switched on simultaneously
9	HB5_HS	HB5 high-side driver control: 0 HB5 HS is turned off (default) 1 HB5 HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB5 are switched on simultaneously
8	HB5_LS	HB5 low-side driver control: 0 HB5 LS is turned off (default) 1 HB5 LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB5 are switched on simultaneously
7	HB4_HS	HB4 high-side driver control: 0 HB4 HS is turned off (default) 1 HB4 HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB4 are switched on simultaneously
6	HB4_LS	HB4 low-side driver control: 0 HB4 LS is turned off (default) 1 HB4 LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB4 are switched on simultaneously
5	HB3_HS	HB3 high-side driver control: 0 HB3 HS is turned off (default) 1 HB3 HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB3 are switched on simultaneously
4	HB3_LS	HB3 low-side driver control: 0 HB3 LS is turned off (default)

Bit	Name	Description
		1 HB3 LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB3 are switched on simultaneously
3	HB2_HS	HB2 high-side driver control: 0 HB2 HS is turned off (default) 1 HB2 HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half-bridge HB2 are switched on simultaneously
2	HB2_LS	HB2 low-side driver control: 0 HB2 LS is turned off (default) 1 HB2 LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB2 are switched on simultaneously
1	HB1_HS	HB1 high-side driver control: 0 HB1 HS is turned off (default) 1 HB1 HS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB1 are switched on simultaneously
0	HB1_LS	HB1 low-side driver control: 0 HB1 LS is turned off (default) 1 HB1 LS is turned on An internal cross-current protection prevents, that both the low-side and high-side drivers of the half bridge HB1 are switched on simultaneously

6.4.20 Control register 17 (0x3E)

Table 120. Control register 17

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	RESERVED	RESERVED	T2_ON_2	T2_ON_1	T2_ON_0	T2_PER_2	T2_PER_1	T2_PER_0	RESERVED	RESERVED	T1_ON_2	T1_ON_1	T1_ON_0	T1_PER_2	T1_PER_1	T1_PER_0	V1_RESET_1	V1_RESET_0	RESERVED	WD_TIME	RESERVED	RESERVED	STBY_SEL	GO_STBY
Reset value	0																							
Access	R		RW						R		RW								R	RW	R		RW	

Table 121. CR17 signals description

Bit	Name	Description
23:22	RESERVED	-
21	T2_ON_2	Configuration of Timer 2 ON-time
20	T2_ON_1	**T2 Config**
19	T2_ON_0	000 ton1 (default) 001 ton2 010 ton3 011 ton4 100 ton5 101 invalid setting; command is ignored and SPI INV CMD is set 110 invalid setting; command is ignored and SPI INV CMD is set 111 invalid setting; command is ignored and SPI INV CMD is set *Note: When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.*
18	T2_PER_2	Configuration of Timer 2 Period
17	T2_PER_1	**T2 Period**
16	T2_PER_0	000 T1 (default) 001 T2 010 T3 011 T4 100 T5 101 T6 110 T7 111 T8 *Note: When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.*
15:14	RESERVED	-
13	T1_ON_2	Configuration of Timer 1 ON-time
12	T1_ON_1	**T1 Config**
11	T1_ON_0	000 ton1 (default) 001 ton2 010 ton3

Bit	Name	Description
		011 ton4 100 ton5 101 invalid setting; command is ignored and SPI INV CMD is set 110 invalid setting; command is ignored and SPI INV CMD is set 111 invalid setting; command is ignored and SPI INV CMD is set *Note: When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.*
10	T1_PER_2	Configuration of Timer 1 Period
9	T1_PER_1	**T1 Period**
8	T1_PER_0	000 T1 (default) 001 T2 010 T3 011 T4 100 T5 101 T6 110 T7 111 T8 *Note: When the configuration of a timer is changed, the timer is automatically restarted using the new configuration.*
7	V1_RESET_1	Voltage regulator V1 reset level
6	V1_RESET_0	**V1 reset level** 00 V_{RT4} (default) 01 V_{RT3} 10 V_{RT2} 11 V_{RT1}
5	RESERVED	-
4	WD_TIME	Window Watchdog Trigger Time 0 TSW1 (default) 1 TSW2 Writing to WD_TIME_x is blocked unless WD_CONFIG_EN = 1
3	RESERVED	-
1	STBY_SEL	see Table 122. STBY_SEL and GO_STBY bits
0	GO_STBY	see Table 122. STBY_SEL and GO_STBY bits

Table 122. STBY_SEL and GO_STBY bits

STBY_SEL	GO_STBY	
1	1	Go to V1_Standby
0	1	Go to VBAT_Standby
1	0	No transition to standby
0	0	No transition to standby (default)

Note: After wake-up event, STBY_SEL and GO_STBY bits do not change the value remaining with the same setting.

6.4.21 Control register 18 (0x3F)

Table 123. Control register 18

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	EI2_PU	RESERVED	RESERVED	EI1_PU	EI2_EN	RESERVED	RESERVED	EI1_EN	EI2_FILT_1	EI2_FILT_0	RESERVED	RESERVED	RESERVED	RESERVED	EI1_FILT_1	EI1_FILT_0	HEN	CAN_REC_ONLY	CAN_ACT	LIN_WU_EN	CAN_WU_EN	TIME_NINT_WAKE_SEL	TIMER_NINT_EN	TRIG
Reset value	0				1				0											1		0		
Access	RW	R		RW		R		RW			R				RW									

Table 124. CR18 signals description

Bit	Name	Description
23	EI2_PU	External Interrupt 2: configuration of internal current source 0: pull-down (default) 1: pull-up *Note: the setting is valid only if input is configured as External Interrupt in CR1 (0x26).*
22:21	RESERVED	-
20	EI1_PU	External Interrupt 1: configuration of internal current source 0: pull-down (default) 1: pull-up
19	EI2_EN	External Interrupt 2 enable 0: EI2 disabled 1: EI2 enabled (default) *Note: the setting is valid only if input is configured as External Interrupt in CR1 (0x26).*
18:17	RESERVED	-
16	EI1_EN	External Interrupt 2 enable 0: EI1 disabled 1: EI1 enabled (default)
15	EI2_FILT_1	External Interrupt 2: configuration of input filter
14	EI2_FILT_0	**Input Filter Configuration** 00 External Interrupt 2 monitored in static mode (filter time t_{wu_stat}) (default) 01 External Interrupt 2 monitored in cyclic mode with Timer2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)(1) 10 External Interrupt 2 monitored in cyclic mode with Timer1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)(1) 11 Invalid setting; command is ignored and SPI INV CMD id set *Note: EI2_FILT_[1:0] setting is only valid if input is configured as External Interrupt in CR1 (0x26).*
13:10	RESERVED	-
9	EI1_FILT_1	External Interrupt 1: configuration of input filter
8	EI1_FILT_0	**Input Filter Configuration** 00 External Interrupt 1 monitored in static mode (filter time t_{wu_stat}) (default) 01 External Interrupt 1 monitored in cyclic mode with Timer 2 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)(1)

Bit	Name	Description
		10 External Interrupt 1 monitored in cyclic mode with Timer 1 (filter time: t_{WU_cyc}; blanking time 80% of timer ON time)[1] 11 Invalid setting; command is ignored and SPI INV CMD is set
7	HEN	Enable H-bridge 0: H-bridge disabled (default) 1: H-bridge enabled Refer to Section 2.4.14: H-bridge driver for details.
6	CAN_REC_ONLY	CAN receive only mode 0: CAN receive Only mode disabled (default) 1: CAN receive Only mode enabled (CAN Trx must be activated, see CAN_ACT bit)
5	CAN_ACT	CAN transceiver activation 0: CAN Trx low-power mode (default) 1: CAN Trx normal mode
4	LIN_WU_EN [2]	Enable wake-up by LIN 0: disabled 1: enabled (default) *Note: the wake-up behavior is configurable in the CR1 (0x26).*
3	CAN_WU_EN [2]	Enable wake-up by CAN 0: disabled 1: enabled (default) *Note: wake-up occurs at a wake–up event according to ISO 11898-2.*
2	TIME_NINT_WAKE_SEL	Select timer for periodic interrupt in standby modes 0: Timer 2 (default) 1: Timer 1
1	TIMER_NINT_ EN	Enable timer interrupt in standby modes 0: Timer Interrupt disabled (default) 1: Timer Interrupt enabled V1_Standby mode: device wakes up and interrupt signal is generated at RXDL/NINT when programmable time-out has elapsed. VBAT_Standby mode: device wakes up after timer expiration and generates Nreset.
0	TRIG	Watchdog Trigger bit

1. *Lower is the timer duration and major is the contribution of output $t_{d\ ON}$.*
2. *Either LIN or CAN must be enabled as wake-up source. Setting both bits 3 and 4 to ‘0’ is an invalid setting. All wake-up sources are configured according to default setting; SPI Error Bit (SPIE) in Global Status Register is set.*

6.5 Status registers

6.5.1 Status register 1 (0x01)

Table 125. Status register 1

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	TW_CL8	TW_CL7	TW_CL6	TW_CL5	TW_CL4	TW_CL3	TW_CL2	TW_CL1	HB21_LS_SC	HB20_LS_SC	HB6_LS_SC	HB5_LS_SC	HB4_LS_SC	HB3_LS_SC	HB2_LS_SC	HB1_LS_SC	HS19_OL	HS18_OL	HS17_OL	HS16_OL	HB21_LS_OL	HB21_HS_OL	HB20_LS_OL	HB20_HS_OL
Access	R&C																							

Table 126. Status register 1 description

Bit	Name	Description
23	TW_CL8	Temperature warning cluster 8: ‘1’ indicates cluster 8 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
22	TW_CL7	Temperature warning cluster 7: ‘1’ indicates cluster 7 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
21	TW_CL6	Temperature warning cluster 6: ‘1’ indicates cluster 6 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
20	TW_CL5	Temperature warning cluster 5: ‘1’ indicates cluster 5 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
19	TW_CL4	Temperature warning cluster 4: ‘1’ indicates cluster 4 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
18	TW_CL3	Temperature warning cluster 3: ‘1’ indicates cluster 3 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
17	TW_CL2	Temperature warning cluster 2: ‘1’ indicates cluster 2 has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
16	TW_CL1	Temperature warning cluster 1: ‘1’ indicates cluster 1 has reached the thermal warning threshold Bit is latched until a “Read & Clear”command
15	HB21_LS_SC	Short circuit on HB21 low-side: “1” indicates short circuit condition on LS of HB21 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
14	HB20_LS_SC	Short circuit on HB20 low-side: “1” indicates short circuit condition on LS of HB20 (second overcurrent threshold in overcurrent recovery mode)

Bit	Name	Description
		Bit is latched until a “Read & Clear” command
13	HB6_LS_SC	Short-circuit on HB6 low-side: “1” indicates short-circuit condition on LS of HB6 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
12	HB5_LS_SC	Short-circuit on HB5 low-side: “1” indicates short-circuit condition on LS of HB5 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
11	HB4_LS_SC	Short-circuit on HB4 low-side: “1” indicates short-circuit condition on LS of HB4 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
10	HB3_LS_SC	Short-circuit on HB3 low-side: “1” indicates short-circuit condition on LS of HB3 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
9	HB2_LS_SC	Short-circuit on HB2 low-side: “1” indicates short-circuit condition on LS of HB2 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
8	HB1_LS_SC	Short-circuit on HB1 low-side: “1” indicates short-circuit condition on LS of HB1 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
7	HS19_OL	HS19 open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
6	HS18_OL	HS18 open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
5	HS17_OL	HS17 open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
4	HS16_OL	HS16 open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
3	HB21_LS_OL	HB21 low-side open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
2	HB21_HS_OL	HB21 high-side open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
1	HB20_LS_OL	HB20 low-side open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
0	HB20_HS_OL	HB20 high-side open-load: ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command

6.5.2 Status register 2 (0x02)

Table 127. **Status register 2**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	TSD1_CL8	TSD1_CL7	TSD1_CL6	TSD1_CL5	TSD1_CL4	TSD1_CL3	TSD1_CL2	TSD1_CL1	HB21_HS_SC	HB20_HS_SC	HB6_HS_SC	HB5_HS_SC	HB4_HS_SC	HB3_HS_SC	HB2_HS_SC	HB1_HS_SC	HS19_OC	HS18_OC	HS17_OC	HS16_OC	HB21_LS_OC	HB21_HS_OC	HB20_LS_OC	HB20_HS_OC
Access	R&C																							

Table 128. **Status register 2 description**

Bit	Name	Description
23	TSD1_CL8	Thermal shutdown of cluster 8 ‘1’ indicates cluster 8 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
22	TSD1_CL7	Thermal shutdown of cluster 7 ‘1’ indicates cluster 7 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
21	TSD1_CL6	Thermal shutdown of cluster 6 ‘1’ indicates cluster 6 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
20	TSD1_CL5	Thermal shutdown of cluster 5 ‘1’ indicates cluster 5 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
19	TSD1_CL4	Thermal shutdown of cluster 4 ‘1’ indicates cluster 4 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
18	TSD1_CL3	Thermal shutdown of cluster 3 ‘1’ indicates luster 3 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
17	TSD1_CL2	Thermal shutdown of cluster 2 ‘1’ indicates cluster 2 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
16	TSD1_CL1	Thermal shutdown of cluster 1 ‘1’ indicates cluster 1 has reached the thermal shutdown threshold (TSD1) and the output cluster was shutdown Bit is latched until a “Read & Clear” command
15	HB21_HS_SC	Short circuit on HB21 high-side: “1” indicates short circuit condition on HS of HB21 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
14	HB20_HS_SC	Short circuit on HB20 high-side: “1” indicates short circuit condition on HS of HB20 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
13	HB6_HS_SC	Short-circuit on HB6 high-side ‘1’ indicates short circuit condition on HS of HB6 (second overcurrent threshold in overcurrent recovery mode)

Bit	Name	Description
		Bit is latched until a “Read & Clear” command
12	HB5_HS_SC	Short-circuit on HB5 high-side ‘1’ indicates short-circuit condition on HS of HB5 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
11	HB4_HS_SC	Short-circuit on HB4 high-side ‘1’ indicates short circuit condition on HS of HB4 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
10	HB3_HS_SC	Short-circuit on HB3 high-side ‘1’ indicates short circuit condition on HS of HB3 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
9	HB2_HS_SC	Short-circuit on HB2 high-side ‘1’ indicates short-circuit condition on HS of HB2 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
8	HB1_HS_SC	Short-circuit on HB1 high-side ‘1’ indicates short-circuit condition on HS of HB1 (second overcurrent threshold in overcurrent recovery mode) Bit is latched until a “Read & Clear” command
7	HS19_OC	HS19 overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
6	HS18_OC	HS18 overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
5	HS17_OC	HS17 overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
4	HS16_OC	HS16 overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
3	HB21_LS_OC	HB21 low-side overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
2	HB21_HS_OC	HB21 high-side overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
1	HB20_LS_OC	HB20 low-side overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command
0	HB20_HS_OC	HB20 high-side overcurrent: ‘1’ indicates that an overcurrent condition was detected at the output Bit is latched until a “Read & Clear” command

6.5.3 Status register 3 (0x03)

Table 129. Status register 3

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WAKE_LIN2	EI9_WAKE	EI8_WAKE	EI7_WAKE	EI6_WAKE	EI5_WAKE	EI4_WAKE	EI3_WAKE	RESERVED	EI9_STATE	EI8_STATE	EI7_STATE	EI6_STATE	EI5_STATE	EI4_STATE	EI3_STATE	RESERVED	RESERVED	SGNDLOSS	IP_SUP_LOW	CAN_SUP_LOW	LIN2_PERM_DOM	LIN2_TXD_DOM	LIN2_PERM_REC
Access	R&CR								R	R&CR							R		R&CR					

Table 130. Status register 3 description

Bit	Name	Description
23	WAKE_LIN2	Wake-up from LIN2: ‘1’ means wake-up from LIN2 Bit is latched until a “Read & Clear” command
22	EI9_WAKE	External interrupt 9 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
21	EI8_WAKE	External interrupt 8 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
20	EI7_WAKE	External interrupt 7 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
19	EI6_WAKE	External interrupt 6 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
18	EI5_WAKE	External interrupt 5 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
17	EI4_WAKE	External interrupt 4 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
16	EI3_WAKE	External interrupt 3 wake-up: ‘1’ means wake-up from external interrupt. Bit is latched until a “Read & Clear” command
15	RESERVED	-
14	EI9_STATE	State of EI9 input: 0: input level is low 1 input level is high The bit shows the momentary status of EI9 and cannot be cleared (“Live bit”)
13	EI8_STATE	State of EI8 input: 0: input level is low 1 input level is high

Bit	Name	Description
		The bit shows the momentary status of EI8 and cannot be cleared ("Live bit")
12	EI7_STATE	State of EI7 input: 0: input level is low 1 input level is high The bit shows the momentary status of EI7 and cannot be cleared ("Live bit")
11	EI6_STATE	State of EI6 input: 0: input level is low 1 input level is high The bit shows the momentary status of EI6 and cannot be cleared ("Live bit")
10	EI5_STATE	State of EI5 input: 0: input level is low 1 input level is high The bit shows the momentary status of EI5 and cannot be cleared ("Live bit")
9	EI4_STATE	State of EI4 input: 0: input level is low 1 input level is high The bit shows the momentary status of EI4 and cannot be cleared ("Live bit")
8	EI3_STATE	State of EI3 input: 0: input level is low 1 input level is high The bit shows the momentary status of EI3 and cannot be cleared ("Live bit")
7:6	RESERVED	-
5	SGNDLOSS	Loss of ground status bit '1' indicates that ground at SGND pin has been lost Bit is not latched
4	IP_SUP_LOW	Internal IP supply low warning threshold '1' indicates that Internal IP voltage supply (analog and/or digital) is less than 3V Bit is latched until a "Read & Clear" command
3	CAN_SUP_LOW	CAN supply low warning threshold '1' indicates that voltage at CAN supply pin reached the CAN supply low warning threshold $V_{CANSUP} < V_{CANSUPlow}$ Bit is latched until a "Read & Clear" command
2	LIN2_PERM_DOM	TXDL2 pin is dominant for $t > t_{dom(TXDL)}$ The LIN2 transmitter is disabled until the bit is cleared Bit is latched until a "Read and clear" command
1	LIN2_TXD_DOM	LIN2 bus signal is dominant for $t > T_{dom(bus)}$ Bit is latched until a "Read and clear" command
0	LIN2_PERM_REC	LIN2 bus signal does not follow TXDL within t_{LIN} The LIN2 transmitter is disabled until the bit is cleared Bit is latched until a "Read and clear" command

6.5.4 Status register 4 (0x04)

Table 131. Status register 4

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	WD_TIMER_STATE_1	WD_TIMER_STATE_0	EI2_STATE	RESERVED	RESERVED	EI1_STATE	ECV_VNR	ECV_VHI	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
Access	R&C			R		R&C			R															

Table 132. Status register 4 description

Bit	Name	Description
23	WD_TIMER_STATE_1	Watchdog timer status **Status** 00 0 - 33% 01 33 - 66% 11 66 - 100% 10 invalid configuration
22	WD_TIMER_STATE_0	
21	EI2_STATE	State of EI2 input 0 input level is low 1 input level is high The bit shows the momentary status of EI2 and cannot be cleared (“live bit”) *Note: the status is only valid if it has been configured as wake-up input in CR1 (0x26). Otherwise this bit is read as ‘0’*
20	RESERVED	-
18	EI1_STATE	State of EI1 input 0 input level is low 1 input level is high The bit shows the momentary status of EI1 and cannot be cleared (“live bit”)
17	ECV_VNR	Electro chrome voltage not reached ‘1’ indicates the electro chrome voltage is not reached. Bit is not latched
16	ECV_VHI	Electro chrome voltage high ‘1’ indicates the electro chrome voltage is too high. Bit is not latched
15:0	RESERVED	-

6.5.5 Status register 5 (0x05)

Table 133. **Status register 5**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ECV_OL	GH_OL	HS0_OL	HS15_OL	HS14_OL	HS13_OL	HS12_OL	HS11_OL	HS10_OL	HS9_OL	HS8_OL	HS7_OL	HB6_LS_OL	HB6_HS_OL	HB5_LS_OL	HB5_HS_OL	HB4_LS_OL	HB4_HS_OL	HB3_LS_OL	HB3_HS_OL	HB2_LS_OL	HB2_HS_OL	HB1_LS_OL	HB1_HS_OL
Access	R&C																							

Table 134. **Status register 5 description**

Bit	Name	Description
23	ECV_OL	Electrochromic open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
22	GH_OL	‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
21	HS0_OL	HS0 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
20	HS15_OL	HS15 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
19	HS14_OL	HS14 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
18	HS13_OL	HS13 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
17	HS12_OL	HS12 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
16	HS11_OL	HS11 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
15	HS10_OL	HS10 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
14	HS9_OL	HS9 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
13	HS8_OL	HS8 open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
12	HS7_OL	HS7 open-load ‘1’ indicates an open-load condition was detected at the output

Bit	Name	Description
		Bit is latched until a “Read & Clear” command
11	HB6_LS_OL	HB6 low-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
10	HB6_HS_OL	HB6 high-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
9	HB5_LS_OL	HB5 low-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
8	HB5_HS_OL	HB5 high-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
7	HB4_LS_OL	HB4 low-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
6	HB4_HS_OL	HB4 high-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
5	HB3_LS_OL	HB3 low-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
4	HB3_HS_OL	HB3 high-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
3	HB2_LS_OL	HB2 low-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
2	HB2_HS_OL	HB2 high-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
1	HB1_LS_OL	HB1 low-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command
0	HB1_HS_OL	HS1 high-side open-load ‘1’ indicates an open-load condition was detected at the output Bit is latched until a “Read & Clear” command

6.5.6 Status register 6 (0x06)

Table 135. **Status register 6**

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	ECV_OC	DSMON_HEAT	HS0_OC	HS15_OC	HS14_OC	HS13_OC	HS12_OC	HS11_OC	HS10_OC	HS9_OC	HS8_OC	HS7_OC	HB6_LS_OC	HB6_HS_OC	HB5_LS_OC	HB5_HS_OC	HB4_LS_OC	HB4_HS_OC	HB3_LS_OC	HB3_HS_OC	HB2_LS_OC	HB2_HS_OC	HB1_LS_OC	HB1_HS_OC
Access	R&C																							

Table 136. **Status register 6 description**

Bit	Name	Description
23	ECV_OC	Electro chrome overcurrent shutdown: ‘1’ indicates the output was shut down due to overcurrent condition. Bit is latched until a “Read & Clear” command
22	DSMON_HEAT	Drain-source monitoring heater output ‘1’ indicates a short-circuit condition was detected Bit is latched until a “Read & Clear” command
21	HS0_OC	HS0 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition. Bit is latched until a “Read & Clear” command
20	HS15_OC	HS15 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
19	HS14_OC	HS14 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
18	HS13_OC	HS13 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
17	HS12_OC	HS12 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
16	HS11_OC	HS11 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
15	HS10_OC	HS10 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
14	HS9_OC	HS9 overcurrent shutdown ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
13	HS8_OC	HS8 overcurrent shutdown: ‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
12	HS7_OC	HS7 overcurrent shutdown:

Bit	Name	Description
		‘1’ indicates the output was shutdown due to overcurrent condition Bit is latched until a “Read & Clear” command
11	HB6_LS_OC	HB6 overcurrent shutdown:
10	HB6_HS_OC	‘1’ indicates the output was shutdown due to overcurrent condition. If overcurrent recovery is disabled (CR13: HB6_OCR = 0): Bit is set upon overcurrent condition and HB6 is turned off If overcurrent recovery is enabled (CR13: HB6_OCR = 1): in case of overcurrent condition this bit is not set. The HB6 goes into Overcurrent Recovery mode. Bit is latched until a “Read & Clear” command
9	HB5_LS_OC	HB5 overcurrent shutdown:
8	HB5_HS_OC	‘1’ indicates the output was shutdown due to overcurrent condition If overcurrent recovery is disabled (CR13: HB5_OCR = 0): bit is set upon overcurrent condition and HB5 is turned off If overcurrent recovery is enabled (CR13: HB5_OCR = 1): in case of overcurrent condition this bit is not set. The HB5 goes into overcurrent recovery mode Bit is latched until a “Read & Clear” command
7	HB4_LS_OC	HB4 overcurrent shutdown:
6	HB4_HS_OC	‘1’ indicates the output was shutdown due to overcurrent condition. If overcurrent recovery is disabled (CR13: HB4_OCR = 0): bit is set upon overcurrent condition and HB4 is turned off If overcurrent recovery is enabled (CR13: HB4_OCR = 1): In case of overcurrent condition this bit is not set. The HB4 goes into overcurrent recovery mode Bit is latched until a “Read & Clear” command
5	HB3_LS_OC	HB3 overcurrent shutdown:
4	HB3_HS_OC	‘1’ indicates the output was shutdown due to overcurrent condition If overcurrent recovery is disabled (CR13: HB3_OCR = 0): bit is set upon overcurrent condition and HB3 is turned off If overcurrent recovery is enabled (CR13: HB3_OCR = 1): in case of overcurrent condition this bit is not set. The HB3 goes into overcurrent recovery mode Bit is latched until a “Read & Clear” command
3	HB2_LS_OC	HB2 overcurrent shutdown:
2	HB2_HS_OC	‘1’ indicates the output was shutdown due to overcurrent condition If overcurrent recovery is disabled (CR13: HB2_OCR = 0): bit is set upon overcurrent condition and HB2 is turned off If overcurrent recovery is enabled (CR13: HB2_OCR = 1): in case of overcurrent condition this bit is not set. The HB2 goes into overcurrent recovery mode Bit is latched until a “Read & Clear” command
1	HB1_LS_OC	HB1 overcurrent shutdown:
0	HB1_HS_OC	‘1’ indicates the output was shutdown due to overcurrent condition If overcurrent recovery is disabled (CR13: HB1_OCR = 0): bit is set upon overcurrent condition and HB1 is turned off If overcurrent recovery is enabled (CR13: HB1_OCR = 1): in case of overcurrent condition this bit is not set. The HB1 goes into overcurrent recovery mode Bit is latched until a “Read & Clear” command

6.5.7 Status register 7 (0x07)

Table 137. Status register 7

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	LIN_PERM_DOM	LIN_TXD_DOM	LIN_PERM_REC	CAN_RXD_REC	CAN_PERM_REC	CAN_PERM_DOM	CAN_TXD_DOM	CANTO	DSMON_HS2	DSMON_HS1	DSMON_LS2	DSMON_LS1	SPI_INV_CMD	SPI_SCK_CNT	CP_LOW	TW	V2SC	V2FAIL	V1FAIL	RESERVED	VSREG_OV	VSREG_UV	VS_OV	VS_UV
Access	R&C																			R	R&C			

Table 138. Status register 7 description

Bit	Name	Description
23	LIN_PERM_DOM	LIN bus signal dominant timeout LIN bus signal is dominant for t > $T_{dom(bus)}$ Bit is latched until a “Read & Clear” command
22	LIN_TXD_DOM	LIN TXD signal dominant timeout TXDL pin is dominant for t > $t_{dom(TXDL)}$ The LIN transmitter is disabled until the bit is cleared. Bit is latched until a “Read & Clear” command
21	LIN_PERM_REC	LIN bus signal permanent recessive LIN bus signal does not follow TXDL within t_{LIN} The LIN transmitter is disabled until the bit is cleared. Bit is latched until a “Read & Clear” command
20	CAN_RXD_REC	CAN RXD signal permanent recessive RXDC has not followed TXDC for 4 times The CAN transmitter is disabled until the bit is cleared. Bit is latched until a “Read & Clear” command
19	CAN_PERM_REC	CAN bus signal permanent recessive CAN bus signal did not follow TXDC for 4 times The CAN transmitter is disabled until the bit is cleared. Bit is latched until a “Read & Clear” command
18	CAN_PERM_DOM	CAN bus signal permanent dominant CAN bus signal is dominant for t > t_{CAN} Bit is latched until a “Read & Clear” command
17	CAN_TXD_DOM	CAN TXD signal permanent dominant TXDC pin is dominant for t > $t_{dom(TXDC)}$ The CAN transmitter is disabled until the bit is cleared. Bit is latched until a “Read & Clear” command
16	CANTO	CAN communication timeout Bit is set if there is no communication on the bus for t > $t_{Silence}$; CANTO indicates that there was a transition from BIAS ON to BIAS OFF Bit is latched until a “Read & Clear” command
15	DSMON_HS2	Drain-source monitoring HS2 ‘1’ indicates a short-circuit or open-load condition was detected Bit is latched until a “Read & Clear” command
14	DSMON_HS1	Drain-source monitoring HS1 ‘1’ indicates a short-circuit or open-load condition was detected Bit is latched until a “Read & Clear” command
13	DSMON_LS2	Drain-source monitoring LS2

Bit	Name	Description
		‘1’ indicates a short-circuit or open-load condition was detected Bit is latched until a “Read & Clear” command
12	DSMON_LS1	Drain-source monitoring LS1 ‘1’ indicates a short-circuit or open-load condition was detected Bit is latched until a “Read & Clear” command
11	SPI_INV_CMD	Invalid SPI command ‘1’ indicates one of the following conditions was detected: • Access to undefined address • Write operation to Status Register • DI stuck at '0' or '1' • CSN timeout • Parity failure • Invalid or undefined setting The SPI frame is ignored. Bit is latched until a “Read & Clear” command
10	SPI_SCK_CNT	SPI clock counter ‘1’ indicates an SPI frame with wrong number of CLK cycles was detected Bit is latched until a “Read & Clear” command
9	CP_LOW	Charge pump voltage low ‘1’ indicates that the charge pump voltage is too low Bit is latched until a “Read & Clear” command
8	TW	Thermal warning ‘1’ indicates the temperature has reached the thermal warning threshold Bit is latched until a “Read & Clear” command
7	V2SC	V2 short-circuit detection ‘1’ indicates a short-circuit to GND condition of V2 at turn on of the regulator ($V2 < V2_{fail}$ for $t > t_{v2short}$) Bit is latched until a “Read & Clear” command
6	V2FAIL	V2 failure detection ‘1’ indicates a V2 fail event occurred since last readout ($V2 < V2_{fail}$ for $t > t_{v2fail}$) Bit is latched until a “Read & Clear” command
5	V1FAIL	V1 failure detection ‘1’ indicates a V1 fail event occurred since last readout ($V1 < V1_{fail}$ for $t > t_{v1fail}$) Bit is latched until a “Read & Clear” command
4	RESERVED	-
3	VSREG_OV	Vsreg overvoltage ‘1’ indicates the voltage at Vsreg has reached the overvoltage threshold Bit is latched until a “Read & Clear” command
2	VSREG_UV	Vsreg under voltage ‘1’ indicates the voltage at Vsreg has reached the undervoltage threshold Bit is latched until a “Read & Clear” command
1	VS_OV	Vs overvoltage ‘1’ indicates the voltage at Vs has reached the overvoltage threshold Bit is latched until a “Read & Clear” command
0	VS_UV	Vs under voltage ‘1’ indicates the voltage at Vs has reached the undervoltage threshold Bit is latched until a “Read & Clear” command

6.5.8 Status register 8 (0x08)

Table 139. Status register 8

	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit name	EI2_WAKE	RESERVED	RESERVED	EI1_WAKE	WAKE_CAN	WAKE_LIN	WAKE_TIMER	DEBUG_ACTIVE	V1UV	V1_RESTART_2	V1_RESTART_1	V1_RESTART_0	WDFAIL_CNT_3	WDFAIL_CNT_2	WDFAIL_CNT_1	WDFAIL_CNT_0	DEVICE_STATE_1	DEVICE_STATE_0	TSD2	TSD1	FORCED_SLEEP_TSD2_V1SC	FORCED_SLEEP_WD	WDFAIL	VPOR
Access	R&C	R		R&C																				

Table 140. Status register 8 description

Bit	Name	Description
23	EI2_WAKE	External interrupt 2 wake-up '1' means wake-up from external interrupt 2 Bit is latched until a "Read & Clear" command
22:21	RESERVED	-
20	EI1_WAKE	External interrupt 1 wake-up '1' means wake-up from external interrupt Bit is latched until a "Read & Clear" command
19	WAKE_CAN	Wake-up from CAN '1' means wake-up from CAN Bit is latched until a "Read & Clear" command
18	WAKE_LIN	Wake-up from LIN '1' means wake-up from LIN Bit is latched until a "Read & Clear" command
17	WAKE_TIMER	Wake-up from timer '1' means wake-up from timer Bit is latched until a "Read & Clear" command
16	DEBUG_ACTIVE	Debug mode active '1' means debug mode Bit is latched until a "Read & Clear" command
15	V1UV	Voltage regulator V1 undervoltage '1' indicates undervoltage condition at voltage regulator V1 (V1 < V_{RTx}) Bit is latched until a "Read & Clear" command
14	V1_RESTART_2	Voltage regulator V1 restart Indicates the number of TSD2 events that caused a restart of voltage regulator V1 Bits cannot be cleared; the counter is cleared automatically if no additional TSD2 event occurs within 1 minute
13	V1_RESTART_1	
12	V1_RESTART_0	
11	WDFAIL_CNT_3	Watchdog failure counter Indicates number of subsequent watchdog failures Bits cannot be cleared; is cleared with a valid watchdog trigger
10	WDFAIL_CNT_2	
9	WDFAIL_CNT_1	
8	WDFAIL_CNT_0	
7	DEVICE_STATE_1	V2 short-circuit detection **Actual state** 00 active mode after power-on or after "Read & Clear" command
6	DEVICE_STATE_0	

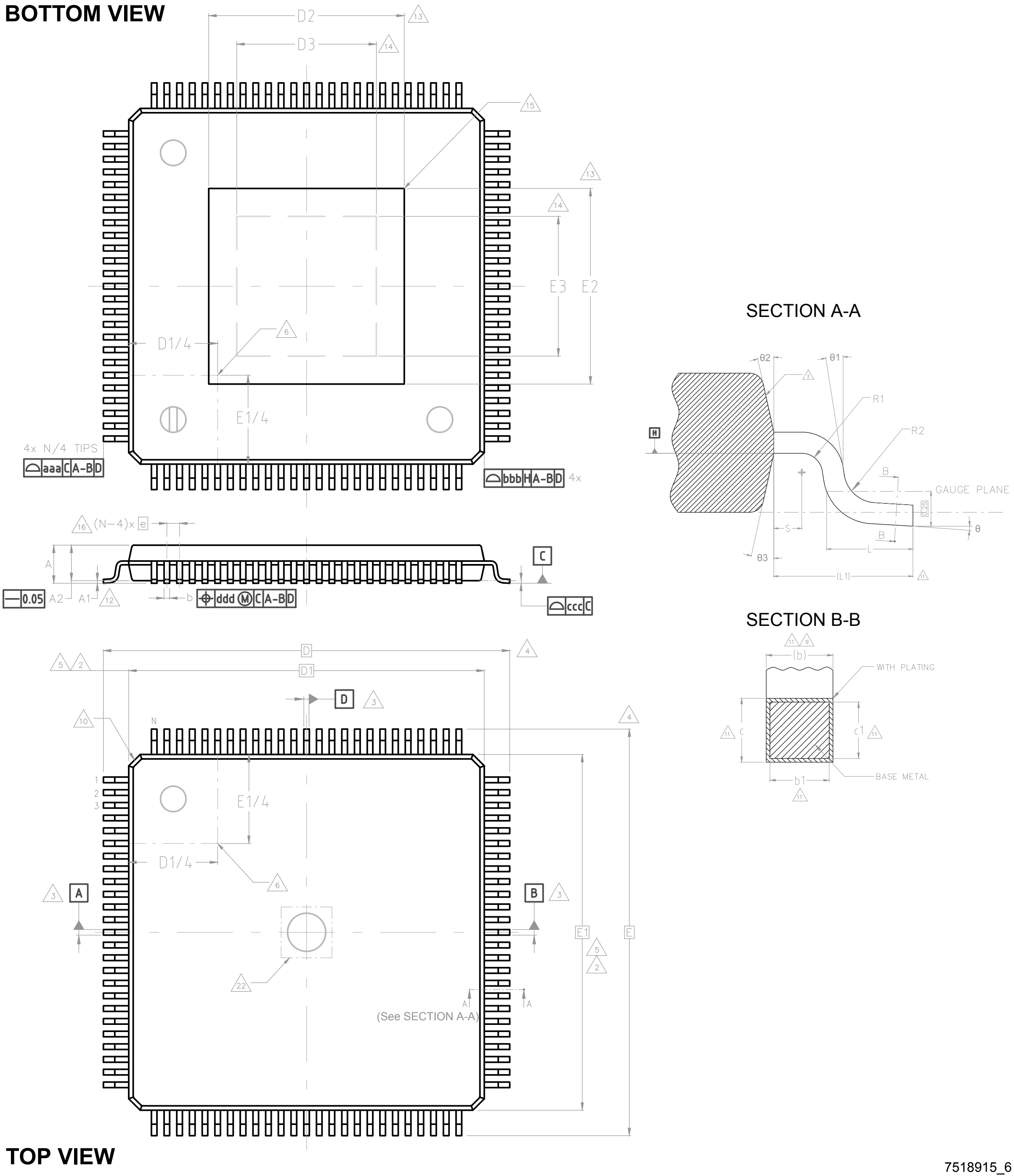
Bit	Name	Description
		01 active mode after wake-up from V1_Standby mode (before “Read & Clear” command) 10 active mode after wake-up from VBAT_Standby mode (before “Read & Clear” command) 11 not used Bit is latched until a “Read & Clear” command; after a “Read & Clear access”, the device state is updated
5	TSD2	Thermal shutdown 2 ‘1’ indicates thermal shutdown 2 was reached Bit is latched until a “Read & Clear” command
4	TSD1	Thermal shutdown 1 ‘1’ indicates thermal shutdown 1 was reached Bit is latched until a “Read & Clear” command
3	FORCED_SLEEP_TSD2_V1SC	Forced sleep TSD2 / V1 short-circuit Device entered forced sleep mode due to: • Thermal shutdown or • Short-circuit on V1 during startup Bit is latched until a “Read & Clear” command
2	FORCED_SLEEP_WD	Forced sleep watchdog Device entered forced sleep mode due to multiple watchdog failures Bit is latched until a “Read & Clear” command
1	WDFAIL	Watchdog failure Watchdog failure Bit is latched until a “Read & Clear” command
0	VPOR	Power-on Reset: VSREG Power-on Reset threshold (V_{POR}) reached Bit is latched until a “Read & Clear” command *Note: If VPOR is set after a cold startup, the device comes from a power on reset.*

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 LQFP100 14x14 mm (exposed pad down) package information

Figure 47. LQFP100 14x14 mm (exposed pad down) package outline



7518915_6

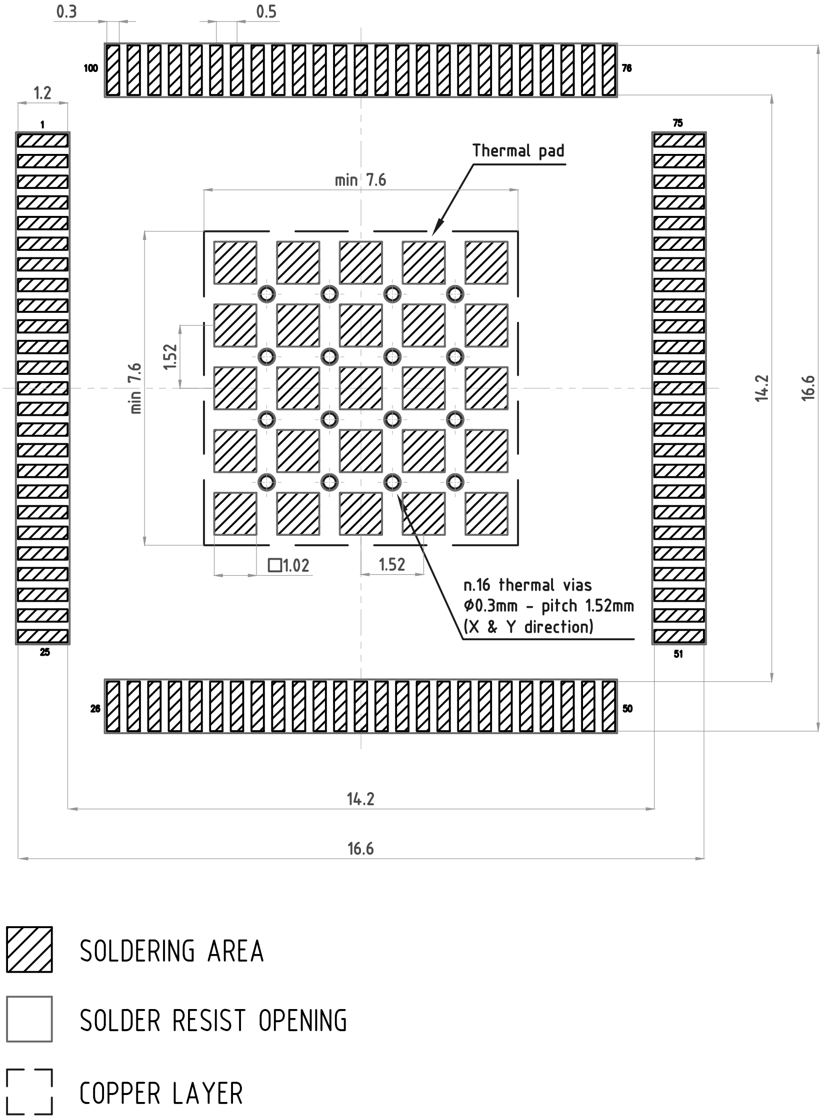
Table 141. LQFP100 14x14 mm (exposed pad down) mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°		
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09		0.20
c1	0.09		0.16
D	16.00 BSC		
D1	14.00 BSC		
D2 = E2			7.95
D3 = E3	6.34		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
N	100		
R1	0.08		
R2	0.08		0.20
S	0.20		

Table 142. LQFP100 14x14 mm (exposed pad down) tolerance of form and position

Symbol	Millimeters
aaa	0.20
bbb	0.20
ccc	0.008
ddd	0.008

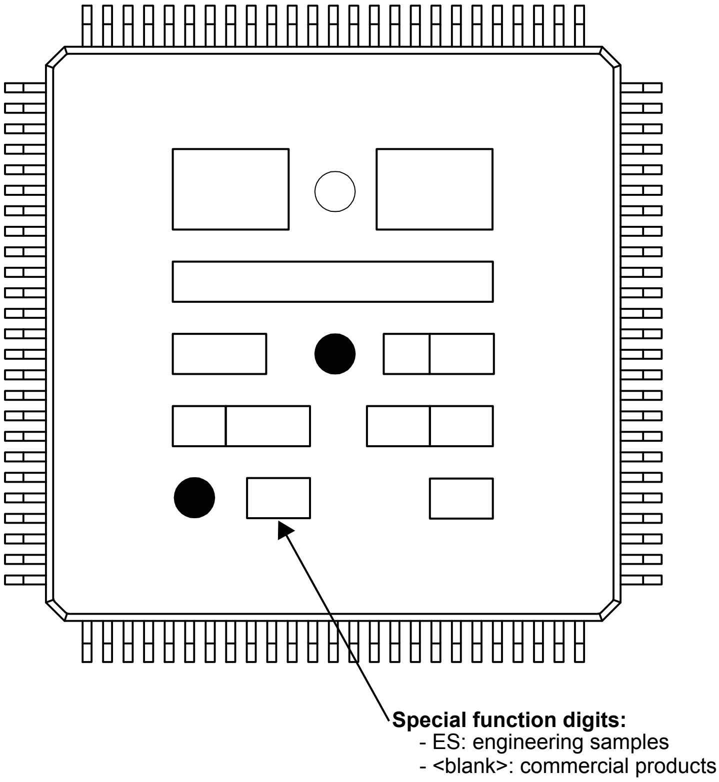
Figure 48. LQFP100 14x14 mm (exposed pad down) footprint



7518915_6_Footprint

7.2 LQFP100 marking information

Figure 49. **LQFP100 marking information**



Parts marked as ES are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event ST is liable for the customer using any of these engineering samples in production. ST's quality department must be contacted to run a qualification activity before any decision to use these engineering samples.

Revision history

Table 143. Document revision history

Date	Revision	Changes
02-Aug-2022	1	Initial release.
21-Feb-2023	2	Updated title, *Features* and *Device summary* on cover page. Updated *Figure 1. Block diagram*. Updated *Section 2.1 Absolute maximum ratings*, *Section 2.2 ESD protection*, *Section 2.4 Electrical characteristics*, *Table 7*, *Table 10*, *Table 11*, *Table 12*, *Table 13*, *Table 14*, *Table 16*, *Table 18*, *Table 21*, *Table 22*, *Table 23*, *Table 27*, *Table 36*, *Table 37*, *Table 41*, *Table 46*, *Table 48* and *Table 49*. Updated *Section 3.2.1 Voltage regulator V1*, *Section 3.3.5 VBAT_Standby mode*, *Table 54*, *Section 3.9.1 Features*, *Section 3.10.1 Features*, *Section 3.12.2 VSREG supply failure*, *Section 3.14 Power outputs HB1,..., HB6, HB20, HB21, HS7,..., HS15, HS0, HS16,..., HS19*, *Section 3.15 Charge pump*, *Section 3.18 Overcurrent detection*, *Section 3.19 Short-circuit current detection*, *Section 3.21 PWM mode of the power outputs*, *Table 60*, *Figure 39* and *Section 3.33 Digital thermal clusters*. Updated *Section 5 Application circuit*. Added "Reset value" in *Section 6.4 Control registers* and updated x*Section 6.2 Control registers overview*, *Section 6.3 Status register overview*, *Table 82*, *Table 93*, *Table 94*, *Table 102*, *Table 103*, *Table 113*, *Table 123*, *Table 126* and *Table 139*. Minor text changes.
10-Nov-2023	3	Updated *Table 5*, *Table 7*, *Table 11*, *Table 14*, *Table 16*, *Table 17*, *Table 18*, *Table 27*, *Table 37*, *Table 41* and *Table 44*. Updated *Section 3.1 Supply VS, VSREG, Section 3.3.3 V1_Standby mode*, *Section 3.3.5 VBAT_Standby mode*, *Section 3.7.1 Temporary failures* and *Section 3.10.2 CAN transceiver operating modes*. Updated *Section 5 Application circuit*. Updated *Table 82* and *Table 113*. Minor text changes
31-Jul-2024	4	Updated *Figure 2. Pin connection (top view)*, *Table 1. Pin function*, *Table 7. Supply monitoring and current consumption*, *Figure 22. Transceiver state diagram*, *Figure 40. Digital thermal clusters identification, Table 96. CR31 signals description*. Minor text changes.
26-Sep-2024	5	Updated Table 11. Voltage regulator 2, Section 3.2.2: Voltage regulator V2, Section 3.7.1: Temporary failures, Section 3.9.1: Features, Section 3.10.3: CAN error handling, Table 78. Control registers overview and Table 82. CR1 signals description.

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