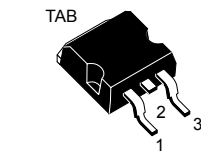
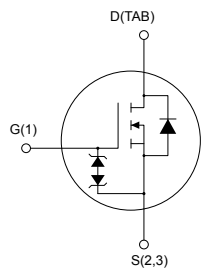


Automotive-grade N-channel 1200 V, 0.62 Ω typ., 12 A, MDmesh K5 Power MOSFET in an H²PAK-2 package


H²PAK-2



NCHG10TAB523TZ


Product status link
[STH13N120K5-2AG](#)
Product summary

Order code	STH13N120K5-2AG
Marking	13N120K5
Package	H ² PAK-2
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STH13N120K5-2AG	1200 V	0.69 Ω	12 A	250 W

- AEC-Q101 qualified 
- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current at $T_C = 25\text{ }^\circ\text{C}$	12	A
	Drain current at $T_C = 100\text{ }^\circ\text{C}$	7.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
$I_{AR}^{(2)}$	Maximum current during repetitive or single-pulse avalanche	4	A
$E_{AS}^{(3)}$	Single-pulse avalanche energy	215	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(5)}$	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature range	-55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.
2. Pulse width limited by T_{Jmax} .
3. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$
4. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS (peak)} \leq V_{(BR)DSS}$
5. $V_{DS} \leq 960\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch², 2oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	1200			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$, $T_c = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$		0.62	0.69	Ω

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	1370	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{riss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }960\text{ V}$	-	128	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	42	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	3	-	Ω
Q_g	Total gate charge	$V_{DD} = 960\text{ V}$, $I_D = 12\text{ A}$	-	44.2	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	7.3	-	nC
Q_{gd}	Gate-drain charge	(see Figure 15. Test circuit for gate charge behavior)	-	30	-	nC

1. Time-related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .
2. Energy-related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 600\text{ V}$, $I_D = 6\text{ A}$,	-	23	-	ns
t_r	Rise time	$R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	11	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	68.5	-	ns
t_f	Fall time		-	18.5	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}	Source-drain current (pulsed)		-		48	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12\text{ A}, V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}, V_{DD} = 60\text{ V}$	-	630		ns
Q_{rr}	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$,	-	12.6		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	40		A
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}, V_{DD} = 60\text{ V}$	-	892		ns
Q_{rr}	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}, T_j = 150\text{ }^\circ\text{C}$	-	15.6		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	35		A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 7. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D = 0\text{ A}$	30	-		V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

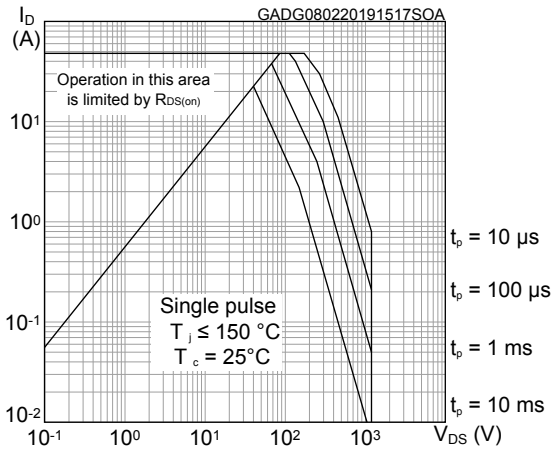


Figure 2. Normalized transient thermal impedance

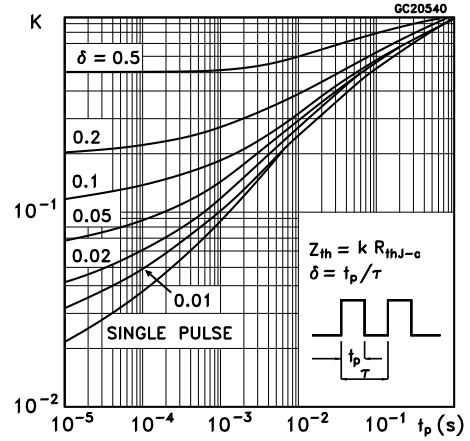


Figure 3. Typical output characteristics

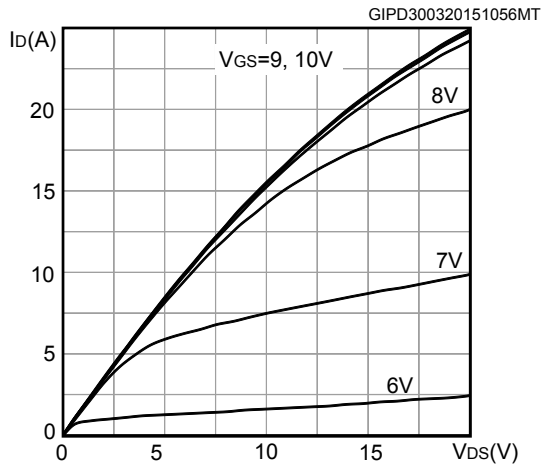


Figure 4. Typical transfer characteristics

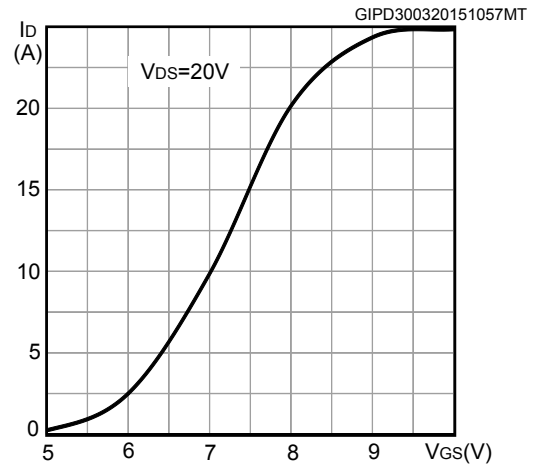


Figure 5. Typical gate charge characteristics

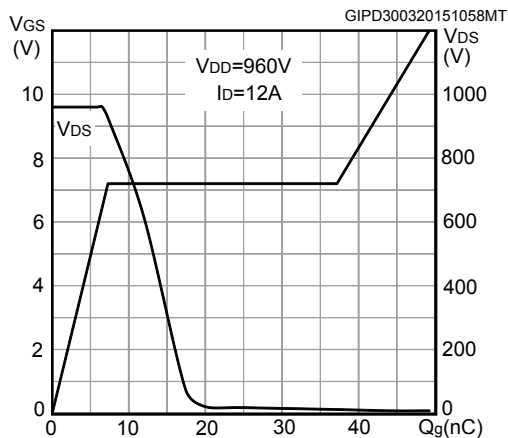


Figure 6. Typical drain-source on-resistance

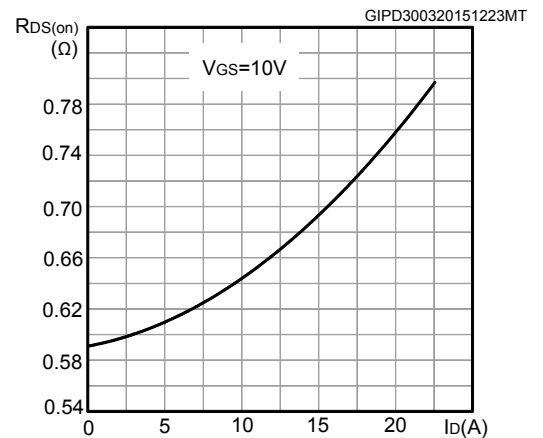


Figure 7. Typical capacitance characteristics

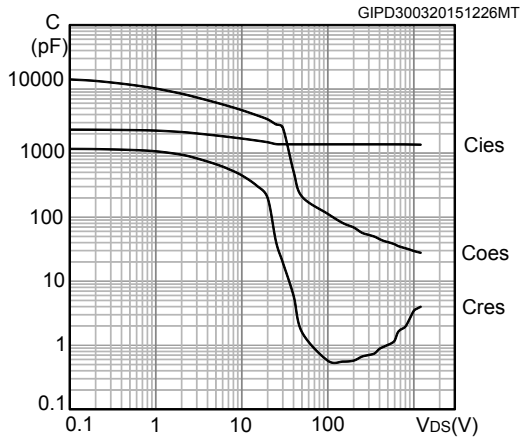


Figure 8. Typical output capacitance stored energy

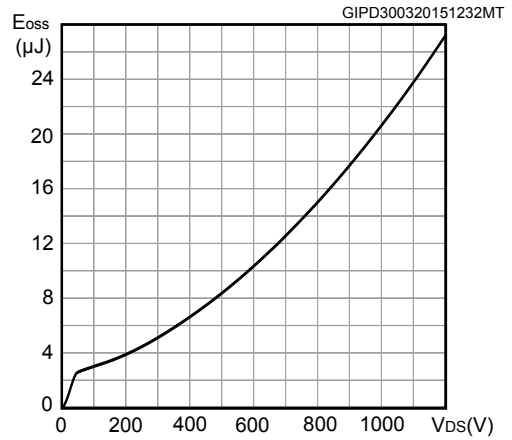


Figure 9. Normalized gate threshold vs temperature

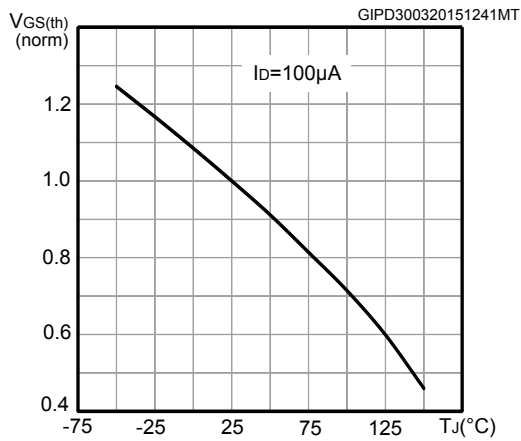


Figure 10. Normalized on-resistance vs temperature

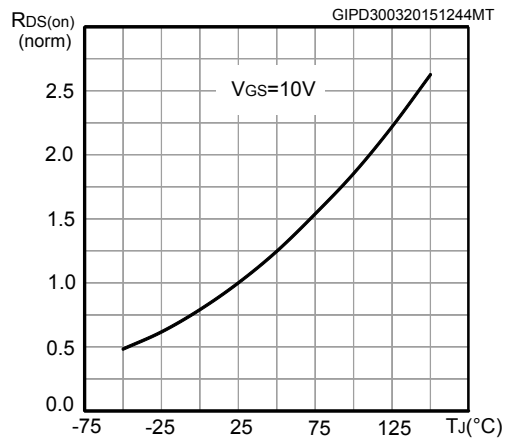


Figure 11. Normalized breakdown voltage vs temperature

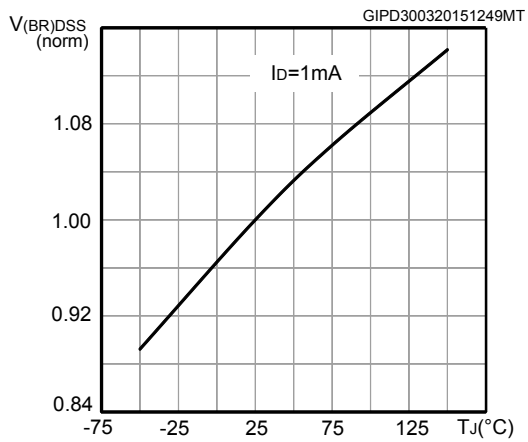


Figure 12. Typical reverse diode forward characteristics

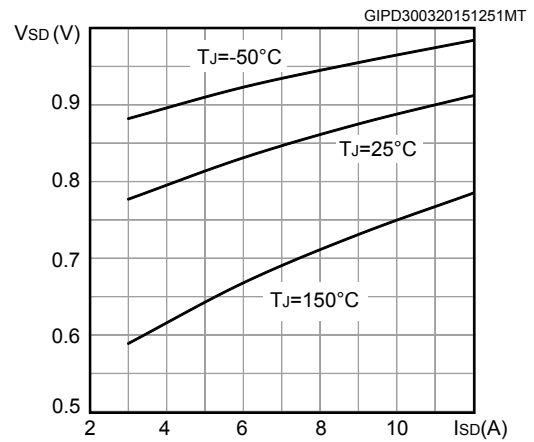
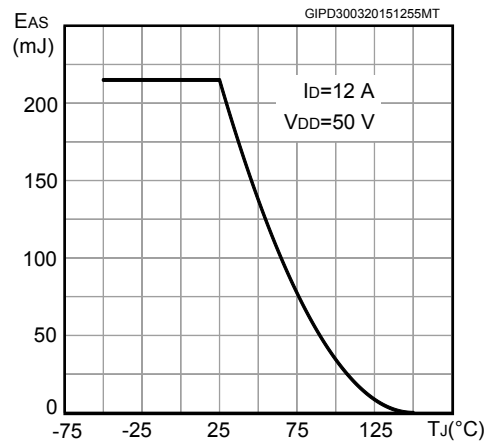
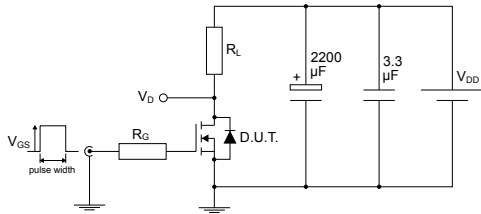


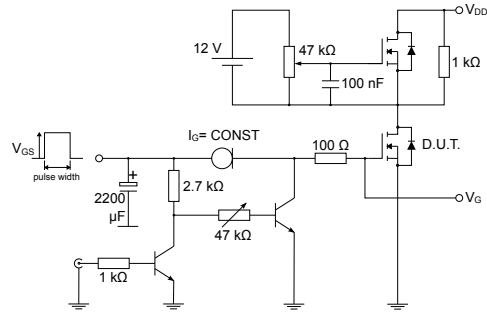
Figure 13. Maximum avalanche energy vs temperature



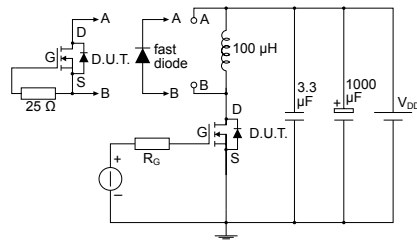
3 Test circuits

Figure 14. Test circuit for resistive load switching times


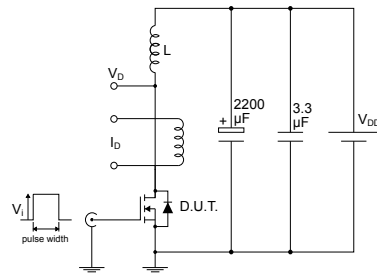
AM01468v1

Figure 15. Test circuit for gate charge behavior


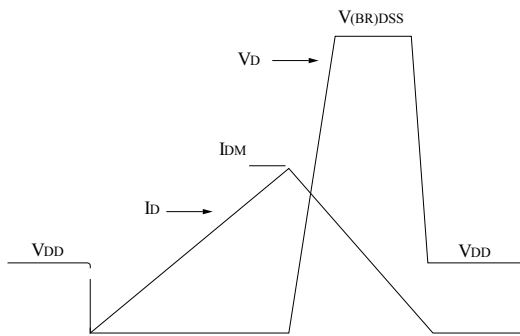
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times


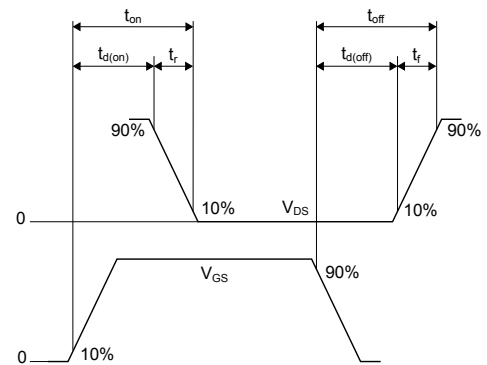
AM01470v1

Figure 17. Unclamped inductive load test circuit


AM01471v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


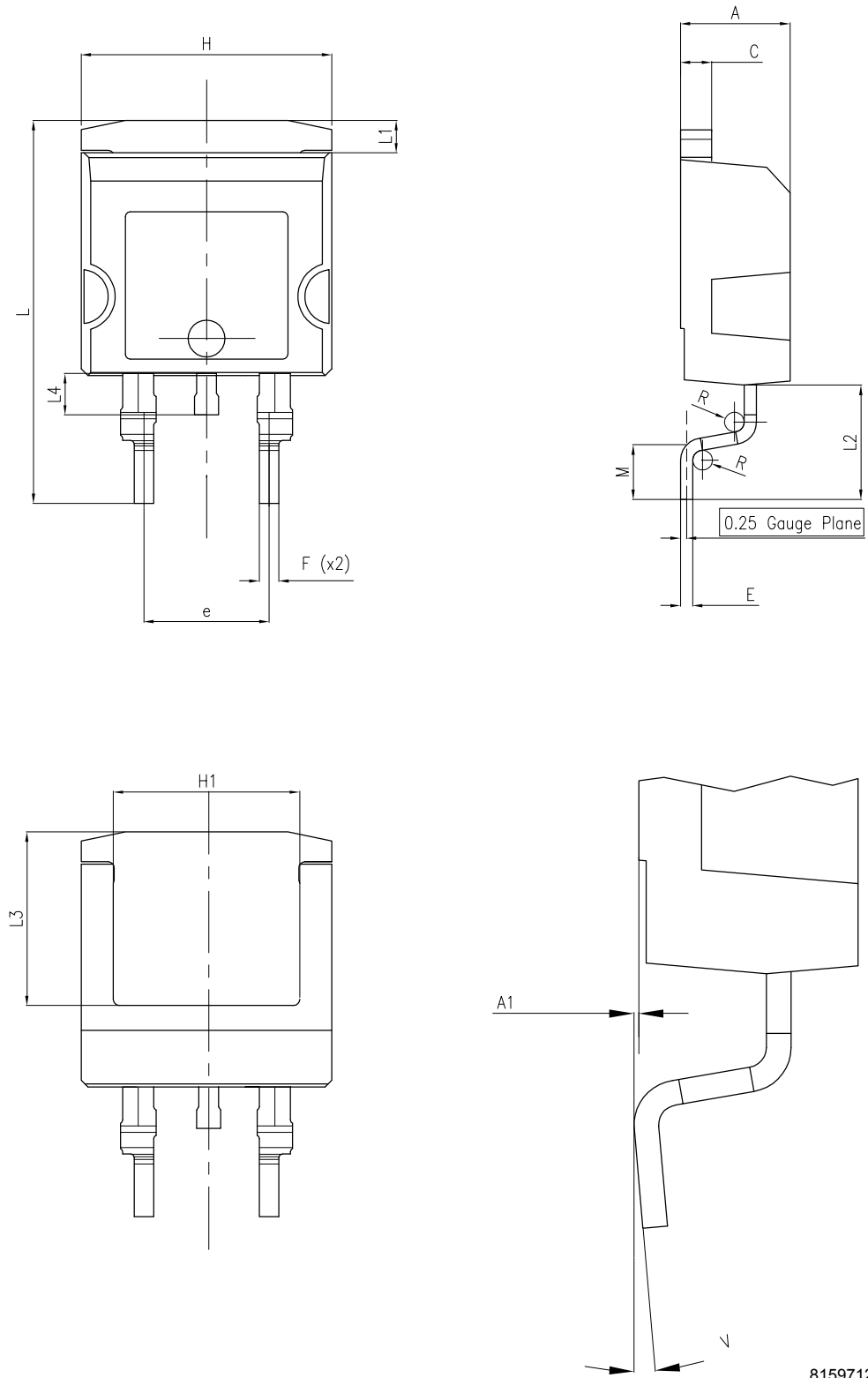
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 20. H²PAK-2 package outline

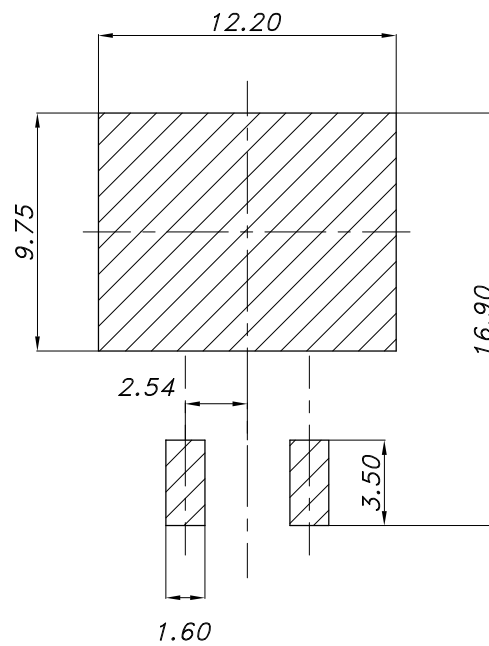


8159712_8

Table 8. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 21. H²PAK-2 recommended footprint

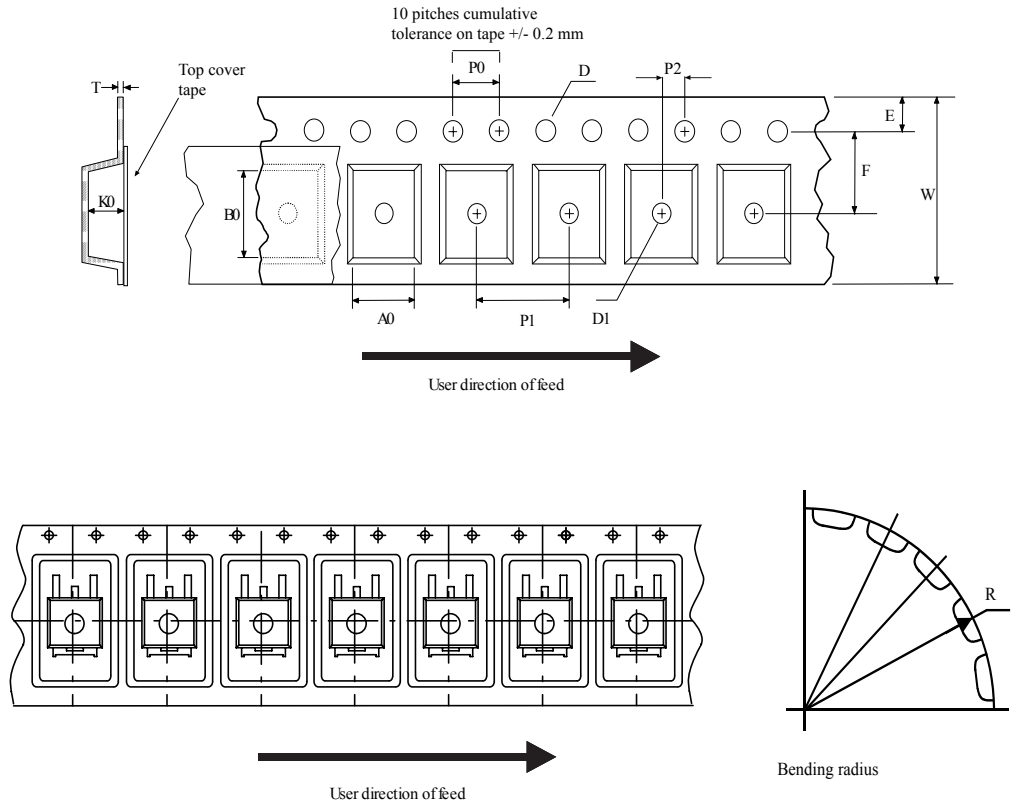


8159712_8

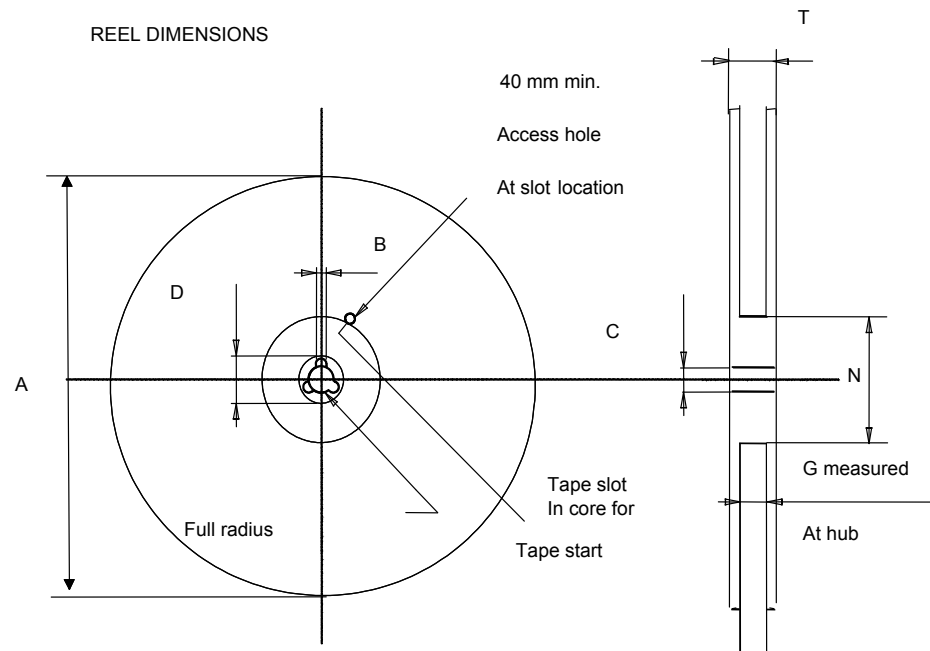
Note: Dimensions are in mm.

4.2 H²PAK-2 packing information

Figure 22. Tape outline



AM08852v2

Figure 23. Reel outline

Table 9. Tape and reel mechanical data

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 10. Document revision history

Date	Version	Changes
14-Feb-2019	1	First release.
10-Sep-2019	2	Updated <i>title</i> and <i>features</i> in cover page. Updated <i>Section 1 Electrical ratings</i> , <i>Section 2 Electrical characteristics</i> and <i>Section 2.1 Electrical characteristics (curves)</i> . Minor text changes.
23-Oct-2019	3	Modified Table 1. Absolute maximum ratings , Table 2. Thermal data , Table 3. On/off states , Table 4. Dynamic , Table 5. Switching times and Table 6. Source-drain diode . Modified Section 2.1 Electrical characteristics (curves) .

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	H ² PAK-2 package information	9
4.2	H ² PAK-2 packing information	11
	Revision history	14

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved