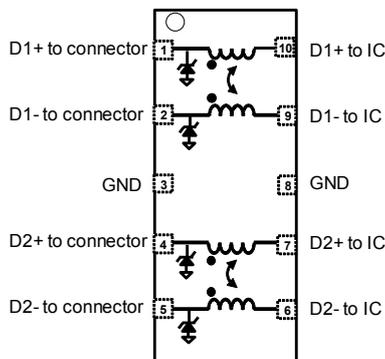


Common mode filter with ESD protection for high speed serial interface



μQFN-10L
1.35 mm x 2.2 mm x 0.5 mm



Product status

ECMF4-2450A60N10

Features

- 6.4 GHz differential bandwidth to comply with HDMI 2.1, HDMI 2.0, HDMI 1.4, USB 3.1 Gen 1 and Gen 2, MIPI, display port, etc.
- High common mode attenuation on WLAN frequencies :
 - From - 30 dB to - 33 dB at 2.4 – 2.47 GHz: Wi-Fi CH1-14 frequencies
 - From - 20 dB to - 15 dB at 5.18 – 5.82 GHz: Wi-Fi CH36-165 frequencies
- Very low PCB space consumption
- Thin package: 0.5 mm max.
- Lead free and RoHS package
- High reduction of parasitic elements through integration
- Exceeds IEC 61000-4-2 level 4 standards:
 - ± 25 kV (air discharge)
 - ± 10 kV (contact discharge)

Applications

- Notebook, laptop
- Streaming box
- Set top box
- Portable devices
- Tablet

Description

The **ECMF4-2450A60N10** is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like HDMI 2.1, HDMI 2.0, HDMI1.4, USB 3.1 Gen 1 and Gen 2, ethernet, MIPI, display port and other high speed serial interfaces.

It has a very large differential bandwidth to comply with these standards and can also protect and filter 2 differential lanes.

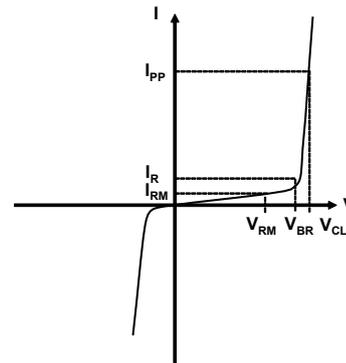
1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ °C}$)

Symbol	Parameter	Value	Unit	
V_{PP}	Peak pulse voltage	IEC 61000-4-2: Contact discharge	10	kV
		Air discharge	25	
I_{RMS}	Maximum RMS current	100	mA	
T_{op}	Maximum operating temperature range	-55 to +125	°C	
T_{stg}	Storage temperature range	-55 to +150		
T_L	Maximum temperature for soldering during 10 s	260		

Figure 1. Electrical characteristics (definitions)

- V_{RM} Maximum stand-off voltage
- V_{CL} Clamping voltage at peak pulse current I_{PP}
- I_{RM} Leakage current at V_{RM}
- I_{PP} Peak pulse current
- V_{BR} Breakdown voltage
- C_{DIODE} ESD diode capacitance
- R_{DC} DC serial resistance
- f_c Differential cut off frequency


Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	5.3	5.8		V
I_{RM}	$V_{RM} = 3.6\text{ V per line}$		< 1	50	nA
	$V_{RM} = 5\text{ V per line}$		3	70	nA
R_{DC}	DC serial resistance, $I_{DC} = 20\text{ mA}$		5		Ω
f_c	Differential mode cut-off frequency at -3 dB		6.4		GHz
V_{CL}	8 kV contact discharge after 30 ns, IEC 61000-4-2		17.3		V
C_{DIODE}	$V_{BIAS} = 0\text{ V}$, $2.5\text{ GHz} \leq f \leq 6\text{ GHz}$, $V_{OSC} = 30\text{ mV}$		0.25	0.40	pF

Table 3. Pin description

Pin number	Description	Pin number	Description
1	D1+ to connector	6	D2- to IC
2	D1- to connector	7	D2+ to IC
3	GND	8	GND
4	D2+ to connector	9	D1- to IC
5	D2- to connector	10	D1+ to IC

1.1 Characteristics curves

Figure 2. Differential attenuation versus frequency ($Z_{0\text{ DIFF}} = 100 \Omega$)

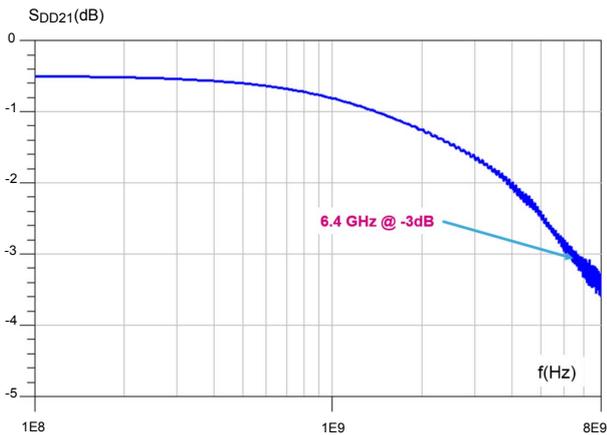


Figure 3. Common mode attenuation versus frequency ($Z_{0\text{ COM}} = 50 \Omega$)

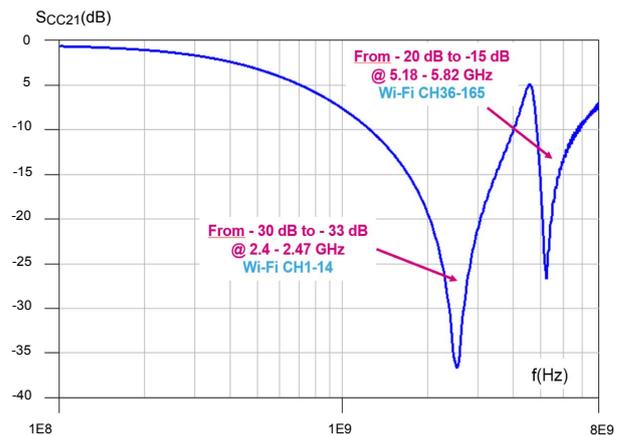


Figure 4. HDMI2.1 12 Gbps eye diagram without ECMF4-2450A60N10 (with worst cable model WCM3), EQ with 8 dB CTLE and one-tap DFE

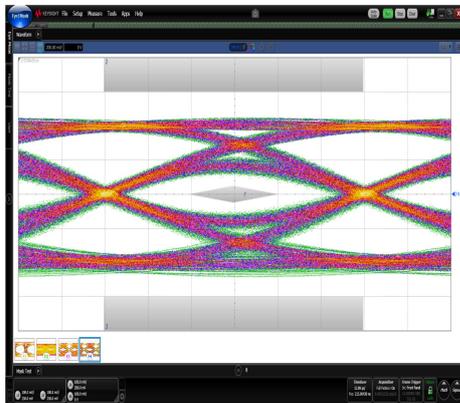


Figure 5. HDMI2.1 12 Gbps eye diagram with ECMF4-2450A60N10 (with worst cable model WCM3), EQ with 8 dB CTLE and one-tap DFE

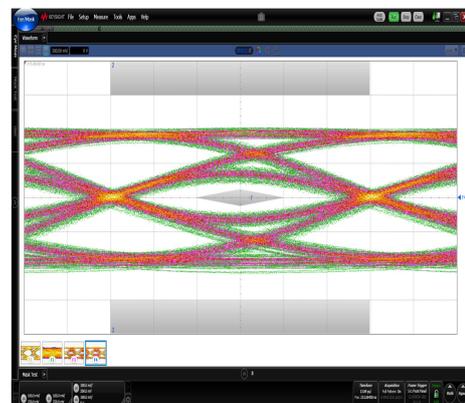


Figure 6. HDMI2.0 5.94 Gbps eye diagram without ECMF4-2450A60N10 (with worst case cable and equalizer)

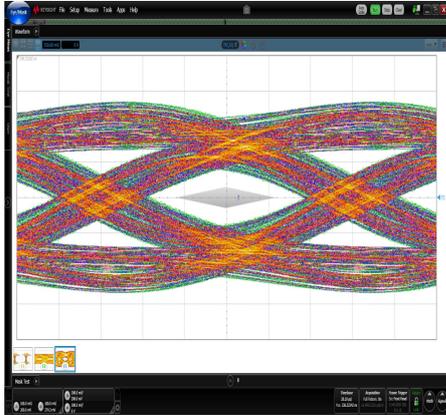


Figure 7. HDMI2.0 5.94 Gbps eye diagram with ECMF4-2450A60N10 (with worst case cable and equalizer)

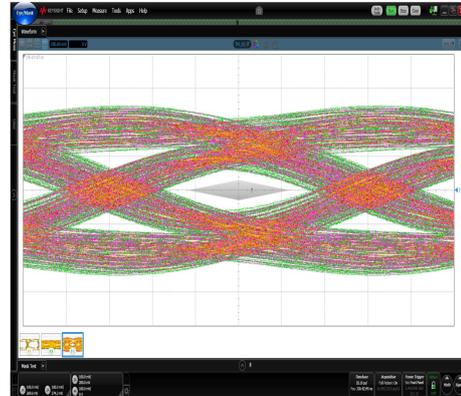


Figure 8. USB3.1 Gen 2 10.0 Gbps eye diagram without ECMF4-2450A60N10 (with type C connector, reference cable, equalizer with $A_{DC} = 6$ dB and DFE)

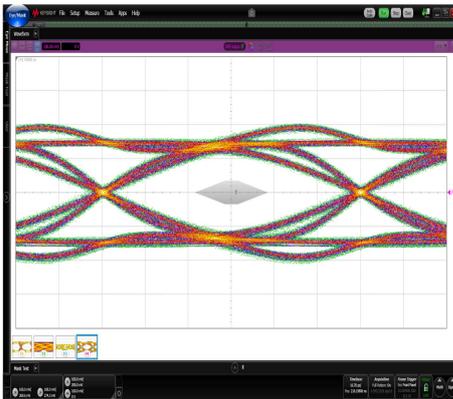


Figure 9. USB3.1 Gen 2 10.0 Gbps eye diagram with ECMF4-2450A60N10 (with type C connector, reference cable, equalizer with $A_{DC} = 6$ dB and DFE)

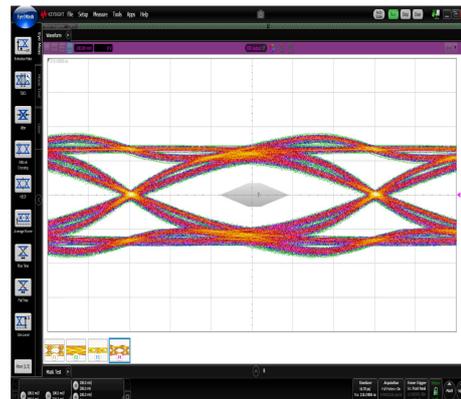


Figure 10. USB3.1 Gen 1 5.0 Gbps eye diagram without ECMF4-2450A60N10 (with type C connector, reference cable and equalizer)

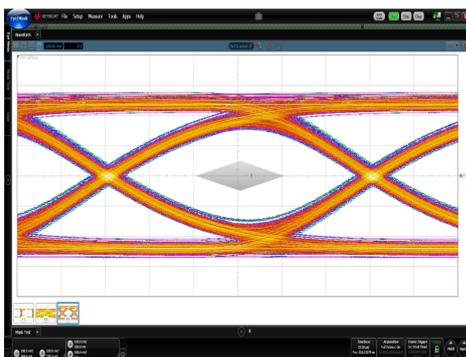


Figure 11. USB3.1 Gen 1 5.0 Gbps eye diagram with ECMF4-2450A60N10 (with type C connector, reference cable and equalizer)

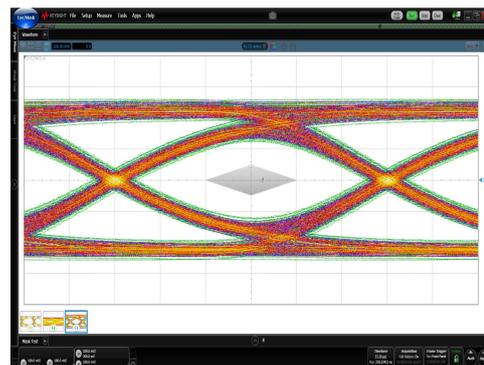


Figure 12. ESD response to IEC61000-4-2 (+8 kV contact discharge)

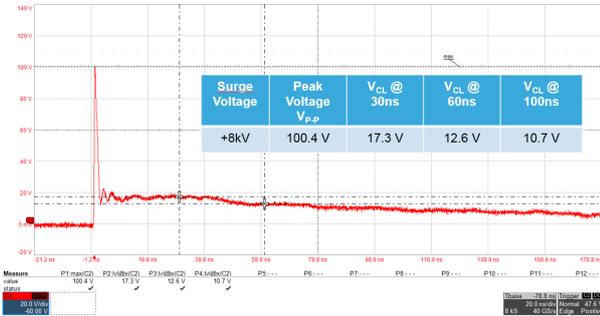


Figure 13. ESD response to IEC61000-4-2 (-8 kV contact discharge)

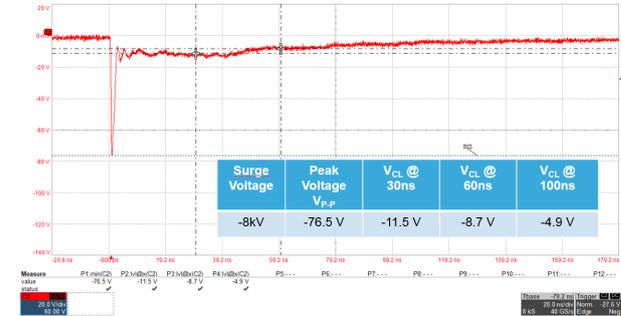
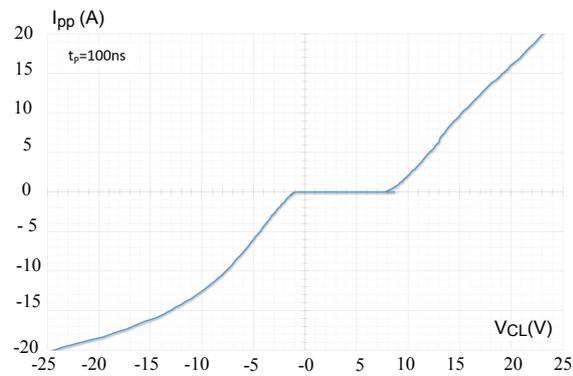


Figure 14. TLP characteristic



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 μ QFN10L package information

Figure 15. μ QFN10L package outline

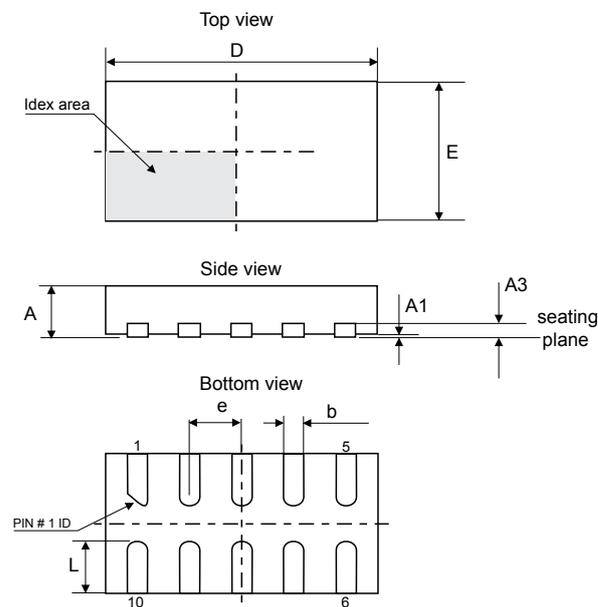
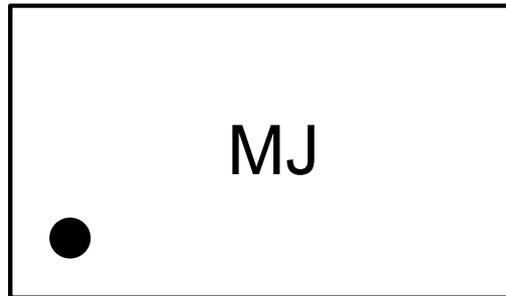
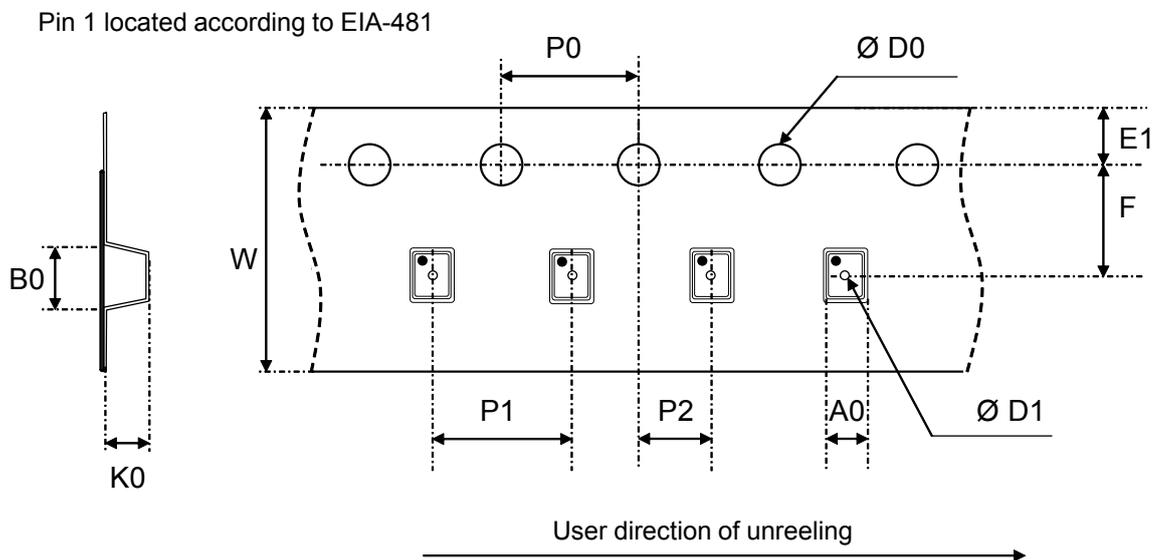


Table 4. μ QFN10L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.41	0.45	0.50
A1	0.00	0.02	0.05
A3		0.127	
b	0.15	0.20	0.25
D	2.15	2.20	2.25
E	1.30	1.35	1.40
e		0.40	
L	0.40	0.50	0.60

Figure 16. Marking layout


Note: The marking codes can be rotated by 90 ° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 17. Tape and reel outline


Note: Pocket dimensions are not on scale
 Pocket shape may vary depending on package

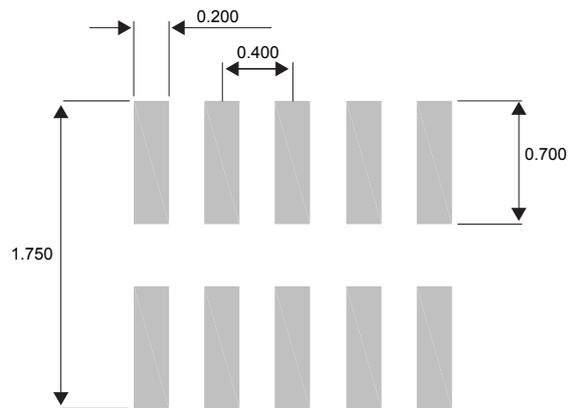
Table 5. Tape and reel mechanical data

Ref.	Dimensions (millimeters)		
	Min.	Typ.	Max.
P1	3.9	4.0	4.1
P0	3.9	4.0	4.1
Ø D0	1.4	1.5	1.6
Ø D1	0.35	0.40	0.45
F	3.45	3.5	3.55
E1	1.65	1.75	1.85
K0	0.6	0.65	0.7
P2	1.95	2	2.05
W	7.9	8	8.1
A0	1.50	1.55	1.60
B0	2.35	2.40	2.45

3 Recommendation PCB assembly

3.1 Footprint

Figure 18. Footprint in mm

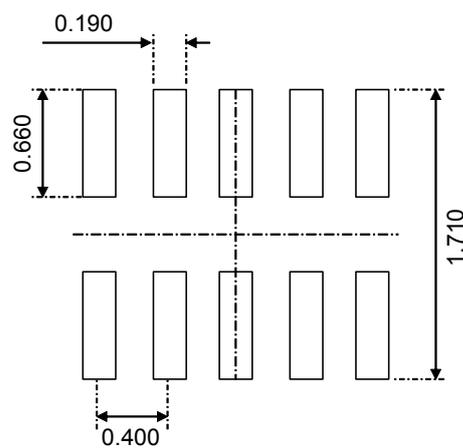


SMD footprint design is recommended.

3.2 Stencil opening design

Recommended design reference: stencil opening thickness: 100 μm

Figure 19. Stencil opening recommendations



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during PCB movement.
4. Solder paste with fine particles: powder particle size is 20-38 μm .

3.4 Placement

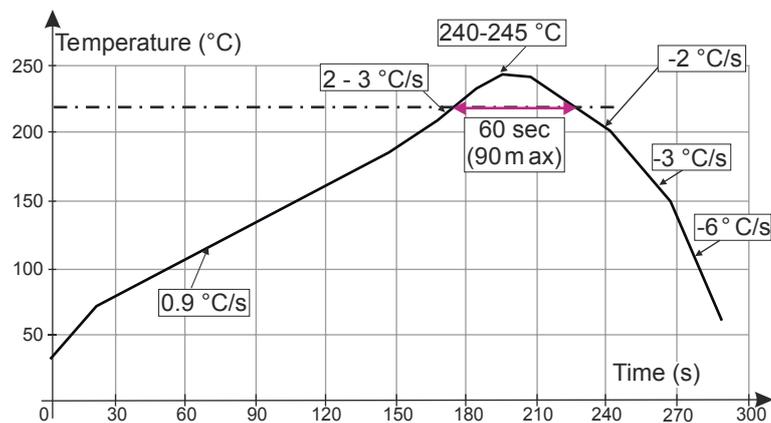
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

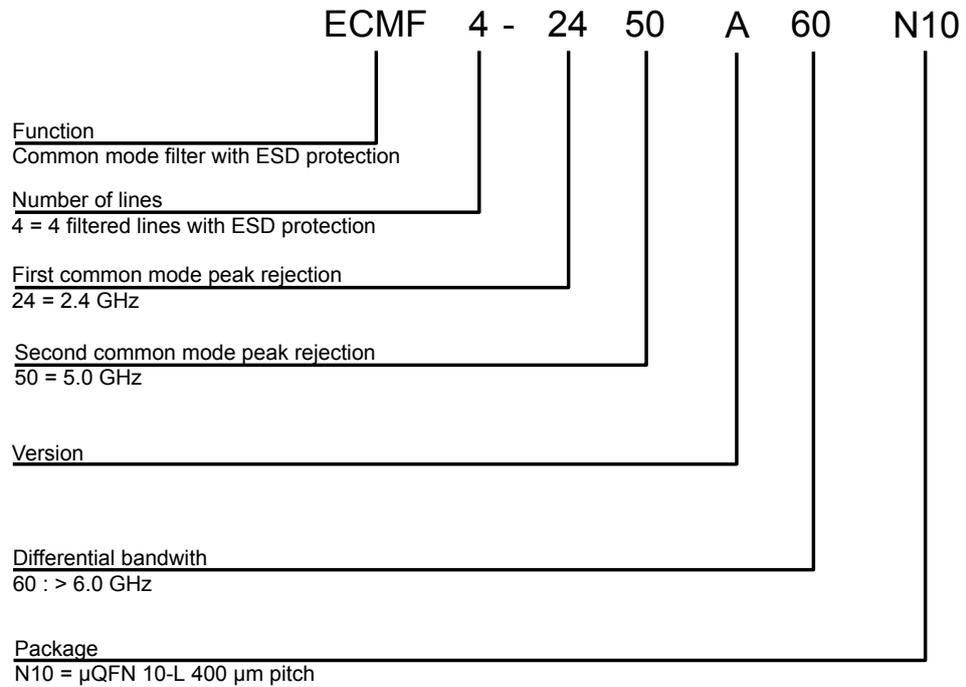
3.6 Reflow profile

Figure 20. ST ECOPACK[®] recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 21. Ordering information scheme

Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ECMF4-2450A60N10	MJ ⁽¹⁾	μ QFN-10L	3.9 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

Revision history

Table 7. Document revision history

Date	Revision	Changes
27-Jul-2018	1	Initial release.
24-Apr-2019	2	Updated Table 6 .

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved