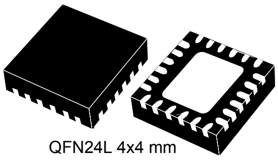
STUSB4500

Datasheet

Standalone USB PD sink controller with short-to-VBUS protections



QFN24L 4x4 mm

Product status link
STUSB4500

Device summary	
Order code	STUSB4500QTR
Description	Standalone USB PD sink controller (auto-run mode)
Package	QFN24 EP 4x4 mm
Marking	4500

Features

- Auto-run Type-C™ and USB PD sink controller
- Dead battery mode support
- Up to 3 sink PDO configurable profiles
- Dual high power charging path support
- Integrated V_{BUS} switch gate drivers (PMOS)
- Integrated V_{BUS} voltage monitoring
- Internal and/or external V_{BUS} discharge paths
- Short-to-VBUS protections on CC pins (22 V)
- High voltage capability on V_{BUS} pins (28 V)
- Dual power supply (V_{SYS} and/or V_{DD}):
  – V_{SYS} = [3.0 V; 5.5 V]
  – V_{DD} = [4.1 V; 22 V]
- Debug accessory mode support
- Temperature range: -40 °C up to 105 °C
- ESD: 3 kV HBM - 1.5 kV CDM
- Certified:
  – USB Type-C™ rev 1.2
  – USB PD rev 2.0 (TID #1000133)
- Interoperable with USB PD rev 3.0

Applications

- Set-top-box, hard disk drives, camcorders, cameras
- IoT, drones, accessories and battery powered devices
- LED lighting and industrial
- Healthcare and handheld devices
- Any Type-C sink device

Description

The STUSB4500 is a USB power delivery controller that addresses sink devices. It implements a proprietary algorithm to allow the negotiation of a power delivery contract with a source without MCU support (auto-run mode). PDO profiles are configured in an integrated non-volatile memory.

The device supports dead battery mode and is suited for sink devices powered from dead battery state and requiring high power charging profile to be fully operational.

Thanks to its 20 V technology, it implements high voltage features to protect the CC pins against short-circuits to V_{BUS} up to 22 V and to support high voltage on the V_{BUS} pins directly connected to the V_{BUS} power path up to 28 V.

1 Functional description

The STUSB4500 is a USB Type-C™ and power delivery controller IC for sink applications. It is able to negotiate a power delivery contract with a source without MCU support (auto-run mode). It relies on proprietary algorithms and configurable PDO (power data objects) thanks to an integrated non-volatile memory. It supports dead battery mode to allow a system to be powered from an external source directly. Combined with its capability to negotiate directly a power contract, the STUSB4500 is the ideal controller device for autonomous systems requiring high power charging profile to be fully operational.

The STUSB4500 major role is to:

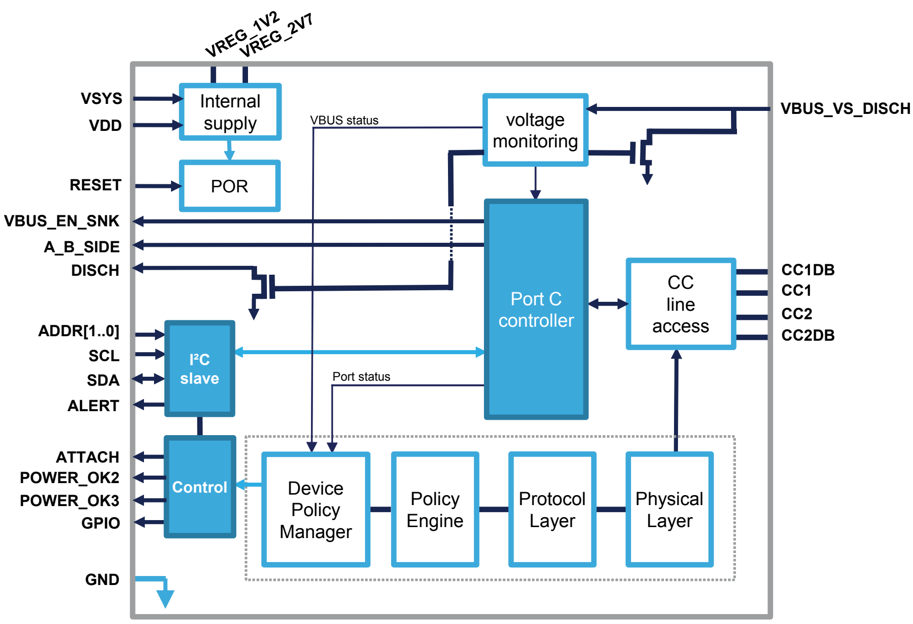
1. Detect the connection between two USB Type-C ports (attach detection)
2. Establish a valid source-to-sink connection
3. Determine the attached device mode: source or debug accessory
4. Resolve cable orientation and twist connections to establish USB data routing (MUX control)
5. Negotiate a USB power delivery (PD) contract with a PD capable source device
6. Configure the incoming V_{BUS} power path and the charging paths accordingly
7. Monitor the V_{BUS} power path and manage the V_{BUS} voltage transitions
8. Handle the high voltage protections

The STUSB4500 also provides:

- Dead battery mode
- PDO (power data object) customization through NVM
- Internal and/or external V_{BUS} discharge paths
- Dual high power charging path support
- Debug accessory mode detection
- Customization of the device configuration through NVM to support specific applications

1.1 Block overview

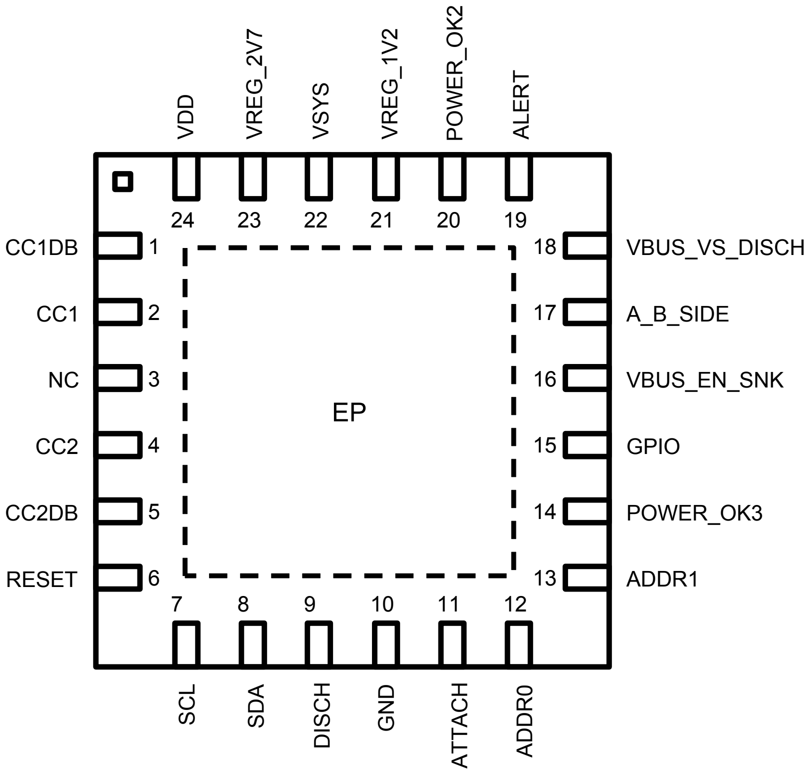
Figure 1. Functional block diagram



2 Inputs/outputs

2.1 Pinout

Figure 2. **STUSB4500 pin connections (top view)**



2.2 Pin list

Table 1. **Pin function list**

Pin	Name	Type	Description	Typical connection
1	CC1DB	HV AIO	Dead battery enable on CC1 pin	To CC1 pin if used or ground
2	CC1	HV AIO	Type-C configuration channel 1	To Type-C receptacle A5
3	NC	-	-	Floating
4	CC2	HV AIO	Type-C configuration channel 2	To Type-C receptacle B5
5	CC2DB	HV AIO	Dead battery enable on CC2 pin	To CC2 pin if used or ground
6	RESET	DI	Reset input, active high	From system
7	SCL	DI	I^2C clock input	To I^2C master, ext. pull-up
8	SDA	DI/OD	I^2C data input/output, active low open drain	To I^2C master, ext. pull-up
9	DISCH	HV AI/OD	Internal discharge path or external discharge path enable, active low open drain	From power system (internal path) or to the discharge path switch (external path), ext. pull-up
10	GND	GND	Ground	Ground
11	ATTACH	OD	Attachment detection, active low open drain	To MCU if any, ext. pull-up
12	ADDR0	DI	I^2C device address setting	Static, to ground or ext. pull-up for address selection, to ground if no connection to MCU
13	ADDR1	DI	I^2C device address setting	Static, to ground or ext. pull-up for address selection, to ground if no connection to MCU
14	POWER_OK3	OD	Power contract flag, active low open drain	To power system, ext. pull-up
15	GPIO	OD	General purpose output, active low open drain	To system, ext. pull-up
16	VBUS_EN_SNK	HV OD	V_{BUS} sink power path enable, active low open drain	To power switch or to power system, ext. pull-up
17	A_B_SIDE	OD	Cable orientation, active low open drain	USB super speed MUX select, ext. pull-up
18	VBUS_VS_DISCH	HV AI	V_{BUS} voltage monitoring and discharge path	From $V_{BUS,}$ receptacle side
19	ALERT	OD	I^2C interrupt, active low open drain	To I^2C master, ext. pull-up
20	POWER_OK2	HV OD	Power contract flag, active low open drain	To power switch or to power system, ext. pull-up
21	VREG_1V2	PWR	1.2 V internal regulator output	1 µF typ. decoupling capacitor
22	VSYS	PWR	Power supply from system	From power system, connect to ground if not used
23	VREG_2V7	PWR	2.7 V internal regulator output	1 µF typ. decoupling capacitor
24	VDD	HV PWR	Power supply from USB power line	From V_{BUS}, receptacle side
-	EP	GND	Exposed pad is connected to ground	To ground

Table 2. **Pin function descriptions**

Type	Description
D	Digital
A	Analog
O	Output pad
I	Input pad
IO	Bidirectional pad
OD	Open drain output
PD	Pull-down
PU	Pull-up
HV	High voltage
PWR	Power
GND	Ground

2.3 Pin description

2.3.1 CC1/CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination, USB power delivery communication, and system configuration management across USB Type-C cable. CC1 and CC2 are HiZ during reset.

2.3.2 CC1DB/CC2DB

CC1DB and CC2DB are used for dead battery mode. This mode is enabled by connecting CC1DB and CC2DB respectively to CC1 and CC2. Thanks to this connection, the pull-down terminations on the CC pins are present by default even if the device is not supplied (see Section 3.5 Dead battery mode).

Warning: CC1DB and CC2DB must be connected to ground when dead battery mode is not supported.

2.3.3 Reset

Active high reset.

2.3.4 I2C interface pins

Table 3. **I²C interface pin list**

Name	Description
SCL	I²C clock, need external pull-up
SDA	I²C data, need external pull-up
ALERT	I²C interrupt, need external pull-up
ADDR0, ADDR1	I²C device address bits (see Section 4 I²C Interface)

Warning: ADDR0 and ADDR1 pins must be connected to ground when there is no connection to an MCU.

2.3.5 DISCH

This input/output pin can be used to implement a discharge path for highly capacitive V_{BUS} line on power system side.

When used as input, the discharge is internal and a serial resistor must connected to the pin to limit the discharge current through the pin. Maximum discharge current is 500 mA.

The pin can be also used as an open drain output to control an external V_{BUS} discharge path when higher discharge current is required by the application, for instance.

The pin is activated at the same time as the internal discharge path on VBUS_VS_DISCH pin. The discharge is activated automatically during cable disconnection, transition to a lower PDO voltage, hard reset and error recovery state. The discharge time is programmable by NVM (see Section 5 Start-up configuration).

2.3.6 GND

Ground.

2.3.7 ATTACH

This pin is asserted when a valid source-to-sink connection is established. It is also asserted when a connection to a debug accessory device is detected.

2.3.8 POWER_OK2/POWER_OK3

These pins report by default the status of the USB power delivery contract negotiation with the source.

Different configurations are proposed as stated in the table below to meet specific application requirements. The configuration of the POWER_OK pins can be changed by NVM programming (see Section 5 Start-up configuration).

Depending on the programmed configuration, they can be used in combination with VBUS_EN_SNK pin to enable different power path scenarios.

POWER_OK2 pin is a high voltage open drain output that allows a PMOS transistor to be directly driven to enable a power path.

POWER_OK3 is a low voltage open drain output.

Table 4. POWER_OK pin configuration

Configuration ID /NVM parameter PWR_OK_CFG[1:0]	Pin name	Value	Description
Configuration 1: all PDOs on single VBUS power path			
00b	VBUS_EN_SNK (1)	Hi-Z	No source attached
		0	Source attached
	POWER_OK2	Hi-Z	No functionality
	POWER_OK3	Hi-Z	No functionality
Configuration 2: all PDOs on single VBUS power path + dedicated high power charging paths			
10b (default)	VBUS_EN_SNK (1)	Hi-Z	No source attached
		0	Source attached
	POWER_OK2	Hi-Z	No PD explicit contract
		0	PD explicit contract with PDO2
	POWER_OK3	Hi-Z	No PD explicit contract
		0	PD explicit contract with PDO3
Configuration 3: all PDOs on single VBUS power path + detection of USB Type-C current capability from source			
11b	VBUS_EN_SNK (1)	Hi-Z	No source attached
		0	Source attached
	POWER_OK2	Hi-Z	No source attached or source supplies default USB Type-C current at 5 V when source attached
		0	Source supplies 3.0 A USB Type-C current at 5 V when source attached
	POWER_OK3	Hi-Z	No source attached or source supplies default USB Type-C current at 5V when source attached
		0	Source supplies 1.5 A USB Type-C current at 5 V when source attached
01b			Not applicable

1. The VBUS_EN_SNK pin values correspond to the default behavior

In case of configuration 2 (default):

- When a PDO negotiation succeeds, the POWER_OK pin related to the negotiated PDO is enabled (active low) when PS_READY message is received from the source

- When a new PDO is negotiated upon source request, the active POWER_OK pin is disabled (Hi-Z) when the STUSB4500 sends an RDO (request data object) message to the source with the new negotiated PDO
- At detachment the POWER_OK pins remain enabled (if already asserted), whereas VBUS_EN_SNK is disabled (Hi-Z) to deactivate the V_{BUS} power path from the USB Type-C receptacle. The POWER_OK pins state is reinitialized (Hi-Z) after new attachment or after a reset

2.3.9 GPIO

This pin is an active low open drain output that can be configured by NVM as per table below (see Section 5 Start-up configuration).

Table 5. GPIO pin configuration

NVM parameter GPIO_CFG[1:0]	Pin name	Pin function	Value	Description
00b	SW_CTRL_GPIO	Software controlled GPIO.	Hi-Z	When bit #0 value is 0b (at start-up)
		The output state is defined by the value of I^2C register bit #0 at address 2Dh	0	When bit #0 value is 1b
01b (default)	ERROR_RECOVERY	Hardware fault detection	Hi-Z	No hardware fault detected
		(see Section 3.7 Hardware fault management)	0	Hardware fault detected
10b	DEBUG	Debug accessory detection	Hi-Z	No debug accessory detected
		(see Section 3.8 Debug accessory mode detection)	0	Debug accessory detected
11b	SINK_POWER	Indicates USB Type-C current capability advertised by the source	Hi-Z	Source supplies default or 1.5 A USB Type-C current at 5 V
			0	Source supplies 3.0 A USB Type-C current at 5 V

2.3.10 VBUS_EN_SNK

This pin allows the incoming V_{BUS} power from the USB Type-C receptacle to be enabled when a source is connected according to different operating conditions stated in the table below. The default behavior of the pin can be changed by NVM programming (see Section 5 Start-up configuration).

Table 6. VBUS_EN_SNK pin configuration

NVM parameter POWER_ONLY _ABOVE_5V	Pin function	Value	Description	Comment
0b (default)	Enables V_{BUS} power path when source attached whatever V_{BUS} voltage (5 V or any PDO voltage)	Hi-Z	No source attached	Valid for all POWER_OK pin configurations 1, 2 and 3
		0	Source attached	
1b	Enables V_{BUS} power path only when source attached and V_{BUS} voltage negotiated to PDO2 or PDO3 voltage	Hi-Z	No source attached or no PD explicit contract with PDO2 or PDO3	
		0	Source attached and PD explicit contract with PDO2 or PDO3	

When POWER_ONLY_ABOVE_5V bit is set to logic level high, the VBUS_EN_SNK pin is asserted only when a PDO2 or PDO3 explicit contract is established with the source (see Section 3.3 Auto-run mode).

This feature is suited for sink devices requiring high power charging profile above 5 V to be fully operational (see Section 6.1.2 Powering a system under high charging profile only).

VBUS_EN_SNK pin is a high voltage open drain output that allows a PMOS transistor to be directly driven to enable the V_{BUS} power path.

2.3.11 A_B_SIDE

This output pin provides the cable orientation. It is used to establish USB SuperSpeed signal routing. This signal is not required in case of USB 2.0 support.

Table 7. USB data MUX select

Value	Description
HiZ	CC1 pin is attached to CC line
0	CC2 pin is attached to CC line

2.3.12 VBUS_VS_DISCH

This input pin is used to sense V_{BUS} presence, monitor V_{BUS} voltage, and discharge V_{BUS} from the USB Type-C receptacle side.

A serial resistor connected to the pin must be used to limit the discharge current through the pin. Maximum discharge current is 50 mA.

The discharge is activated automatically during cable disconnection, transition to a lower PDO voltage, hard reset and error recovery state. The discharge time is programmable by NVM (see Section 5 Start-up configuration).

2.3.13 VREG_1V2

This pin is used only for external decoupling of the 1.2 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min., 10 µF max.)

2.3.14 VSYS

This is the low power supply from the system, if there is any. It can be connected directly to a single cell Lithium battery or to the system power supply delivering 3.3 V or 5 V. It is recommended to connect the pin to ground when it is not used.

2.3.15 VREG_2V7

This pin is used only for external decoupling of the 2.7 V internal regulator. The recommended decoupling capacitor is: 1 µF typ. (0.5 µF min., 10 µF max.)

2.3.16 VDD

This is the power supply from the USB power line for applications powered by V_{BUS}.

3 Description of features

3.1 CC interface

The STUSB4500 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks: the CC line interface block and the CC control logic block.

The CC line interface block is used to:

- Set pull-down termination mode on the CC pins
- Monitor the CC pin voltage values related to the attachment detection thresholds
- Protect the CC pins against overvoltage

The CC control logic block is used to:

- Execute the Type-C FSM related to the sink power role with debug accessory support
- Determine the electrical state for each CC pin related to the detected thresholds
- Evaluate the conditions relative to the CC pin states and the V_{BUS} voltage value to transition from one state to another in the Type-C FSM
- Advertise a valid source-to-sink connection
- Determine the attached device mode: source or debug accessory
- Determine cable orientation to allow external routing of the USB data
- Manage USB Type-C power capability on V_{BUS}: USB default, medium or high current mode
- Handle hardware faults

3.2 Power delivery blocks

3.2.1 Physical layer

The physical layer defines the signaling technology for USB power delivery. It is the physical link between CC pins and protocol layer. In Tx mode, it receives packet data from the protocol layer, calculates and appends a CRC, encodes the payload (i.e. packet data and CRC) and transmits the packet (i.e. preamble, SOP, payload, CRC and EOP) using biphase mark coding (i.e. BMC) over CC pins. In Rx mode, it recovers the clock and the data, detects the SOP, decodes the received data including the CRC, detects the EOP and validates the CRC.

3.2.2 Protocol layer

The protocol layer has the responsibility to manage the messages from/to the physical layer. It automatically manages the protocol receive timeouts, the message counter, the retry counter and the GoodCRC messages.

It communicates with the internal policy engine.

3.2.3 Policy engine

The policy engine implements the power negotiation with the connected device according to its sink role. It implements all state machines controlling the protocol layer that forms and schedules the messages.

The policy engine uses the protocol layer to send/receive messages.

The policy engine interprets the device policy manager’s input in order to implement policy for port and directs the protocol layer to send appropriate messages.

3.2.4 Device policy manager

The device policy manager deals with the power capability request and change management. It operates according to the decision algorithm described in the following section.

3.3 Auto-run mode

The STUSB4500 implements a hardcoded decision algorithm that allows the device to negotiate in autonomous way a power delivery transaction with a source according to the PDO (power data objects) profiles programmed in the NVM.

It makes the STUSB4500 a plug-and-play, autonomous and effective solution to develop USB PD sink systems operating in standalone.

3.3.1 Sink PDOs configuration

The STUSB4500 features up to 3 sink PDOs (SNK_PDO). The value of each PDO is defined in the NVM (see Section 5 Start-up configuration).

Table 8. Sink PDO description

Sink PDO #	Comment	Priority	Description
PDO1	Mandatory	Low	Defines the default power configuration
PDO2	Optional	Medium	Defines the intermediate power configuration
PDO3	Optional	High	Defines the highest power configuration (if any)

PDO voltage configuration:

- PDO1 voltage is fixed to 5 V by hardware
- PDO2 and PDO3 voltages are programmable by NVM from 5 V to 20 V by steps of 50 mV as defined in the USB PD standard specification (see Section 5 Start-up configuration)

PDO current configuration:

- The current of each PDO is programmable by NVM through look-up table see (Section 5 Start-up configuration)
- 15 predefined values are set in the look-up table from 0.5 A to 5 A
- 1 custom value can be programmed in the look-up table from 10 mA to 5 A by steps of 10 mA as defined in the USB PD standard specification. This value is common to all PDOs if used

3.3.2 Decision algorithm description

The decision algorithm compares each SNK_PDOi with the SRC_PDOj capabilities received from the source.

The comparison starts from the SNK_PDO with the highest priority to the SNK_PDO with the lowest priority. The voltage is compared first, the current afterwards.

A match occurs when both conditions are met:

1. V(SNK_PDOi) = V(SRC_PDOj)
2. I(SNK_PDOi) ≤ I(SRC_PDOj)

The comparison loop stops at the first match. The remaining SRC_PDOj are not compared and the SNK_PDOi with lower priority are discarded.

In case of match:

- An RDO (request data object) message is formed with matched voltage V(SNK_PDOi) as operating voltage, related I(SNK_PDOi) current as operating current and I(SRC_PDOj) current from matched SRC_PDOj as maximum current
- The RDO message is sent to the source for evaluation and acceptance by the source prior the transition to matched PDO voltage by the source and the reception of PS_READY message by the sink

In case of no match:

- At the end of the comparison loop, if no match happens, the USB PD negotiation ends with an explicit USB PD contract at 5 V
- An RDO message is sent to the source with capability mismatch enabled, operating current set to current value from source PDO at 5 V, and maximum current set to I(SNK_PDO1)

3.3.3 Requesting maximum source current

Thanks to dedicated NVM bit “REQ_SRC_CURRENT”, the operating current informed in the RDO message, when a matching PDO is found, can be set either to the current value from the matched sink PDO (default) or to the current value from the matched source PDO.

Requesting current value from the matched source PDO is useful for a sink that can benefit from higher power capability than originally required in order to increase its performance. This implies for the source to allocate a power reserve as stated in the USB PD standard specification.

In case the sink is not able to consume more power than requested, this option must not be used. It avoids allocating by the source a power reserve that is not used, thus limiting the overall power system optimization.

3.3.4 Decision algorithm application with examples

The following capabilities from the source have been considered to study the negotiation result for different sink PDO configuration cases with the STUSB4500:

- SRC_PDO1 = 5 V, 3 A
- SRC_PDO2 = 9 V, 3 A
- SRC_PDO3 = 15 V, 2 A

Table 9. Decision algorithm results for different cases

Case	Configured sink capabilities	Result REQ_SRC_CURRENT = 0b	Result REQ_SRC_CURRENT = 1b
1	SNK_PDO2 = 9 V, 2.5 A	Match: RDO = 9 V, 2.5 A, 3 A	Match: RDO = 9 V, 3 A, 3 A
	SNK_PDO1 = 5 V, 3 A	Not compared	Not compared
2	SNK_PDO3 = 9.1 V, 2.9 A	No match	No match
	SNK_PDO2 = 8.9 V, 2.9 A	No match	No match
	SNK_PDO1 = 5 V, 3 A	Match: RDO = 5 V, 3 A, 3 A	Match: RDO = 5 V, 3 A, 3 A
3	SNK_PDO3 = 15 V, 2.1 A	No match	No match
	SNK_PDO2 = 9 V, 2.5 A	Match: RDO = 9 V, 2.5 A, 3 A	Match: RDO = 9 V, 3 A, 3 A
	SNK_PDO1 = 5 V, 3 A	Not compared	Not compared
4	SNK_PDO3 = 15.1 V, 2 A	No match	No match
	SNK_PDO2 = 15 V, 1 A	Match: RDO = 15 V, 1 A, 2 A	Match: RDO = 15 V, 2 A, 2 A
	SNK_PDO1 = 5 V, 3 A	Not compared	Not compared
5	SNK_PDO2 = 15 V, 3 A	No match	No match
	SNK_PDO3 = 9 V, 1 A	Match: RDO = 9 V, 1 A, 3 A	Match: RDO = 9 V, 3 A, 3 A
	SNK_PDO1 = 5 V, 1 A	Not compared	Not compared

3.4 VBUS power path control

3.4.1 VBUS monitoring

The V_{BUS} monitoring block supervises from the VBUS_VS_DISCH input pin the V_{BUS} voltage on the USB Type-C receptacle side.

It is used to check that V_{BUS} is within a valid voltage range to establish a valid source-to-sink connection and to enable safely the V_{BUS} power path through the VBUS_EN_SNK pin.

It allows detection of unexpected V_{BUS} voltage conditions such as undervoltage or overvoltage relative to the valid V_{BUS} voltage range. When such conditions occur, the STUSB4500 reacts as follows:

- At attachment, it prevents the source-to-sink connection to be established and the V_{BUS} power path to be asserted
- After attachment, it goes into unattached state and it disables the V_{BUS} power path

The valid V_{BUS} voltage range is defined by a high limit $V_{MONUSBH}$ and a low limit that can take as value either V_{THUSB} or $V_{MONUSBL}$ depending on system operation and V_{BUS} voltage.

V_{THUSB} low limit is fixed by hardware at 3.3 V. It corresponds to the undervoltage condition to detect a V_{BUS} disconnection when V_{BUS} voltage is at 5 V (USB Type-C or PDO1). The nominal value of $V_{MONUSBL}$ is V_{BUS}-5%. The low limit value can be shifted by fraction of V_{BUS} from -1% to -15%. The nominal value of $V_{MONUSBH}$ is V_{BUS} +5%. The high limit value can be shifted independently by fraction of V_{BUS} from +1% to +15%. It means the threshold limits can vary from V_{BUS}-5% to V_{BUS}-20% for the low limit and from V_{BUS}+5% to V_{BUS}+20% for the high limit.

At attachment, the valid V_{BUS} voltage range is defined by $V_{MONUSBH}$ and $V_{MONUSBL}$ limits to establish a valid source-to-sink connection. After attachment and during system operations, the valid V_{BUS} voltage range is automatically adjusted to $V_{MONUSBH}$ and V_{THUSB} limits when V_{BUS} voltage is at 5 V (USB Type-C or PDO1), or to $V_{MONUSBH}$ and $V_{MONUSBL}$ limits when V_{BUS} operates under PDO2 or PDO3 voltage.

The V_{BUS} voltage value is automatically adjusted to 5 V (USB Type-C) at attachment and to the negotiated PDO voltage after PDO transition. During each PDO transition, the V_{BUS} monitoring is disabled for tSrcReady (285 ms max.) as per USB PD standard specifications. Then the new limits applicable to the negotiated PDO voltage are monitored.

The threshold limits are preset by default in the NVM with different shift coefficients (see Section 7.3 Electrical and timing characteristics). The threshold limits can be changed independently through NVM programming (see Section 5 Start-up configuration).

3.4.2 VBUS discharge

The monitoring block also handles the V_{BUS} discharge paths connected to the VBUS_VS_DISCH pin for the USB Type-C receptacle side and to the DISCH pin for the power system side. The discharge paths are activated at the same time when disconnection is detected, during transition to a lower PDO voltage, when a hard reset is performed or when the device goes into the error recovery state (see Section 3.7 Hardware fault management). At detachment, during error recovery state or hard reset, the discharge is activated for $T_{DISUSB0V}$ time. During transition to a lower PDO voltage, the discharge is activated for $T_{DISUSBPDO}$ time.

The discharge time durations are also preset by default in the NVM (see Section 7.3 Electrical and timing characteristics). The discharge time durations can be changed through NVM programming (see Section 5 Start-up configuration).

The V_{BUS} discharge feature is enabled by default in the NVM and can be disabled through NVM programming (see Section 5 Start-up configuration).

3.4.3 VBUS power path assertion

The STUSB4500 can control the assertion of the V_{BUS} power path from the USB Type-C receptacle, directly or indirectly, through the VBUS_EN_SNK pin.

The table below summarizes the operating conditions that determine the electrical value of the VBUS_EN_SNK pin during system operation.

Table 10. VBUS_EN_SNK pin behavior depending on the operating conditions

<table>
<tr><th rowspan="2">Value</th><th colspan="5">Operating conditions</th></tr>
<tr><th>NVM parameter POWER_ONLY _ABOVE_5V</th><th>Connection stage</th><th>V_{BUS} voltage from source</th><th>V_{BUS} monitoring conditions on VBUS_VS_DISCH pin</th><th>Type-C state</th></tr>
<tr><td rowspan="3">0</td><td rowspan="2">0b</td><td>At attachment</td><td>5 V
(USB Type-C)</td><td>$V_{BUS} < V_{MONUSBH1}$
and
$V_{BUS} > V_{MONUSBL1}$</td><td rowspan="3">Attached.SNK
or
Debug Accessory.SNK</td></tr>
<tr><td>During operation</td><td>5 V
(USB Type-C
or SNK_PDO1)</td><td>$V_{BUS} < V_{MONUSBH1}$
and
$V_{BUS} > V_{THUSB}$</td></tr>
<tr><td>0b or 1b</td><td>During operation</td><td>V(SNK_PDO2)
or V(SNK_PDO3)</td><td>$V_{BUS} < V_{MONUSBH2/3}$
and
$V_{BUS} > V_{MONUSBL2/3}$</td></tr>
<tr><td rowspan="5">Hi-Z</td><td>0b or 1b</td><td>Before attachment</td><td>N.A.</td><td>N.A.</td><td>Unattached.SNK</td></tr>
<tr><td>1b</td><td rowspan="2">At attachment</td><td rowspan="2">5 V
(USB Type-C)</td><td>$V_{BUS} < V_{MONUSBH1}$
and
$V_{BUS} > V_{MONUSBL1}$</td><td>Attached.SNK
or
Debug Accessory.SNK</td></tr>
<tr><td>0b</td><td>$V_{BUS} > V_{MONUSBH1}$
and
$V_{BUS} < V_{MONUSBL1}$</td><td>AttachWait.SNK</td></tr>
<tr><td>0b</td><td rowspan="2">During operation</td><td>5 V
(USB Type-C
or SNK_PDO1)</td><td>$V_{BUS} > V_{MONUSBH1}$
or
$V_{BUS} < V_{THUSB}$</td><td rowspan="2">Attached.SNK
or
Debug Accessory.SNK</td></tr>
<tr><td>0b or 1b</td><td>V(SNK_PDO2)
or V(SNK_PDO3)</td><td>$V_{BUS} > V_{MONUSBH2/3}$
or
$V_{BUS} < V_{MONUSBL2/3}$</td></tr>
</table>

Type-C state column refers to the Type-C FSM states as defined in the USB Type-C standard specification.

3.5 Dead battery mode

Dead battery mode allows systems powered by a battery to be supplied by the V_{BUS} when the battery is discharged and to start the battery charging process. This mode is also used in systems that are powered through the V_{BUS} only.

Dead battery mode operates only if the CC1DB and CC2DB pins are connected respectively to the CC1 and CC2 pins. Thanks to these connections, the STUSB4500 presents a pull-down termination on its CC pins and advertises itself as a sink even if the device is not supplied.

When a source system connects to a USB Type-C port with the STUSB4500 configured in dead battery mode, it can detect the pull-down termination, establish the source-to-sink connection, and provide the $V_{BUS.}$ The STUSB4500 is then supplied thanks to the VDD pin connected to V_{BUS} on the USB Type-C receptacle side. The STUSB4500 can finalize the connection on its side and enable the power path on V_{BUS} thanks to the VBUS_EN_SNK pin to allow the system to be powered.

3.6 High voltage protections

The STUSB4500 can be safely used in systems or connected to systems that handle high voltage on the V_{BUS} power path. The device integrates an internal circuitry on the CC pins that tolerates high voltage and ensures protection up to 22 V in case of unexpected short-circuits with the V_{BUS} or in case of a connection to a device supplying high voltage on the V_{BUS}.

3.7 Hardware fault management

The STUSB4500 handles during system operation some pre-identified hardware fault conditions. When such conditions happen, the circuit goes into a transient error recovery state named ErrorRecovery in the Type-C FSM as defined in the USB Type-C standard specifications.

The error recovery state is equivalent to force a detach event. When entering in this state, the device de-asserts the V_{BUS} power path by disabling the VBUS_EN_SNK, POWER_OK2 and POWER_OK3 pins, and it removes the terminations from the CC pins during several tens of milliseconds. Then, it transitions to the unattached state.

The STUSB4500 goes into error recovery state when at least one condition listed below is met:

- If an overtemperature is detected (junction temperature above maximum T_J)
- If an overvoltage is detected on the CC pins (voltage on CC pins above V_{OVP})
- If after a hard reset the power delivery communication with the source is broken

The detection of a hardware fault is advertised through the GPIO pin when configured in ERROR_RECOVERY mode.

See Section 7 Electrical characteristics for threshold values.

3.8 Debug accessory mode detection

The STUSB4500 detects a connection to a debug and test system (DTS) as defined in the USB Type-C standard specification. The debug accessory detection is advertised through the GPIO pin when configured in DEBUG mode.

A debug accessory device is detected when both the CC1 and CC2 pins are pulled up by an R_p resistor from the connected device. The voltage levels on the CC1 and CC2 pins give the orientation and current capability as described in the table below. The GPIO pin configured in DEBUG mode is asserted to advertise the DTS detection and the A_B_SIDE pin indicates the orientation of the connection.

Table 11. Orientation and current capability detection in sink power role

#	CC1 pin (CC2 pin)	CC2 pin (CC1 pin)	Charging current configuration	A_B_SIDE pin CC1/CC2 (CC2/CC1)
1	R_p 3 A	R_p 1.5 A	Default	Hi-Z (0)
2	R_p 1.5 A	R_p default	1.5 A	Hi-Z (0)
3	R_p 3 A	R_p default	3.0 A	Hi-Z (0)
4	R_p def/1.5 A/3 A	R_p def/1.5 A/3 A	Default	Hi-Z (Hi-Z)

4 I2C interface

4.1 Read and write operations

The I²C interface is used to configure, control and read the operation status of the device. It is compatible with the Philips I²C Bus® (version 2.1). The I²C is a slave serial interface based on two signals:

- SCL - serial clock line: input clock used to shift data
- SDA - serial data line: input/output bidirectional data transfers

A filter rejects the potential spikes on the bus data line to preserve data integrity.

The bidirectional data line supports transfers up to 400 Kbit/s (fast mode). The data are shifted to and from the chip on the SDA line, MSB first.

The first bit must be high (START) followed by the 7-bit device address and the read/write control bit.

Four 7-bit device address are available for the STUSB4500 thanks to the external programming of DevADDR0 and DevADDR1 bits through ADDR0 and ADDR1 pins setting i.e. 0x28 or 0x29 or 0x2A or 0x2B. It allows four STUSB4500 devices to be connected on the same I^2C bus.

Table 12. Device address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DevADDR6	DevADDR5	DevADDR4	DevADDR3	DevADDR2	DevADDR1	DevADDR0	R/W
0	1	0	1	0	ADDR1	ADDR0	0/1

Table 13. Register address format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RegADDR7	RegADDR6	RegADDR5	RegADDR4	RegADDR3	RegADDR2	RegADDR1	RegADDR0

Table 14. Register data format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 3. Read operation

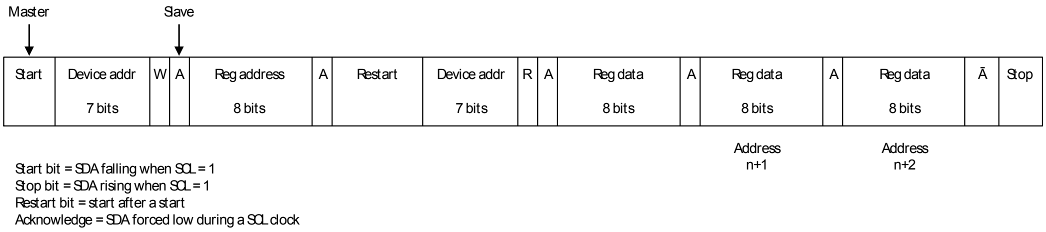
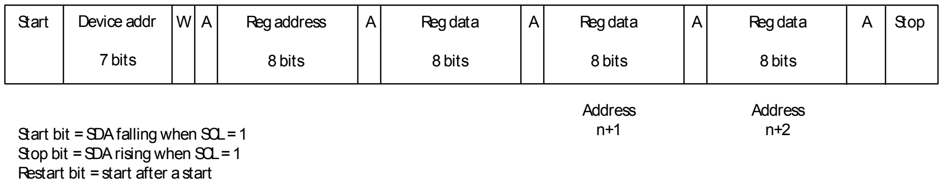


Figure 4. Write operation



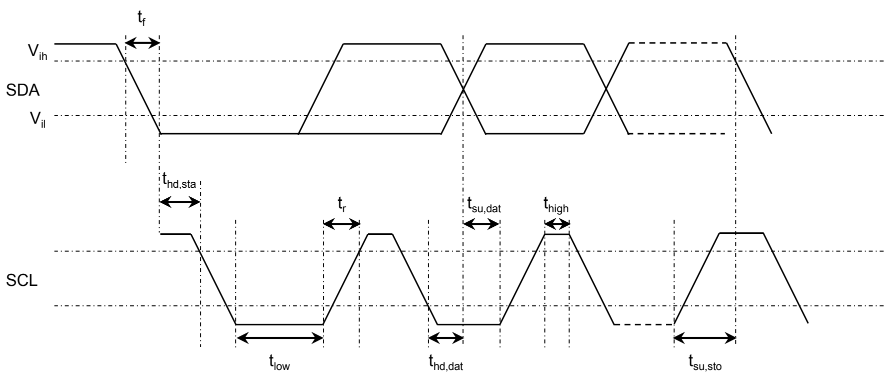
4.2 Timing specifications

The device uses a standard slave I²C channel at speed up to 400 kHz.

Table 15. I²C timing parameters - VDD = 5 V

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{scl}	SCL clock frequency	0	-	400	kHz
$t_{hd,sta}$	Hold time (repeated) START condition	0.6	-	-	µs
t_{low}	LOW period of the SCL clock	1.3	-	-	µs
t_{high}	HIGH period of the SCL clock	0.6	-	-	µs
$t_{su,dat}$	Setup time for repeated START condition	0.6	-	-	µs
$t_{hd,dat}$	Data hold time	0.04	-	0.9	µs
$t_{su,dat}$	Data setup time	100	-	-	µs
t_r	Rise time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
t_f	Fall time of both SDA and SCL signals	20 + 0.1 C_b	-	300	ns
$t_{su,sto}$	Set-up time for STOP condition	0.6	-	-	µs
t_{buf}	Bus free time between a STOP and START condition	1.3	-	-	µs
C_b	Capacitive load for each bus line	-	-	400	pF

Figure 5. I²C timing diagram



5 Start-up configuration

5.1 User-defined parameters

The STUSB4500 has a set of user-defined parameters that can be customized by NVM re-programming through the I^2C interface. This feature allows the customer to change the preset configuration of the USB Type-C and PD interface and to define a new configuration to meet specific application requirements addressing various use cases, or specific implementations.

The NVM re-programming overrides the initial default setting to define a new default setting that is used at power-up or after a reset. The default setting is copied at power-up, or after a reset, from the embedded NVM into I^2C registers. The values copied in the I^2C registers are used by the STUSB4500 during the system operation.

The NVM re-programming is possible with a customer password. The I^2C registers must be re-initialized after each NVM re-programming to make effective the new parameters setting either through power-off and power-up sequence, or through reset.

5.2 Default start-up configuration

The table below lists the user-defined parameters and indicates the default start-up configuration of the STUSB4500.

Table 16. STUSB4500 user-defined parameters and default settings

Parameter name	Parameter description	Reset value (default)	Value	Description
SNK_PDO_NUMB[1:0]	Number of sink PDOs	11b (3)	00b	1 PDO
			01b	1 PDO
			10b	2 PDOs
			11b	3 PDOs
V_SNK_PDO2	Voltage value for SNK_PDO2	0.05*300 (15 V)	0.05*100 to 0.05*400	Flexible voltage value 5 V ≤ 0.05*V_SNK_PDO2_FLEX[9:0] ≤ 20 V by steps of 50 mV Default V_SNK_PDO2_FLEX[9:0] = 0100101100
V_SNK_PDO3	Voltage value for SNK_PDO3	0.05*400 (20 V)	0.05*100 to 0.05*400	Flexible voltage value 5 V ≤ 0.05*V_SNK_PDO3_FLEX[9:0] ≤ 20 V by steps of 50 mV Default V_SNK_PDO3_FLEX[9:0] = 0110010000
I_SNK_PDO1	Current value for SNK_PDO1	0101b (1.5 A)	0000b	I_SNK_PDO_LUT[3:0] flexible current value from look-up table (see Table 17. Look-up table for sink PDO current configuration)
			0001b to 1111b	I_SNK_PDO_LUT[3:0] pre-defined current values from look-up table (see Table 17. Look-up table for sink PDO current configuration)

Parameter name	Parameter description	Reset value (default)	Value	Description
I_SNK_PDO2	Current value for SNK_PDO2	0101b (1.5 A)	0000b	I_SNK_PDO_LUT[3:0] flexible current value from look-up table (see Table 17. Look-up table for sink PDO current configuration)
			0001b to 1111b	I_SNK_PDO_LUT[3:0] pre-defined current values from look-up table (see Table 17. Look-up table for sink PDO current configuration)
I_SNK_PDO3	Current value for SNK_PDO3	0011b (1.0 A)	0000b	I_SNK_PDO_LUT[3:0] flexible current value from look-up table (see Table 17. Look-up table for sink PDO current configuration)
			0001b to 1111b	I_SNK_PDO_LUT[3:0] pre-defined current values from look-up table (see Table 17. Look-up table for sink PDO current configuration)
I_SNK_PDO_FLEX	Flexible current value common to all PDOs	0.01*200 (2.0 A)	0.01*1 to 0.01*500	Flexible current value 10 mA ≤ 0.01*I_SNK_PDO_FLEX[9:0] ≤ 5A by steps of 10 mA Default I_SNK_PDO_FLEX[9:0] = 0011001000 (see Table 17. Look-up table for sink PDO current configuration)
SHIFT_VBUS_HL1	Coefficient to shift up nominal V_{BUS} high voltage limit applicable to 5 V and SNK_PDO1 voltage	1010b (10%)	0001b to 1111b	1% ≤ $V_{SHUSBH1}$ ≤ 15% of VBUS by increment of 1% Default $_{VSHUSBH1}$ = 10%
SHIFT_VBUS_LL1	Coefficient to shift down nominal V_{BUS} low voltage limit applicable to 5 V and SNK_PDO1 voltage	1111b (15%)	0001b to 1111b	1% ≤ $V_{SHUSBL1}$ ≤ 15% of V_{BUS} by increment of 1% Default $V_{SHUSBL1}$ = 15%
SHIFT_VBUS_HL2	Coefficient to shift up nominal V_{BUS} high voltage limit applicable to SNK_PDO2 voltage	0101b (5%)	0001b to 1111b	1% ≤ $V_{SHUSBH2}$ ≤ 15% of V_{BUS} by increment of 1% Default $V_{SHUSBH2}$ = 5%
SHIFT_VBUS_LL2	Coefficient to shift down nominal V_{BUS} applicable to SNK_PDO2 voltage	1111b (15%)	0001b to 1111b	1% ≤ $V_{SHUSBL2}$ ≤ 15% of V_{BUS} by increment of 1% Default $V_{SHUSBL2}$ = 15%
SHIFT_VBUS_HL3	Coefficient to shift up nominal V_{BUS} high voltage limit applicable to SNK_PDO3 voltage	0101b (5%)	0001b to 1111b	1% ≤ $V_{SHUSBH3}$ ≤ 15% of VBUS by increment of 1% Default $V_{SHUSBH3}$ = 5%
SHIFT_VBUS_LL3	Coefficient to shift down nominal V_{BUS} low voltage limit applicable to SNK_PDO3 voltage	1111b (15%)	0001b to 1111b	1% ≤ $V_{SHUSBL3}$ ≤ 15% of V_{BUS} by increment of 1% Default $V_{SHUSBL3}$ = 15%
VBUS_DISCH_TIME_TO_0V	Coefficient used to compute V_{BUS} discharge time to 0V	1001b (9)	0001b to 1111b	1 ≤ $T_{DISPAR0V}$ ≤ 15 by increment of 1 Unit discharge time: 84 ms (typ.) Default coefficient $T_{DISPAR0V}$ = 9, discharge time $T_{DISUSB0V}$ = 756 ms

Parameter name	Parameter description	Reset value (default)	Value	Description
VBUS_DISCH_TIME_TO_PDO	Coefficient used to compute V_{BUS} discharge time when transitioning to lower PDO voltage	1100b (12)	0001b to 1111b	1 ≤ $T_{DISPARPDO}$ ≤ 15 by increment of 1 Unit discharge time: 24 ms (typ.) Default coefficient $T_{DISPARPDO}$ = 12, discharge time $T_{DISUSBPDO}$ = 288 ms
VBUS_DISCH_DISABLE	V_{BUS} discharge deactivation on VBUS_VS_DISCH and DISCH pins	0b	0b	V_{BUS} discharge enabled
			1b	V_{BUS} discharge disabled
USB_COMM_CAPABLE	USB 2.0 or 3.x data communication capability by sink system	0b	0b	Sink does not support data communication
			1b	Sink supports data communication
SNK_UNCONS_POWER	Unconstrained Power bit setting in capabilities message sent by the sink	0b	0b	No external source of power
			1b	An external source of power is available and is sufficient to adequately power the system while charging external devices
REQ_SRC_CURRENT	In case of match, selects which operating current from the sink or the source is to be requested in the RDO message	0b	0b	Request I(SNK_PDO) as operating current in RDO message
			1b	Request I(SRC_PDO) as operating current in RDO message
POWER_OK_CFG[1:0]	Selects POWER_OK pins configuration (see Section 2.3.8 POWER_OK2 / POWER_OK3)	10b	00b	Configuration 1
			01b	Not applicable
			10b	Configuration 2 (default)
			11b	Configuration 3
POWER_ONLY_ABOVE_5V	Selects VBUS_EN_SNK pin configuration (see Section 2.3.10 VBUS_EN_SNK)	0b	0b	VBUS_EN_SNK pin enabled when source attached whatever VBUS voltage (5 V or any PDO voltage)
			1b	VBUS_EN_SNK pin enabled only when source attached and VBUS voltage negotiated to PDO2 or PDO3 voltage
GPIO_CFG[1:0]	Selects GPIO pin configuration (see Section 2.3.9 GPIO)	01b	00b	SW_CTRL_GPIO
			01b	ERROR_RECOVERY
			10b	DEBUG
			11b	SINK_POWER

Table 17. Look-up table for sink PDO current configuration

Parameter name	Parameter value	PDO current value	Description
I_SNK_PDO_LUT[3:0]	0000b	0.01 ≤ 0.01*I_SNK_PDO_FLEX[9:0] ≤ 5 by steps of 10 mA Default I_SNK_PDO_FLEX[9:0] = 0011001000 (0.01*200=2 A)	Flexible current value
	0001b	0.50 A	Pre-defined current values
	0010b	0.75 A	
	0011b	1.00 A	
	0100b	1.25 A	
	0101b	1.50 A	
	0110b	1.75 A	
	0111b	2.00 A	
	1000b	2.25 A	
	1001b	2.50 A	
	1010b	2.75 A	
	1011b	3.00 A	
	1100b	3.50 A	
	1101b	4.00 A	
	1110b	4.50 A	
	1111b	5.00 A	

Table 18. STUSB4500 default sink PDO programming

Sink PDO #	Type	Priority	PDO value	V_{BUS} monitoring Low voltage limit $V_{MONUSBL}$	V_{BUS} monitoring High voltage limit $V_{MONUSBH}$
PDO1	Fixed voltage	Low	5 V / 1.5 A	3.3 V (detachment) -20 % (attachment)	+15 %
PDO2	Flexible voltage	Medium	15 V / 1.5 A	-20 %	+10 %
PDO3	Flexible voltage	High	20 V / 1.0 A	-20 %	+10 %

See Section 7.3 Electrical and timing characteristics for parameters related to V_{BUS}.

6 Application

The sections below are not part of the ST product specification. They are intended to give a generic application overview to be used by the customer as a starting point for further implementations and customizations. ST does not warrant compliance with customer specifications. Full system implementation and validation are under the customer's responsibility.

6.1 General information

6.1.1 Power supplies

The STUSB4500 can be supplied in three different ways depending on the targeted application:

- Through the VDD pin only for applications powered by V_{BUS} that operate with dead battery mode support
- Through the VSYS pin only for AC powered applications with a system power supply delivering 3.3 V or 5 V
- Through the VDD and VSYS pins either for applications powered by a battery with dead battery mode support or for applications powered by V_{BUS} with a system power supply delivering 3.3 V or 5 V. When both VDD and VSYS power supplies are present, the low power supply VSYS is selected when VSYS voltage is above 3.1 V. Otherwise VDD is selected

6.1.2 Powering a system under high charging profile only

The STUSB4500 allows the V_{BUS} power path to be enabled through VBUS_EN_SNK pin only when a high power charging profile above 5 V has been negotiated (PDO2 or PDO3) with the source (see Section 3.3 Auto-run mode).

This feature can be turned on thanks to NVM bit POWER_ONLY_ABOVE_5V (see Section 5 Start-up configuration). When the bit value is set to logic level high, the VBUS_EN_SNK pin is asserted only when a PDO2 or PDO3 explicit contract is established with the source (see Section 2.3.10 VBUS_EN_SNK).

In case of mismatch, the V_{BUS} power path remains open while the source provides 5 V on the USB Type-C receptacle. The source and the sink stay electrically connected through the CC pins. Thus, when the source is able later to provide power capabilities corresponding to those expected by the sink, a new negotiation is again possible upon source request. If the PDO negotiation succeeds, the VBUS_EN_SNK pin is asserted which allows the system to be powered at the negotiated PDO profile.

This feature is suited for sink devices requiring high power charging profile above 5 V to be fully operational.

6.1.3 Connection to MCU or application processor

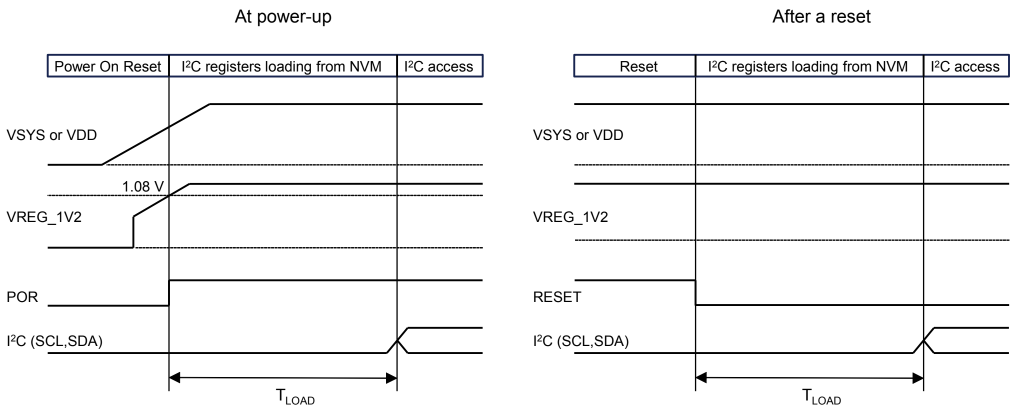
The STUSB4500 runs as a standalone USB PD sink controller. The connection to an MCU or an application processor is optional. However, an I²C interface with an interrupt allows simple connection to most of MCU and SOC of the market.

When a connection through the I²C interface is implemented, it provides extensive functionality during the system operation. For instance, it may be used to:

1. Define the port configuration during system boot (in case the NVM parameters are not customized during manufacturing)
2. Provide a diagnostic of the Type-C connection in real time

At power-up or after a reset, the first software access to the I^2C registers of the STUSB4500 can be done only after T_{LOAD} as shown in the figure below. T_{LOAD} corresponds to the time required to initialize the I^2C registers with the default values from the embedded NVM. At power-up, the loading phase starts when the voltage level on the VREG_1V2 output pin of the 1.2 V internal regulator reaches 1.08 V to release the internal POR signal. After a reset, the loading phase starts when the signal on the RESET pin is released.

Figure 6. I²C register initialization sequence at power-up or after a reset

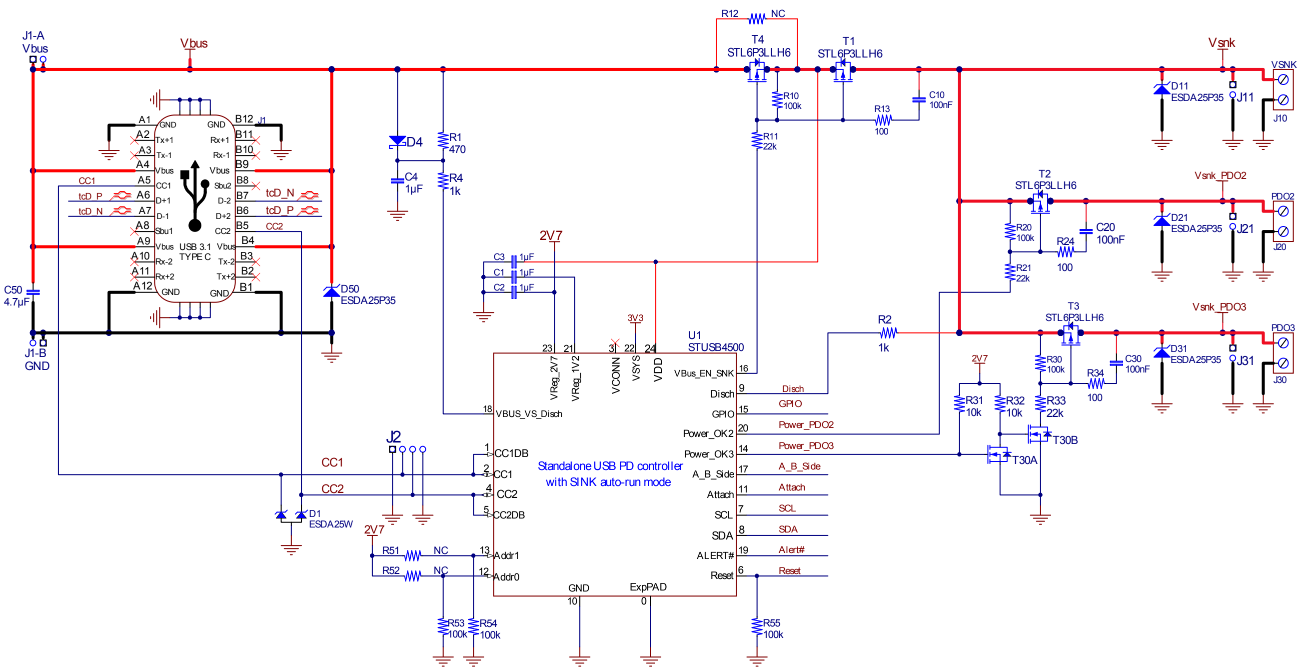


6.2 Typical applications

6.2.1 Sink USB PD application with dual high power charging paths

6.2.1.1 *Application schematic*

Figure 7. Implementation example with POWER_OK pins configuration #2 (default)



6.2.1.2 *VBUS power path activation*

Table 19. VBUS power path activation versus negotiated PDO contract

Negotiated PDO contract	Transistors T4/T1 (VBUS_EN_SNK)	Transistor T2 (POWER_OK2)	Transistor T3 (POWER_OK3)
Implicit 5 V USB Type-C or PDO1 contract	ON	OFF	OFF
PDO2 contract	ON	ON	OFF
PDO3 contract	ON	OFF	ON

7 Electrical characteristics

7.1 Absolute maximum ratings

All voltages are referenced to GND.

Table 20. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	28	V
V_{SYS}	Supply voltage on VSYS pin	6	V
V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB}	High voltage on CC pins	22	V
$V_{VBUS\_EN\_SNK}$ $V_{VBUS\_VS\_DISCH}$ V_{DISCH} V_{POWER_OK2}	High voltage on V_{BUS} pins	28	V
V_{SCL}, V_{SDA} V_{ALERT} V_{RESET} V_{ATTACH} $V_{A\_B\_SIDE}$ V_{POWER_OK3} V_{GPIO} V_{ADDR0}, V_{ADDR1}	Operating voltage on I/O pins	-0.3 to 6	V
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature	145	°C
ESD	HBM	3	kV
	CDM	1.5	kV

7.2 Operating conditions

Table 21. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage on VDD pin	4.1 to 22	V
V_{SYS}	Supply voltage on VSYS pin	3.0 to 5.5	V
V_{CC1}, V_{CC2} V_{CC1DB}, V_{CC2DB}	CC pins	0 to 5.5	V
$V_{VBUS\_EN\_SNK}$ $V_{VBUS\_VS\_DISCH}$ V_{DISCH} V_{POWER_OK2}	High voltage pins	0 to 22	V
V_{SCL}, V_{SDA} V_{ALERT} V_{RESET} V_{ATTACH} $V_{A\_B\_SIDE}$ V_{POWER_OK3} V_{GPIO} V_{ADDR0}, V_{ADDR1}	Operating voltage on I/O pins	0 to 4.5	V
T_A	Operating temperature	-40 to 105	°C

7.3 Electrical and timing characteristics

Unless otherwise specified: V_{DD} = 5 V, T_A = 25 °C, all voltages are referenced to GND.

Table 22. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DD\ (SNK)}$	Current consumption	Device idle as a SINK (not connected, no communication) V_{SYS} @ 3.3 V	115	140	165	µA
		V_{DD} @ 5.0 V	110	160	210	µA
T_{LOAD}	I^2C registers loading time from NVM	At power-up or after a reset			30	ms
CC1 and CC2 pins						
R_d	CC pull-down resistors	-40 °C < T_A < +105 °C	-10%	5.1	+10%	kΩ
R_{INCC}	CC input impedance	Terminations off	200			kΩ
$V_{TH0.2}$	Detection threshold 1	Min. $I_{P\text{-}USB}$ detection by sink on R_d, min CC voltage for connected sink	0.15	0.20	0.25	V
$V_{TH0.66}$	Detection threshold 2	Min. $I_{P\_1.5}$ detection by sink on R_d	0.61	0.66	0.71	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{TH1.23}$	Detection threshold 3	Min. $I_{P\_3.0}$ detection by sink on Rd	1.16	1.23	1.31	V
$V_{TH2.6}$	Detection threshold 4	Max. CC voltage for connected sink	2.45	2.60	2.75	V
V_{OVP}	Overvoltage protection on CC pins		5.82	6	6.18	V
VBUS_VS_DISCH pin monitoring and driving						
V_{THUSB}	V_{BUS} disconnection threshold (5 V USB Type-C or PDO1 selected)	V_{SYS} = 3.0 to 5.5 V	3.2	3.3	3.4	V
V_{TH0V}	V_{BUS} safe 0 V threshold (vSafe0V)	V_{SYS} = 3.0 to 5.5 V	0.5	0.6	0.7	V
I_{DISUSB}	V_{BUS} discharge current	Through external resistor connected to VBUS_VS_DISCH pin			50	mA
$T_{DISUSB0V}$	V_{BUS} discharge time to 0 V	At detachment, during error recovery state or hard reset, Coefficient $T_{DISPAR0V}$ programmable by NVM, Default $T_{DISPAR0V}$ = 9, $T_{DISUSB0V}$ = 756 ms	70 *$T_{DISPAR0V}$	84 *$T_{DISPAR0V}$	100 *$T_{DISPAR0V}$	ms
$T_{DISUSBPDO}$	V_{BUS} transition discharge time to new PDO	At transition to a lower PDO voltage, Coefficient $T_{DISPARPDO}$ programmable by NVM, Default $T_{DISPARPDO}$ = 12, $T_{DISUSBPDO}$ = 288 ms	20 *$T_{DISPARPDO}$	24 *$T_{DISPARPDO}$	28 *$T_{DISPARPDO}$	ms
$V_{MONUSBH}$	V_{BUS} monitoring high voltage limit	V_{BUS} can be 5 V_{USB} Type-C voltage or any PDO voltage, V_{BUS}+5% is nominal high voltage limit, Shift coefficient V_{SHUSBH} is programmable by NVM from 1% to 15% of V_{BUS} by step of 1%, Default $V_{SHUSBH1}$ = 10%, $V_{MONUSBH1}$ = V_{BUS} +15% (5 V USB Type-C or PDO1), $V_{SHUSBH2/3}$ = 5%, $V_{MONUSBH2/3}$ = V_{BUS}+10% (PDO2 or PDO3)		V_{BUS}+5% +V_{SHUSBH}		V
$V_{MONUSBL}$	VBUS monitoring low voltage limit	V_{BUS} can be 5 V_{USB} Type-C voltage or any PDO voltage, V_{BUS}-5% is nominal low voltage limit, Shift coefficient V_{SHUSBL} is programmable by NVM from 1% to 15% of V_{BUS} by step of 1%, Default $V_{SHUSBL1/2/3}$ = 15%, $V_{MONUSBL1/2/3}$ = V_{BUS}-20% (5 V USB Type-C or any PDO)		V_{BUS}-5% -V_{SHUSBL}		V
DISCH pin driving						
I_{DISPWR}	Power system discharge current	Through external resistor connected to DISCH pin			500	mA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Digital input/output (SCL, SDA, ALERT, RESET, ATTACH, A_B_SIDE, POWER_OK3, GPIO, ADDR0, ADDR1)						
V_{IH}	High level input voltage		1.2			V
V_{IL}	Low level input voltage				0.35	V
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V
20 V open drain outputs (VBUS_EN_SNK, DISCH, POWER_OK2)						
V_{OL}	Low level output voltage	Ioh = 3 mA			0.4	V

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 QFN24 EP 4x4 mm package information

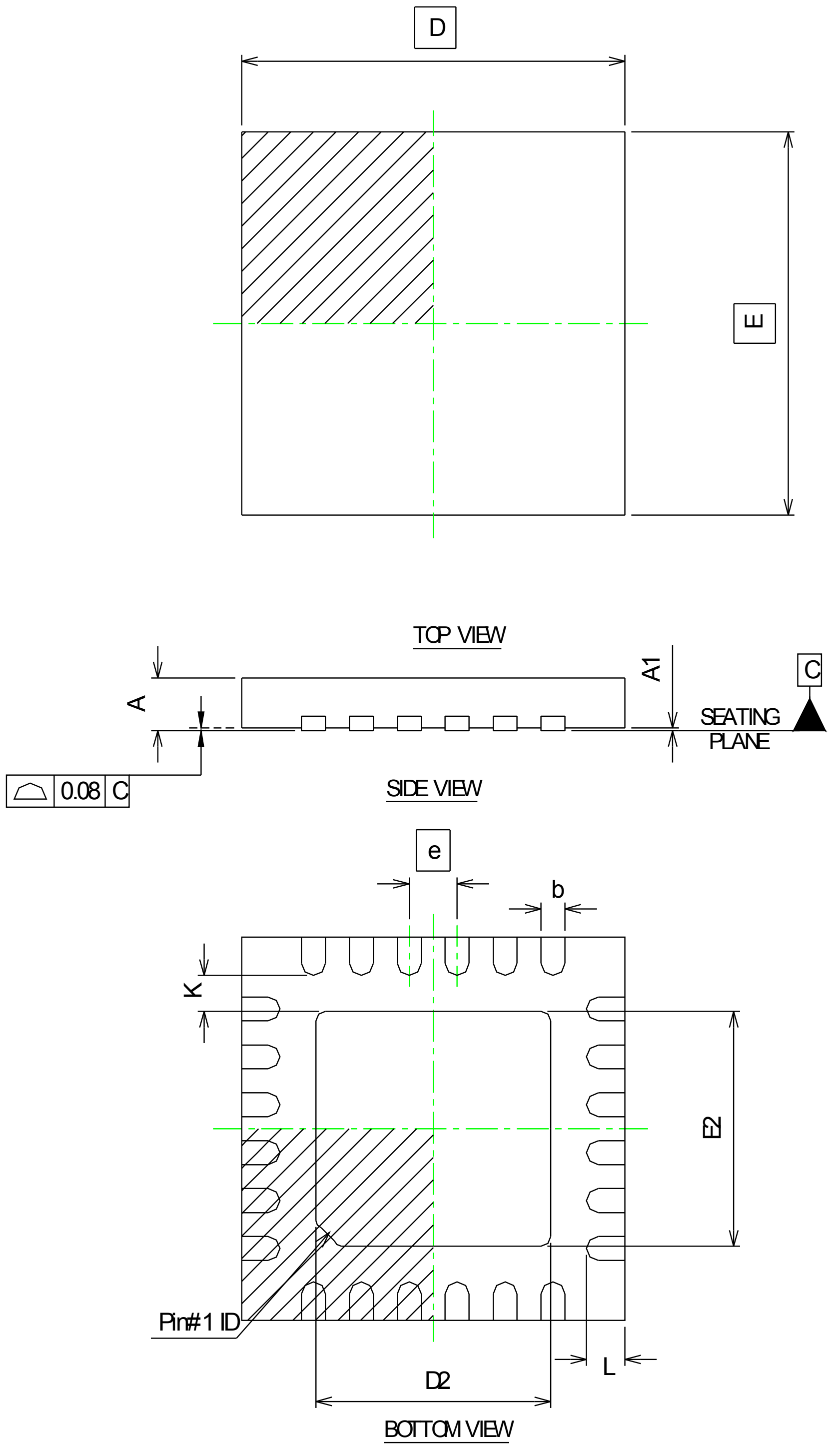
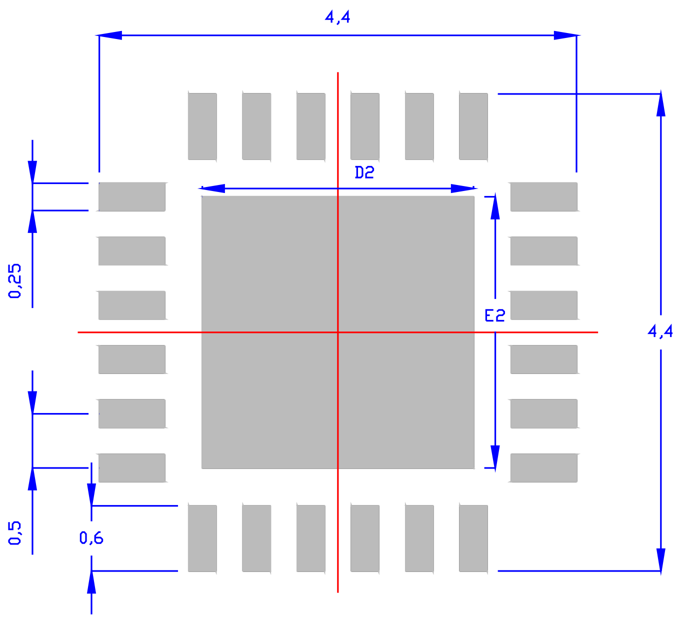


Figure 8. QFN24 EP 4x4 mm package information

Table 23. **QFN24 EP 4x4 mm package mechanical data**

Ref.	Millimeters			Inches		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.0010	0.012
D	3.95	4.00	4.05	0.156	0.157	0.159
D2	2.55	2.70	2.80	0.100	0.106	0.110
E	3.95	4.00	4.05	0.156	0.157	0.159
E2	2.55	2.70	2.80	0.100	0.106	0.110
e	0.45	0.50	0.55	0.018	0.020	0.022
K	0.15	-	-	0.006	-	-
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 9. **QFN24 EP 4x4 mm recommended footprint**



8.2 Thermal information

Table 24. **Thermal information**

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	5	

9 Terms and abbreviations

Table 25. List of terms and abbreviations

Term	Description
Accessory mode	Debug accessory mode. It is defined by the presence of pull-up resistors R_p/R_p on CC1/CC2 pins in sink power role.
DFP	Downstream facing port, specifically associated with the flow of data in a USB connection. Typically the ports on a HOST or the ports on a hub to which devices are connected. In its initial state, the DFP sources V_{BUS} and V_{CONN}, and supports data.
DRP	Dual-role port. A port that can operate as either a source or a sink. The port role may be changed dynamically.
Sink	Port asserting R_d on the CC pins and consuming power from the V_{BUS}; most commonly a device.
Source	Port asserting R_p on the CC pins and providing power over the V_{BUS}; most commonly a host or hub DFP.
UFP	Upstream facing port, specifically associated with the flow of data in a USB connection. The port on a device or a hub that connects to a host or the DFP of a hub. In its initial state, the UFP sinks V_{BUS} and supports data.

Revision history

Table 26. **Document revision history**

Date	Revision	Changes
06-Apr-2018	1	Initial release.

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