STQ1NK80ZR-AP - STN1NK80Z
STD1NK80Z - STD1NK80Z-1

N-CHANNEL 800V - 13 Ω - 1 A TO-92 /SOT-223/DPAK/IPAK
Zener - Protected SuperMESH™ MOSFET

Table 1: General Features

<table>
<thead>
<tr>
<th>TYPE</th>
<th>V&lt;sub&gt;DSS&lt;/sub&gt;</th>
<th>R&lt;sub&gt;DS(on)&lt;/sub&gt;</th>
<th>I&lt;sub&gt;D&lt;/sub&gt;</th>
<th>P&lt;sub&gt;w&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>STQ1NK80ZR-AP</td>
<td>800 V</td>
<td>&lt; 16 Ω</td>
<td>0.3 A</td>
<td>3 W</td>
</tr>
<tr>
<td>STN1NK80Z</td>
<td>800 V</td>
<td>&lt; 16 Ω</td>
<td>0.25 A</td>
<td>2.5 W</td>
</tr>
<tr>
<td>STD1NK80Z</td>
<td>800 V</td>
<td>&lt; 16 Ω</td>
<td>1.0 A</td>
<td>45 W</td>
</tr>
<tr>
<td>STD1NK80Z-1</td>
<td>800 V</td>
<td>&lt; 16 Ω</td>
<td>1.0 A</td>
<td>45 W</td>
</tr>
</tbody>
</table>

- TYPICAL R<sub>DS(on)</sub> = 13Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST’s well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- AC ADAPTORS AND BATTERY CHARGERS
- SWITH MODE POWER SUPPLIES (SMPS)

Table 2: Order Codes

<table>
<thead>
<tr>
<th>SALES TYPE</th>
<th>MARKING</th>
<th>PACKAGE</th>
<th>PACKAGING</th>
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<tr>
<td>STQ1NK80ZR-AP</td>
<td>Q1NK80ZR</td>
<td>TO-92</td>
<td>AMMOPAK</td>
</tr>
<tr>
<td>STN1NK80Z</td>
<td>N1NK80Z</td>
<td>SOT-223</td>
<td>TAPE &amp; REEL</td>
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<tr>
<td>STD1NK80ZT4</td>
<td>D1NK80Z</td>
<td>DPAK</td>
<td>TAPE &amp; REEL</td>
</tr>
<tr>
<td>STD1NK80Z-1</td>
<td>D1NK80Z</td>
<td>IPAK</td>
<td>TUBE</td>
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</table>

Figure 1: Package

Figure 2: Internal Schematic Diagram

Rev. 3
Table 3: Absolute Maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Drain-source Voltage ($V_{GS} = 0$)</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DGR}$</td>
<td>Drain-gate Voltage ($R_{GS} = 20 k\Omega$)</td>
<td>800</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-source Voltage</td>
<td>± 30</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current (continuous) at $T_C = 25^\circ C$</td>
<td>0.3</td>
<td>A</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Drain Current (continuous) at $T_C = 100^\circ C$</td>
<td>0.19</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}(\dagger)$</td>
<td>Drain Current (pulsed)</td>
<td>5</td>
<td>A</td>
</tr>
<tr>
<td>$P_{TOT}$</td>
<td>Total Dissipation at $T_C = 25^\circ C$</td>
<td>3</td>
<td>W</td>
</tr>
<tr>
<td>$V_{ESD(G-S)}$</td>
<td>Gate source ESD ($C_{HBM} = 100pF$, $R = 1.5k\Omega$)</td>
<td>1000</td>
<td>V</td>
</tr>
<tr>
<td>$dv/dt$</td>
<td>Peak Diode Recovery voltage slope</td>
<td>4.5</td>
<td>V/\text{ns}</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Operating Junction Temperature</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{Stg}$</td>
<td>Storage Temperature</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

($\dagger$) Pulse width limited by safe operating area
(1) $I_{SD} \leq 1$ A, $di/dt \leq 200$ A/µs, $V_{DD} \leq 640$

Table 4: Thermal Data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>TO-92</th>
<th>SOT-223</th>
<th>DPAK/IPAK</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{thj-case}$</td>
<td>Thermal Resistance Junction-case Max</td>
<td>--</td>
<td>--</td>
<td>2.78</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{thj-amb}(#)$</td>
<td>Thermal Resistance Junction-ambient Max</td>
<td>120</td>
<td>50</td>
<td>100</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{thj-lead}$</td>
<td>Thermal Resistance Junction-lead Max</td>
<td>40</td>
<td>--</td>
<td>--</td>
<td>°C/W</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Maximum Lead Temperature For Soldering Purpose</td>
<td>260</td>
<td>--</td>
<td>300</td>
<td>°C</td>
</tr>
</tbody>
</table>

(\#) When mounted on 1inch² FR-4 BOARD, 2 oz Cu

Table 5: Avalanche Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Max Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{AR}$</td>
<td>Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_J$ max)</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single Pulse Avalanche Energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)</td>
<td>50</td>
<td>mJ</td>
</tr>
</tbody>
</table>

Table 6: GATE-SOURCE ZENER DIODE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BV_{GSO}$</td>
<td>Gate-Source Breakdown Voltage</td>
<td>$Igs=\pm$ 1mA (Open Drain)</td>
<td>30</td>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.
### ELECTRICAL CHARACTERISTICS (\(T_{\text{CASE}} = 25^\circ\text{C} \text{ UNLESS OTHERWISE SPECIFIED})

#### Table 7: On/Off

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{(BR)DSS})</td>
<td>Drain-source Breakdown Voltage</td>
<td>(I_D = 1) mA, (V_{GS} = 0)</td>
<td>800</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{DSS})</td>
<td>Zero Gate Voltage Drain Current ((V_{GS} = 0))</td>
<td>(V_{DS} = ) Max Rating</td>
<td>1</td>
<td>50</td>
<td></td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(I_{GSS})</td>
<td>Gate-body Leakage Current ((V_{DS} = 0))</td>
<td>(V_{GS} = \pm 20) V</td>
<td>±10</td>
<td></td>
<td></td>
<td>(\mu)A</td>
</tr>
<tr>
<td>(V_{GS(TH)})</td>
<td>Gate Threshold Voltage</td>
<td>(V_{DS} = V_{GS}, \ I_D = 50) (\mu)A</td>
<td>3</td>
<td>3.75</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>(R_{DS(on)})</td>
<td>Static Drain-source On Resistance</td>
<td>(V_{GS} = 10) V, (I_D = 0.5) A</td>
<td>13</td>
<td>16</td>
<td></td>
<td>(\Omega)</td>
</tr>
</tbody>
</table>

#### Note:
1. Pulsed: Pulse duration = 300 \(\mu\)s, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. \(C_{\text{oss eq.}}\) is defined as a constant equivalent capacitance giving the same charging time as \(C_{\text{oss}}\) when \(V_{DS}\) increases from 0 to 80\% \(V_{DSS}\).

#### Table 8: Dynamic

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(g_{fs}) (1)</td>
<td>Forward Transconductance</td>
<td>(V_{DS} = 15) V, (I_D = 0.5) A</td>
<td>0.8</td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td>(C_{oss})</td>
<td>Input Capacitance</td>
<td>(V_{DS} = 25) V, (f = 1) MHz, (V_{GS} = 0)</td>
<td>160</td>
<td>26</td>
<td>6.7</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{oss})</td>
<td>Output Capacitance</td>
<td>(V_{DS} = 0) V, (V_{DS} = 0) to 640V</td>
<td>9.5</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(C_{oss eq.})</td>
<td>Equivalent Output Capacitance</td>
<td>(V_{DD} = 640) V, (I_D = 1.0) A, (V_{GS} = 10) V (see Figure 24)</td>
<td>7.7</td>
<td>1.4</td>
<td>4.5</td>
<td>nC</td>
</tr>
<tr>
<td>(t_{on})</td>
<td>Turn-on Delay Time</td>
<td>(V_{DD} = 400) V, (I_D = 0.5) A (R_{G} = 4.7) (\Omega), (V_{GS} = 10) V (see Figure 21)</td>
<td>8</td>
<td>30</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{rr})</td>
<td>Rise Time</td>
<td>(V_{DD} = 50) V, (T_{j} = 25^\circ)C (see Figure 22)</td>
<td>365</td>
<td>802</td>
<td>4.4</td>
<td>nC</td>
</tr>
<tr>
<td>(t_{off})</td>
<td>Turn-off Delay Time</td>
<td>(V_{DD} = 50) V, (T_{j} = 150^\circ)C (see Figure 22)</td>
<td>388</td>
<td>802.7</td>
<td>4.6</td>
<td>nC</td>
</tr>
</tbody>
</table>

#### Table 9: Source Drain Diode

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(I_{SD})</td>
<td>Source-drain Current</td>
<td>(I_{SD} = 1.0) A, (V_{GS} = 0)</td>
<td>1.0</td>
<td></td>
<td>5</td>
<td>A</td>
</tr>
<tr>
<td>(I_{SDM}) (2)</td>
<td>Source-drain Current (pulsed)</td>
<td>(I_{SD} = 1.0) A, (V_{GS} = 0)</td>
<td>1.0</td>
<td></td>
<td>5</td>
<td>A</td>
</tr>
<tr>
<td>(V_{SD(1)})</td>
<td>Forward On Voltage</td>
<td>(I_{SD} = 1.0) A, (V_{GS} = 0)</td>
<td>1.6</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(I_{tr})</td>
<td>Reverse Recovery Time</td>
<td>(I_{SD} = 1.0) A, (dI/dt = 100) A/(\mu)s (V_{DD} = 50) V, (T_{j} = 25^\circ)C (see Figure 22)</td>
<td>365</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(Q_{tr})</td>
<td>Reverse Recovery Charge</td>
<td>(I_{SD} = 1.0) A, (dI/dt = 100) A/(\mu)s (V_{DD} = 50) V, (T_{j} = 150^\circ)C (see Figure 22)</td>
<td>388</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(I_{RRM})</td>
<td>Reverse Recovery Current</td>
<td>(I_{SD} = 1.0) A, (dI/dt = 100) A/(\mu)s</td>
<td>365</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

#### Note:
1. Pulsed: Pulse duration = 300 \(\mu\)s, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.
3. \(C_{oss eq.}\) is defined as a constant equivalent capacitance giving the same charging time as \(C_{oss}\) when \(V_{DS}\) increases from 0 to 80\% \(V_{DSS}\).
Figure 20: Unclamped Inductive Load Test Circuit

![Unclamped Inductive Load Test Circuit Diagram](image1)

Figure 21: Switching Times Test Circuit For Resistive Load

![Switching Times Test Circuit Diagram](image2)

Figure 22: Test Circuit For Inductive Load Switching and Diode Recovery Times

![Test Circuit For Inductive Load Switching and Diode Recovery Times Diagram](image3)

Figure 23: Unclamped Inductive Waveform

![Unclamped Inductive Waveform Diagram](image4)

Figure 24: Gate Charge Test Circuit

![Gate Charge Test Circuit Diagram](image5)
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com
DPAK FOOTPRINT

All dimensions are in millimeters

TAPE AND REEL SHIPMENT

REEL MECHANICAL DATA

<table>
<thead>
<tr>
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<th>mm</th>
<th>inch</th>
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<tr>
<td>A</td>
<td>330</td>
<td>12.992</td>
</tr>
<tr>
<td>B</td>
<td>1.5</td>
<td>0.059</td>
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<tr>
<td>C</td>
<td>12.8</td>
<td>0.504</td>
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<tr>
<td>D</td>
<td>20.2</td>
<td>0.795</td>
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<td>G</td>
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<td>N</td>
<td>50</td>
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<tr>
<td>T</td>
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BASE QTY | BULK QTY
--- | ---
2500 | 2500

TAPE MECHANICAL DATA

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<td>0.409</td>
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<tr>
<td>D</td>
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<tr>
<td>D1</td>
<td>1.5</td>
<td>0.059</td>
</tr>
<tr>
<td>E</td>
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<td>0.065</td>
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<tr>
<td>F</td>
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<td>P0</td>
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<tr>
<td>P1</td>
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<td>0.311</td>
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<td>P2</td>
<td>1.9</td>
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<td>R</td>
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<td>W</td>
<td>15.7</td>
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All dimensions are in millimeters.
### TO-92 MECHANICAL DATA

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<td>MIN.</td>
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<td>4.32</td>
<td>4.95</td>
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<tr>
<td>b</td>
<td>0.36</td>
<td>0.51</td>
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<tr>
<td>D</td>
<td>4.45</td>
<td>4.95</td>
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<tr>
<td>E</td>
<td>3.30</td>
<td>3.94</td>
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<tr>
<td>e</td>
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<td>2.67</td>
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<td>e1</td>
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<tr>
<td>L</td>
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<td>15.49</td>
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<td>R</td>
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<td>2.41</td>
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<td>S1</td>
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<td>1.52</td>
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<td>W</td>
<td>0.41</td>
<td>0.56</td>
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<tr>
<td>V</td>
<td>5°</td>
<td>5°</td>
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## SOT-223 MECHANICAL DATA

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<th>typ.</th>
<th>max.</th>
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<th>inch</th>
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<td></td>
<td>0.071</td>
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<tr>
<td>B</td>
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<td>B1</td>
<td>2.90</td>
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<td>3.10</td>
<td>0.114</td>
<td>0.118</td>
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<tr>
<td>c</td>
<td>0.24</td>
<td>0.26</td>
<td>0.32</td>
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<td>0.010</td>
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<tr>
<td>D</td>
<td>6.30</td>
<td>6.50</td>
<td>6.70</td>
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<td>0.256</td>
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<td>0.181</td>
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<td>H</td>
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<td>7.30</td>
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<td>10°</td>
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<tr>
<td>A1</td>
<td>0.02</td>
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</tbody>
</table>

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![Diagram](P008B)
TO-252 (DPAK) MECHANICAL DATA

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<th>MIN.</th>
<th>TYP.</th>
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P032P_B
### TO-251 (IPAK) MECHANICAL DATA

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0068771-E
Table 10: Revision History

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