VIPerA16

Automotive grade fixed frequency offline converter

Datasheet - production data

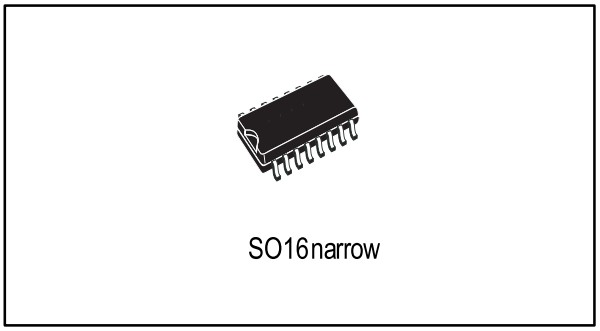
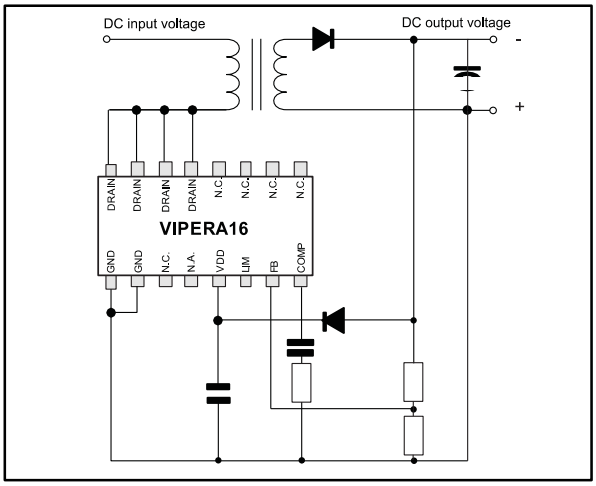


Figure 1: Typical application



Features

- AEC-Q100 qualified
- PPAP capable
- 800 V avalanche rugged power section
- PWM operation with seattle drain current limit (I_{DLim})
- Operating frequency: 115 kHz with jittering for reduced EMI
- No need of auxiliary winding
- No load input power lower than 30 mW at 230 V_{AC}
- On-board soft-start
- Overload/short circuit protection
- Open loop protection
- Auto-restart after a fault condition
- Hysteretic thermal shutdown

Applications

- Auxiliary power supply for automotive

Description

The device is an off-line converter with a 800 V avalanche ruggedness power section, a PWM controller, user defined overcurrent limit, protection against feedback network disconnection, hysteretic thermal protection, soft start up and safe auto restart after any fault condition. It is able to power itself directly from the rectified mains, eliminating the need for an auxiliary bias winding. Advance frequency jittering reduces EMI filter cost. Burst mode operation and the IC low consumption both help to meet the standard set by energy saving regulations.

Table 1: Device summary

Order codes	Package	Packing
VIPERA16HD	SO16 narrow	Tube
VIPERA16HDTR		Tape and reel

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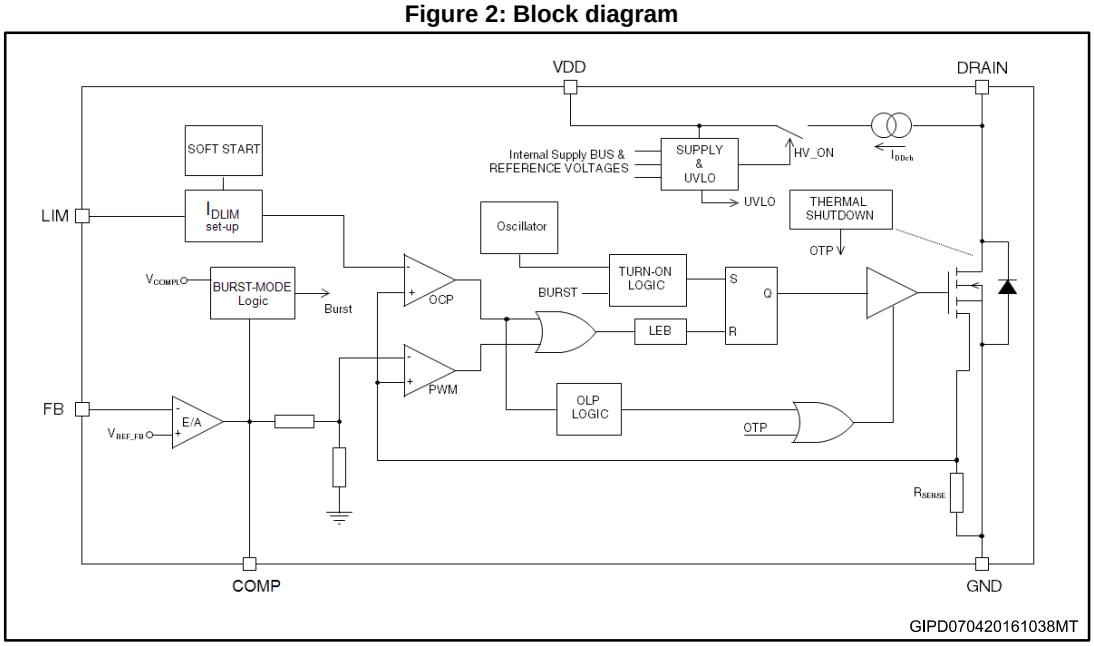
1 Block diagram

Figure 2: Block diagram



2 Typical power

Table 2: Typical power

Part number	230 V_{AC}		85-265 V_{AC}	
	Adapter (1)	**Open frame** (2)	**Adapter** (1)	**Open frame** (2)
VIPERA16	9 W	10 W	5 W	6 W

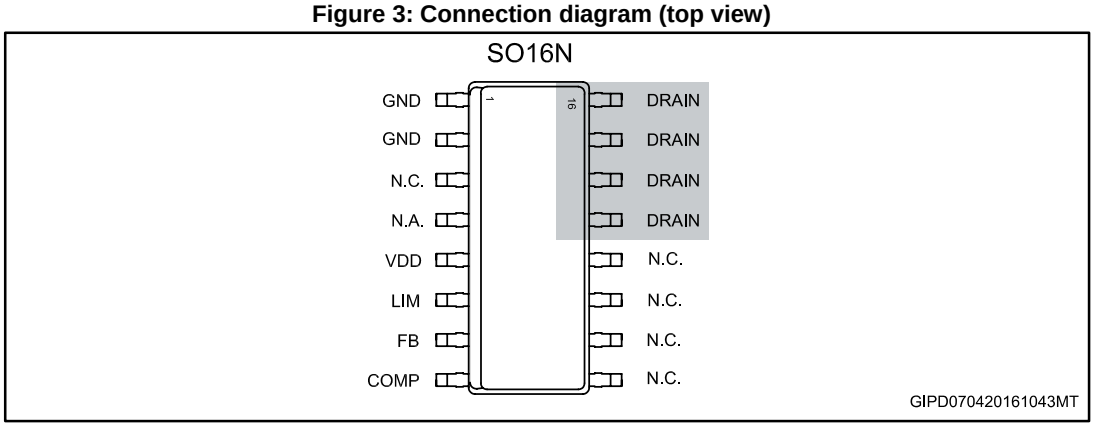
Notes:

(1)Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.

(2)Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat sinking.

3 Pin setting

Figure 3: Connection diagram (top view)



The copper area for heat dissipation has to be designed under the DRAIN pins.

Table 3: Pin description

Pin N.	Name	Function
1-2	GND	Connected to the source of the internal power MOSFET and controller ground reference.
3	N.C.	Not internally connected. This pin can be optionally connected to GND.
4	N.A.	Not available for user. This pin is mechanically connected to the controller die pad of the frame. In order to improve the noise immunity, is highly recommended connect it to GND (pin 1-2).
5	VDD	Supply voltage of the control section. This pin provides the charging current of the external capacitor.
6	LIM	This pin allows setting the drain current limitation to a lower value respect to I_{Dlim}, which is the default one. The pin can be left open if default drain current limitation, I_{Dlim}, is used.
7	FB	Inverting input of the internal trans conductance error amplifier. Connecting the converter output to this pin through a single resistor results in an output voltage equal to the error amplifier reference voltage (see V_{FB_REF} on *Table 8: "Controller section"*). An external resistors divider is required for higher output voltages.
8	COMP	Output of the internal trans conductance error amplifier. The compensation network have to be placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop. The pin is used also to directly control the PWM with an optocoupler. The linear voltage range extends from V_{COMPL} to V_{COMPH} (*Table 8: "Controller section"*).
9 -12	N.C.	Not connected.
13-16	DRAIN	MOSFET drain. The internal high-voltage current source sinks current from this pin to charge the VDD capacitor at startup and during steady-state operation. These pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB, some copper area must be placed under these pins in order to decrease the total junction-to-ambient thermal resistance thus facilitating the power dissipation.

4 Electrical data

4.1 Maximum ratings

Table 4: Absolute maximum ratings

Symbol	Pin	Parameter	Value		Unit
			Min.	Max.	
V_{DRAIN}	13, 16	Drain-to-source (ground) voltage		800	V
		Drain-to-source (ground) voltage (T_J = -40 °C - 25 °C)		750	
E_{AV}	13, 16	Repetitive avalanche energy (limited by T_J = 150 °C)		2	mJ
I_{AR}	13, 16	Repetitive avalanche current (limited by T_J = 150 °C)		1	A
I_{DRAIN}	13, 16	Pulse drain current (limited by T_J = 150 °C)		2.5	A
V_{COMP}	8	Input pin voltage	-0.3	3.5	V
V_{FB}	7	Input pin voltage	-0.3	4.8	V
V_{LIM}	6	Input pin voltage	-0.3	2.4	V
V_{DD}	5	Supply voltage	-0.3	Self limited	V
I_{DD}	5	Input current		20	mA
P_{TOT}		Power dissipation at T_A < 60 °C		1	W
T_J		Operating junction temperature range	-40	150	°C
T_{STG}		Storage temperature	-55	150	°C

4.2 Thermal data

Table 5: Thermal data

Symbol	Parameter	Max. value	Unit
R_{thJP}	Thermal resistance junction pin (dissipated power = 1 W)	35	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W)	110	°C/W
R_{thJA}	Thermal resistance junction ambient (dissipated power = 1 W) (1)	80	°C/W

Notes:

(1)When mounted on a standard single side FR4 board with 100 mm^2 (0.155 sq. in) of Cu (35 µm thick).

4.3 Electrical characteristics

T_J = -40 to 125 °C, V_{DD} = 14 V[a]

Table 6: Power section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	I_{DRAIN} = 1 mA, V_{COMP} = GND, T_J = 25 °C	800			V
I_{OFF}	OFF state drain current	V_{DRAIN} = max. rating, V_{COMP} = GND			70	µA
$R_{DS(on)}$	Drain-source ON state resistance	I_{DRAIN} = 0.2 A, T_J = 25 °C		20	24	Ω
		I_{DRAIN} = 0.2 A, T_J = 125 °C		43	52	Ω
C_{OSS}	Effective (energy related) output capacitance	V_{DRAIN} = 0 to 640 V		10		pF

Table 7: Supply section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Voltage						
V_{DRAIN_START}	Drain-source start voltage		40	50	60	V
I_{DDch1}	Startup charging current	V_{DRAIN} = 100 V to 640 V, V_{DD} = 4 V	-0.6		-1.8	mA
I_{DDch2}	Charging current during operation	V_{DRAIN} = 100 V to 640 V, V_{DD} = 9 V falling edge	-7		-13	mA
V_{DD}	Operating voltage range		11.5		23.5	V
$V_{DDclamp}$	V_{DD} clamp voltage	I_{DD} = 15 mA	23.5			V
V_{DDon}	V_{DD} startup threshold		12	13	14	V
V_{DDCSon}	V_{DD} on internal high voltage current generator threshold		9.5	10.5	11.5	V
V_{DDoff}	V_{DD} undervoltage shutdown threshold				7	V
Current						
I_{DD0}	Operating supply current, not switching	F_{OSC} = 0 kHz, V_{COMP} = GND			0.6	mA
		F_{OSC} = 0 kHz, V_{COMP} = GND (T_J = 125 °C)			0.7	mA
I_{DD1}	Operating supply current, switching	V_{DRAIN} = 120 V			1.5	mA
I_{DDoff}	Operating supply current with V_{DD} < V_{DDoff}	V_{DD} < V_{DDoff}			0.35	mA
I_{DDol}	Open loop failure current threshold	V_{DD} = $V_{DDclamp}$ V_{COMP} = 3.3 V	4			mA

[a] Adjust V_{DD} above V_{DDon} startup threshold before setting to 14 V.

Table 8: Controller section

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Error amplifier						
V_{REF_FB}	FB reference voltage		3.2	3.3	3.4	V
$I_{FB\_PULL\ UP}$	Current pull-up			-1		µA
G_M	Transconductance			2		mA/V
Current setting (LIM) pin						
V_{LIM_LOW}	Low level clamp voltage	I_{LIM} = -100 µA		0.5		V
Compensation (COMP) pin						
V_{COMPH}	Upper saturation limit	T_J = 25 °C		3		V
V_{COMPL}	Burst mode threshold	T_J = 25 °C	1	1.1	1.2	V
V_{COMPL_HYS}	Burst mode hysteresis	T_J = 25 °C		40		mV
H_{COMP}	ΔV_{COMP} /ΔI_{DRAIN}		4		9	V/A
$R_{COMP(DYN)}$	Dynamic resistance	V_{FB} = GND		15		kΩ
I_{COMP}	Source / sink current	V_{FB} > 100 mV		150		µA
	Max. source current	V_{COMP} = GND, V_{FB} = GND		220		µA
Current limitation						
I_{Dlim}	Drain current limitation	I_{LIM} = -10 µA, V_{COMP} = 3.3 V	0.36	0.40	0.44	A
t_{SS}	Soft-start time			8.5		ms
T_{ON_MIN}	Minimum turn-on time				450	ns
I_{Dlim_bm}	Burst mode current limitation	V_{COMP} = V_{COMPL}		85		mA
Overload						
t_{OVL}	Overload time			50		ms
$t_{RESTART}$	Restart time after fault			1		s
Oscillator section						
F_{OSC}	Switching frequency		103	115	127	kHz
		T_J = -40 °C -25 °C	85		115	kHz
F_D	Modulation depth	F_{OSC} = 115 kHz		±8		kHz
F_M	Modulation frequency			230		Hz
D_{MAX}	Maximum duty cycle		70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature		150	160		°C
T_{HYST}	Thermal shutdown hysteresis			30		°C

5 Typical electrical characteristics

Figure 4: I_{Dlim} vs T_J

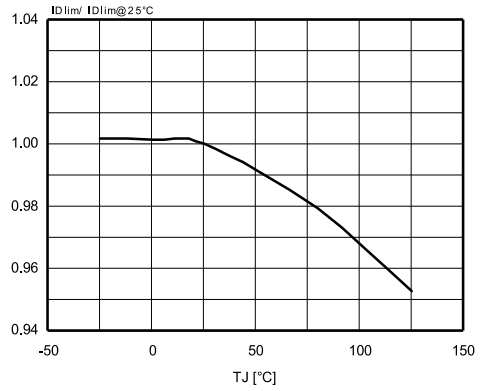


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Figure 5: F_{OSC} vs T_J

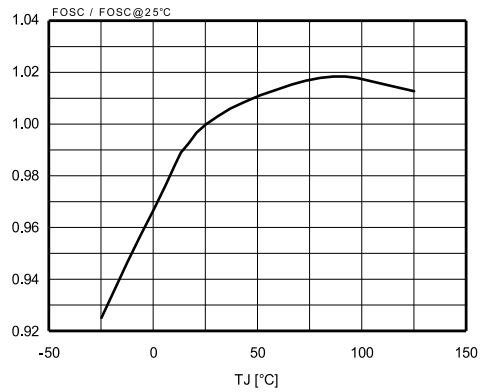

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Figure 6: V_{DRAIN_START} vs T_J

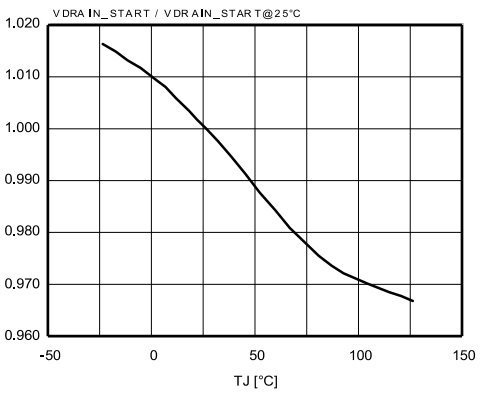

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Figure 7: H_{COMP} vs T_J

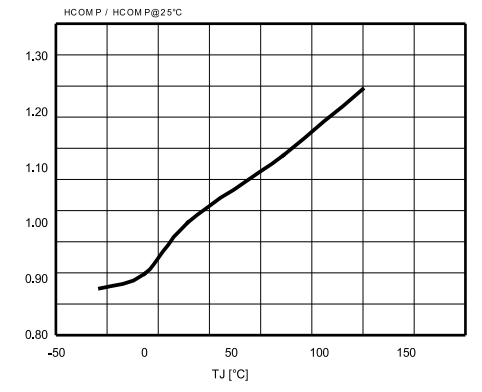

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Figure 8: G_M vs T_J

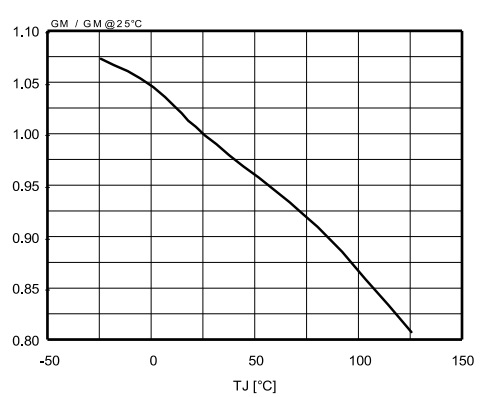

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Figure 9: V_{REF_FB} vs T_J

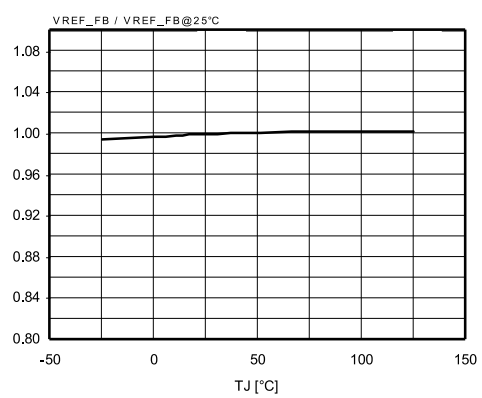

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Figure 10: I_{COMP} vs T_J

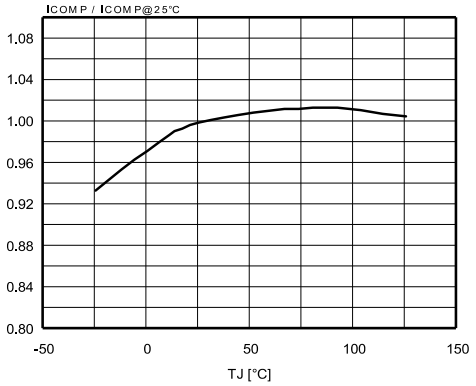

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Figure 11: Operating supply current

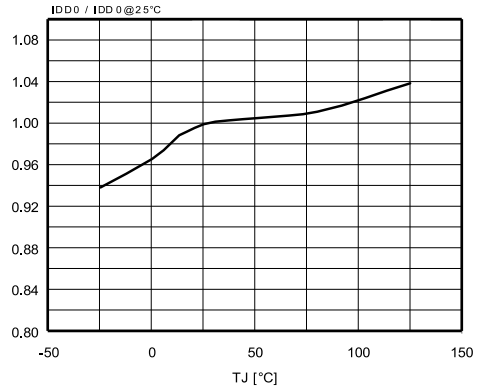

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Figure 12: Operating supply current (switching) vs T_J

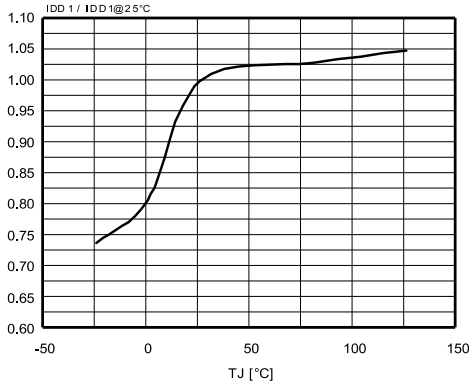

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Figure 13: I_{Dlim} vs R_{LIM}

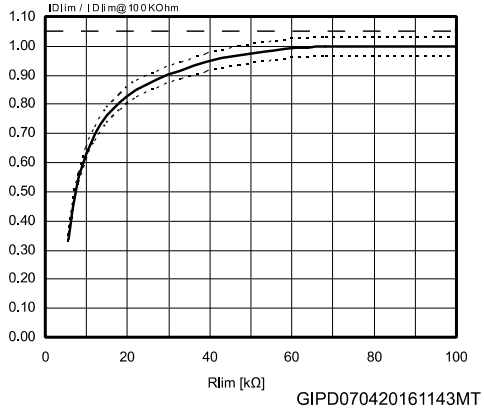

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Figure 14: Power MOSFET on-resistance vs T_J

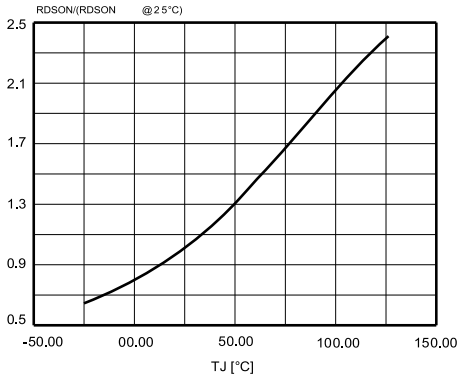

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Figure 15: Power MOSFET break down voltage vs T_J

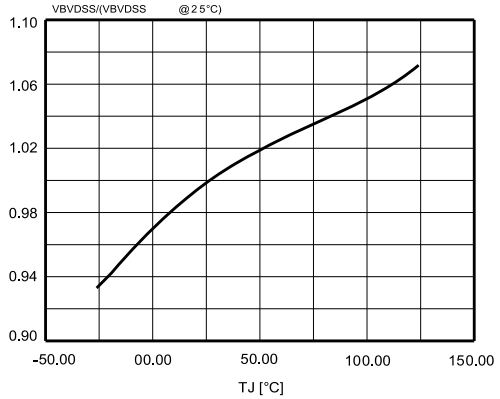

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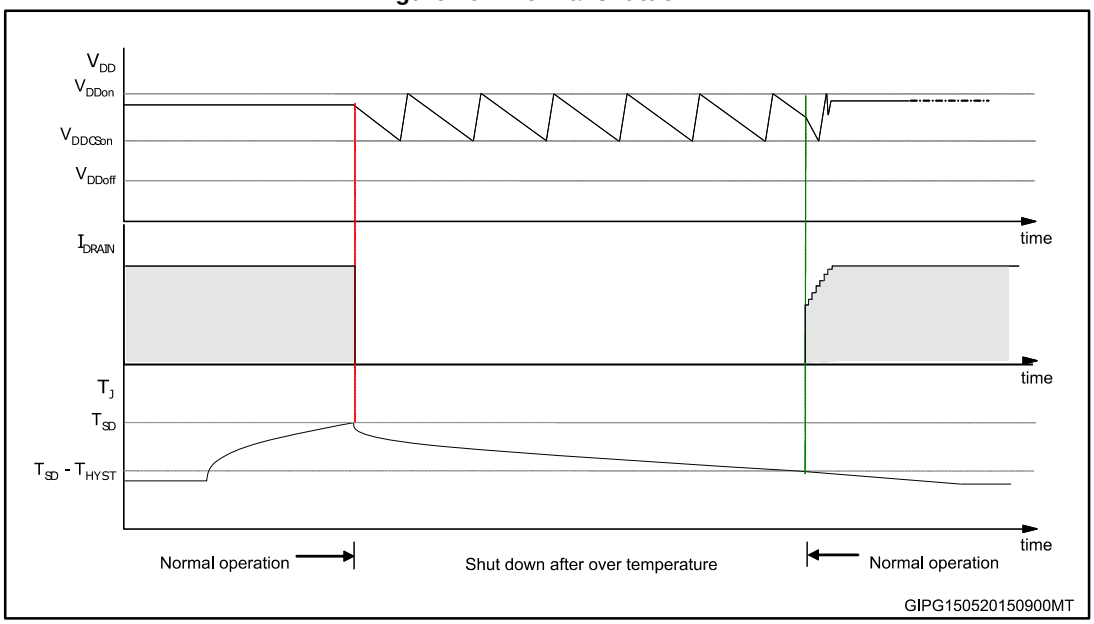
Figure 16: Thermal shutdown



6 Typical circuit

Figure 17: Buck converter

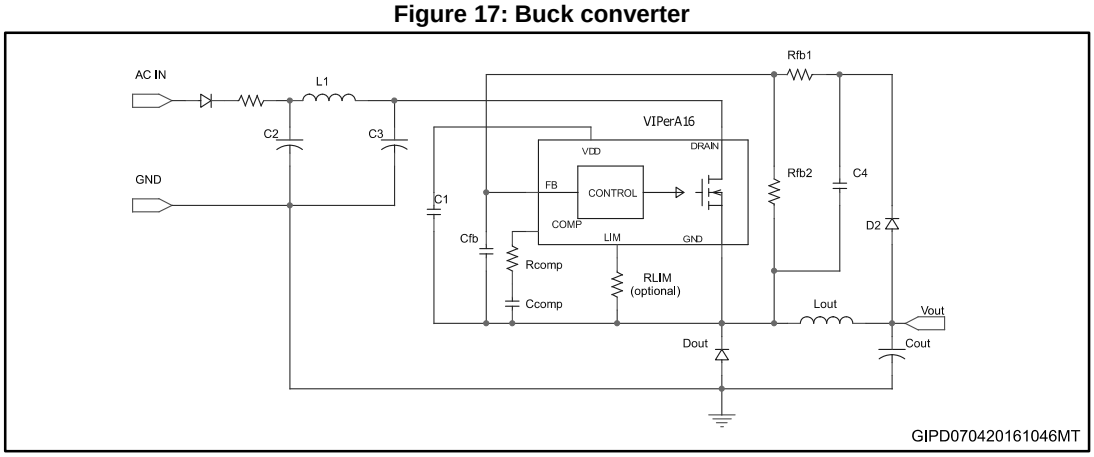


Figure 18: Buck boost converter

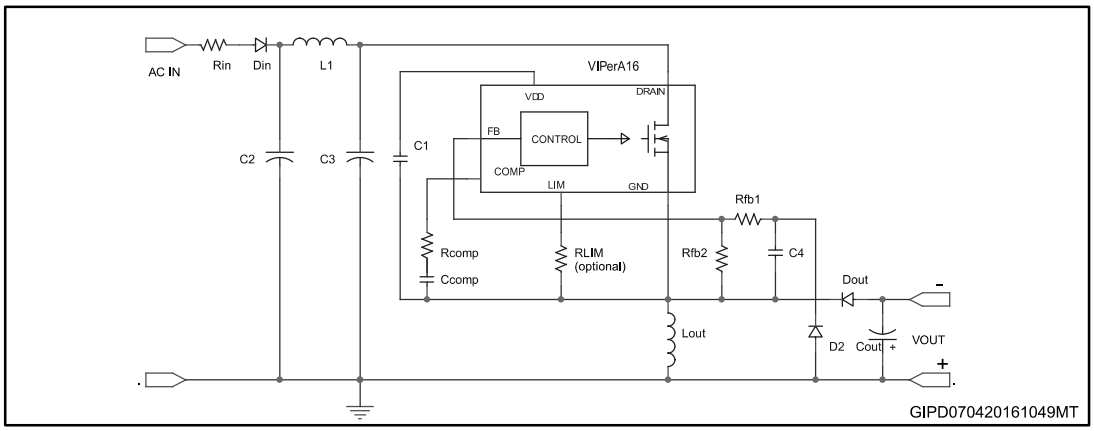


Figure 19: Flyback converter (primary regulation)

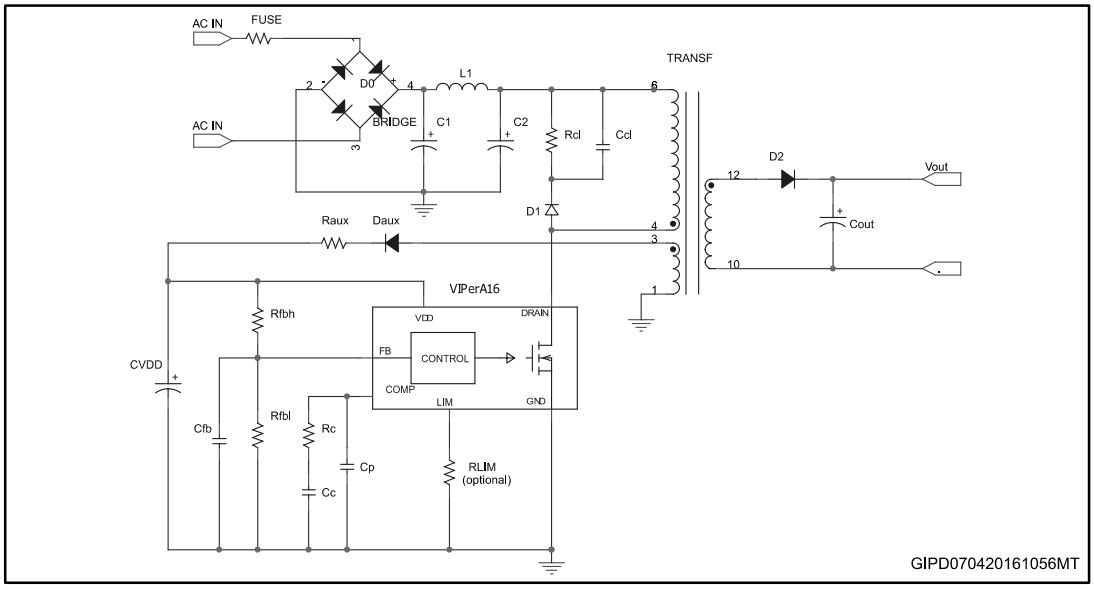
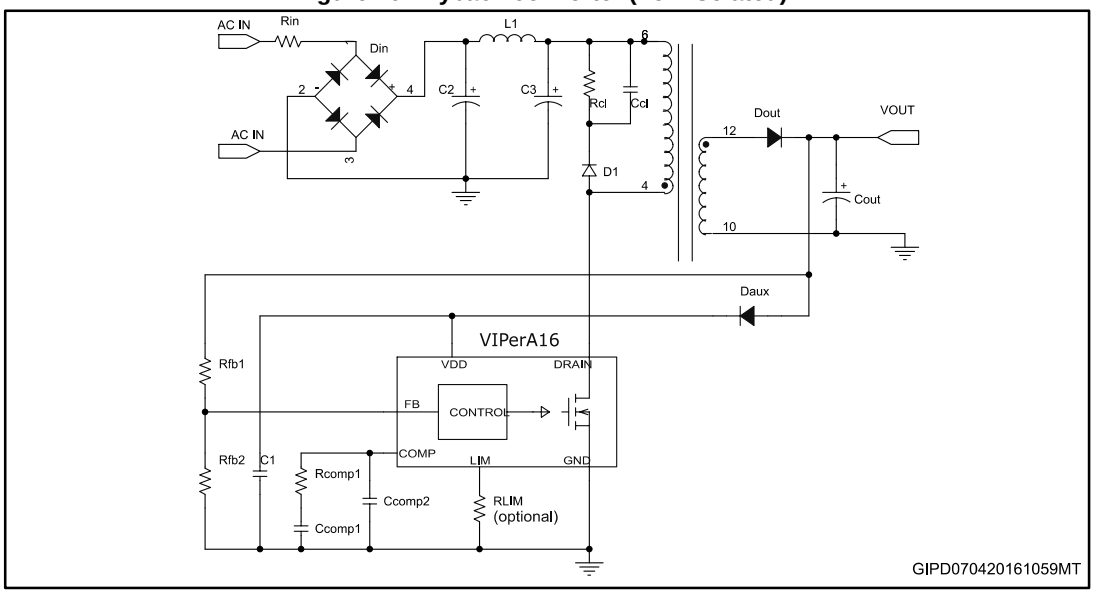


Figure 20: Flyback converter (non-isolated)



7 Power section

The power section is implemented with an N-channel Power MOSFET with a breakdown voltage of 800 V min. and a typical $R_{DS(on)}$ of 20 Ω. It includes a SenseFET structure to allow a virtually lossless current sensing and thermal sensor.

The gate driver of the Power MOSFET is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize common mode EMI. During UVLO conditions, an internal pull-down circuit holds the gate low in order to ensure that the Power MOSFET cannot be turned on accidentally.

8 High voltage current generator

The high voltage current generator is supplied by the DRAIN pin. At the first startup of the converter it is enabled when the voltage across the input bulk capacitor reaches the V_{DRAIN_START} threshold, sourcing an I_{DDch1} current (see *Table 7: "Supply section "*); as the V_{DD} voltage reaches the V_{DDon} threshold, the power section starts switching and the high voltage current generator is turned OFF. The device is powered by the energy stored in the V_{DD} capacitor.

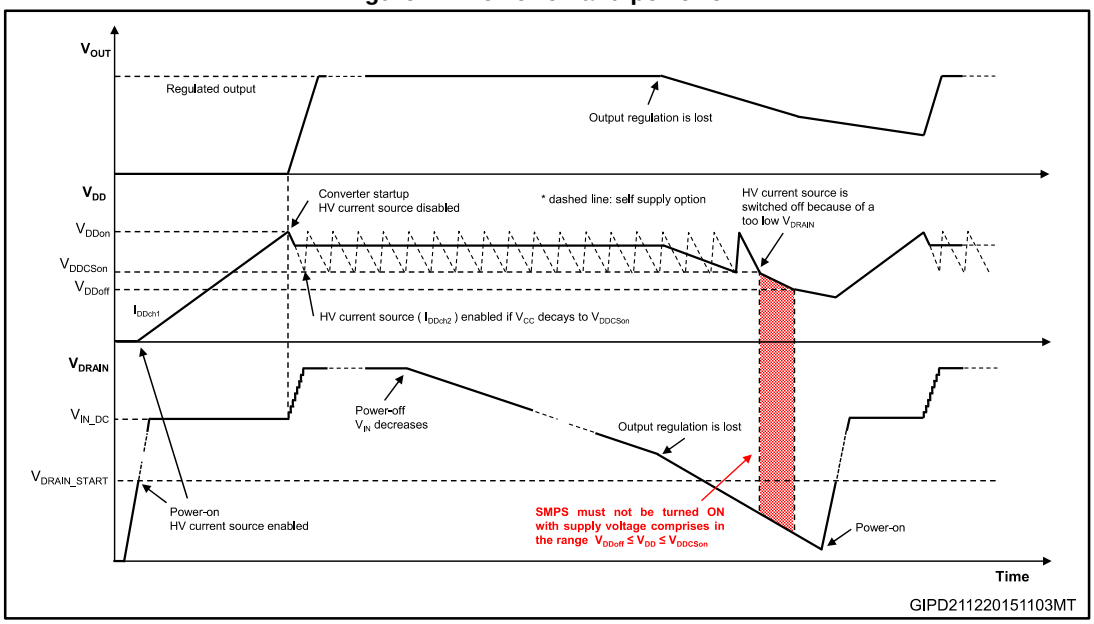
In steady-state condition, if the self-biasing function is used, the high voltage current generator is activated between V_{DDCSon} and V_{DDon} (see *Table 7: "Supply section "*), delivering I_{DDch2} to the V_{DD} capacitor during the MOSFET OFF time (see *Figure 21: "Power-on and power-off"*).

The device can also be supplied through the auxiliary winding; in this case the high voltage current source is disabled during steady-state operation, provided that VDD is above V_{DDCSon}.

At converter power-down, the V_{DD} voltage drops and the converter activity stops as it falls below the V_{DDoff} threshold (see *Table 7: "Supply section "*).

In case of repeated restart, in order to ensure safe operations, the converter power-on must be avoided when the V_{DD} supply voltage is comprised in the range $V_{DDoff} < V_{DD} < V_{ddcson}$.

Figure 21: Power-on and power-off



9 Oscillator

The switching frequency is internally fixed at 115 kHz. The switching frequency is modulated by approximately ±8 kHz at a 230 Hz (typical) rate, so that the resulting spread-spectrum action distributes the energy of each harmonic of the switching frequency over a number of sideband harmonics having the same energy on the whole but smaller amplitudes.

10 Soft start

During the startup phase of converters, the soft-start function progressively increases the cycle-by-cycle drain current limit, up to the default value I_{Dlim}. By this way the drain current is further limited and the output voltage is progressively increased reducing the stress on the secondary diode. The soft-start time is internally fixed to t_{SS}, see typical value in *Table 8: "Controller section"*, and the function is activated for any attempt of converter startup and after a fault event.

This function helps prevent saturation of transformers during startup and short-circuit.

11 Adjustable current limit set point

The device includes a current mode PWM controller: cycle-by-cycle, the drain current is sensed through the integrated resistor R_{SENSE} and the voltage is applied to the non-inverting input of the PWM comparator, see *Figure 2: "Block diagram"*. As soon as the sensed voltage is equal to the voltage derived from the COMP pin, the Power MOSFET is switched off.

In parallel with the PWM operations, the comparator OCP, see *Figure 2: "Block diagram"*, checks the level of the drain current and switch off the Power MOSFET in case the current is higher than the threshold I_{Dlim}, see *Table 8: "Controller section "*.

The level of the drain current limit, I_{Dlim}, can be reduced depending on the sunk current from the LIM pin. The resistor R_{LIM}, between the LIM and GND pins, fixes the current sunk and then the level of the current limit, I_{Dlim}, see *Figure 13: "IDlim vs RLIM"*.

When the LIM pin is left open or if the R_{LIM} has a high value (i.e. > 80 kΩ), the current limit is fixed to its default value, I_{Dlim}, as reported in *Table 8: "Controller section "*.

12 FB pin and COMP pin

The device can be used both in non-isolated and in isolated topology. In case of non-isolated topology, the feedback signal from the output voltage is applied directly to the FB pin as the inverting input of the internal error amplifier having the reference voltage, V_{REF_FB}, see *Table 8: "Controller section "*.

The output of the error amplifier sources and sinks the current, I_{COMP}, respectively to and from the compensation network connected on the COMP pin. This signal is then compared, in the PWM comparator, with the signal coming from the SenseFET; the Power MOSFET is switched off when the two values are the same on a cycle-by-cycle basis, see *Figure 2: "Block diagram"* and *Figure 22: "Feedback circuit"*.

When the power supply output voltage is equal to the error amplifier reference voltage, V_{REF_FB}, a single resistor must be connected from the output to the FB pin. For higher output voltages the external resistor divider is needed. If the voltage on the FB pin is accidentally left floating, an internal pull-up protects the controller.

The output of the error amplifier is externally accessible through the COMP pin and is used for the loop compensation: usually an RC network.

As reported in *Figure 22: "Feedback circuit"*, in case of isolated power supply, the internal error amplifier must be disabled (FB pin shorted to GND). In this case an internal resistor is connected between an internal reference voltage and the COMP pin, see *Figure 22: "Feedback circuit"*. The current loop must be closed on the COMP pin through the opto-transistor in parallel with the compensation network. The V_{COMP} dynamics range is between V_{COMPL} and V_{COMPH}, as reported in *Figure 23: "COMP pin voltage vs. IDRAIN"*.

When the voltage V_{COMP} drops below the voltage threshold V_{COMPL}, the converter enters burst mode, see *Section 13: "Burst mode"*.

When the voltage V_{COMP} rises above the V_{COMPH} threshold, the peak drain current reaches its limit, as well as the deliverable output power.

Figure 22: Feedback circuit

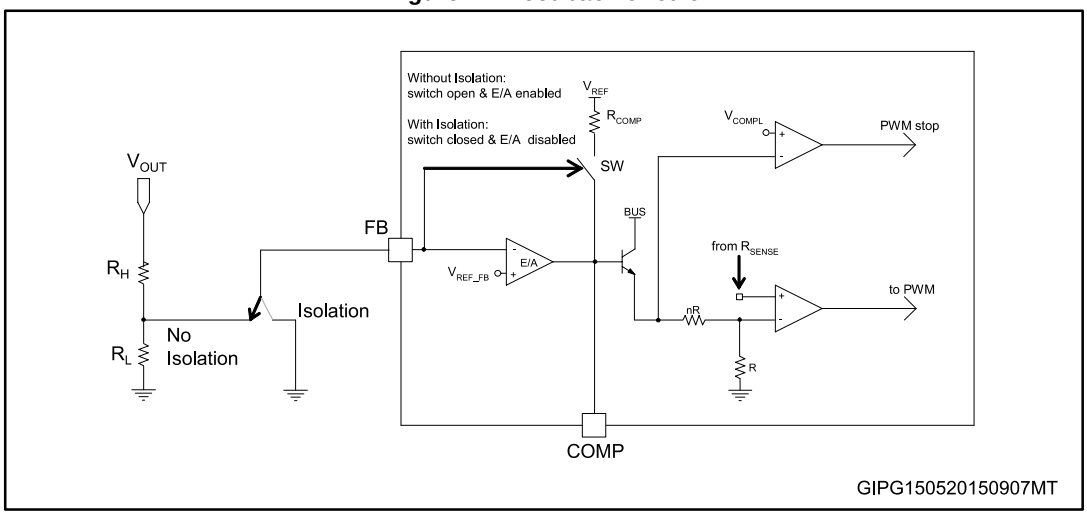
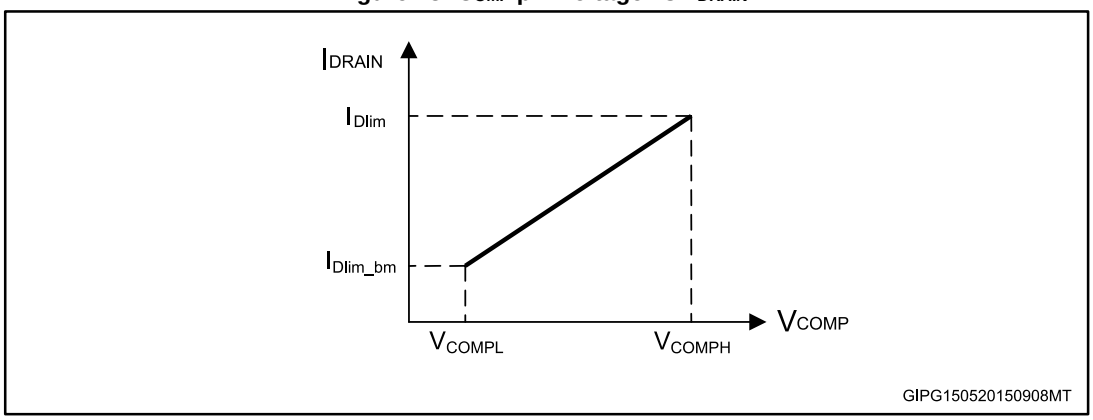


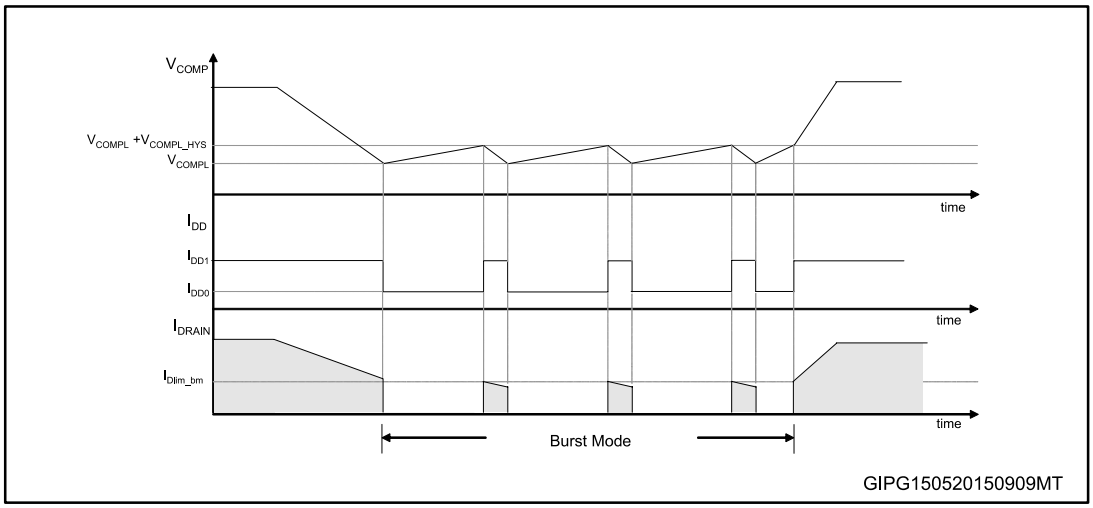
Figure 23: C_{OMP} pin voltage vs. I_{DRAIN}



13 Burst mode

When the voltage V_{COMP} drops below the threshold, V_{COMPL}, the Power MOSFET is kept in an OFF state and the consumption is reduced to the I_{DD0} current, as reported in *Table 7: "Supply section "*. As a reaction to the energy delivery stop, the V_{COMP} voltage increases and as soon as it exceeds the threshold V_{COMPL} + V_{COMPL_HYS}, the converter starts switching again with a consumption level equal to the I_{DD1} current. This ON-OFF operation mode, referred to as “burst mode” and reported in *Figure 24: "Load-dependent operating modes: timing diagrams"*, reduces the average frequency, which can drop even to a few hundred hertz, therefore minimizing all frequency-related losses and making it easier to comply with energy saving regulations. During burst mode, the drain current limit is reduced to the value I_{Dlim_bm} (reported in *Table 8: "Controller section "*) in order to avoid the audible noise issue.

Figure 24: Load-dependent operating modes: timing diagrams



14 Automatic auto-restart after overload or short-circuit

The overload protection is implemented in an automatic way using the integrated up-down counter. Every cycle is incremented or decremented depending on whether the current logic detects the limit condition or not. The limit condition is the peak drain current, I_{Dlim} , reported in *Table 8: "Controller section "* or the one set by the user through the R_{LIM} resistor, as reported in *Figure 13: "IDlim vs RLIM"*. After the reset of the counter, if the peak drain current is continuously equal to the level I_{Dlim}, the counter is incremented till the fixed time, t_{OVL}, after that the Power MOSFET switch-on is disabled. It is activated again, through the soft-start, after the $t_{RESTART}$ time, see *Figure 25: "Timing diagram: OLP sequence (IC externally biased)"* and *Figure 26: "Timing diagram: OLP sequence (IC internally biased)"*, and the mentioned time values in *Table 8: "Controller section "*.

In case of overload or a short-circuit event, the Power MOSFET switching is stopped after a time that depends on the counter and that can be a maximum equal to t_{OVL}. The protection occurs in the same way until the overload condition is removed, see *Figure 25: "Timing diagram: OLP sequence (IC externally biased)"* and *Figure 26: "Timing diagram: OLP sequence (IC internally biased)"*. This protection ensures restart attempts of the converter with low repetition rate, so that it works safely with extreme low power throughput and avoids the IC overheating in case of repeated overload events. If the overload is removed before the protection tripping, the counter is decremented cycle-by-cycle down to zero and the IC is not stopped.

Figure 25: Timing diagram: OLP sequence (IC externally biased)

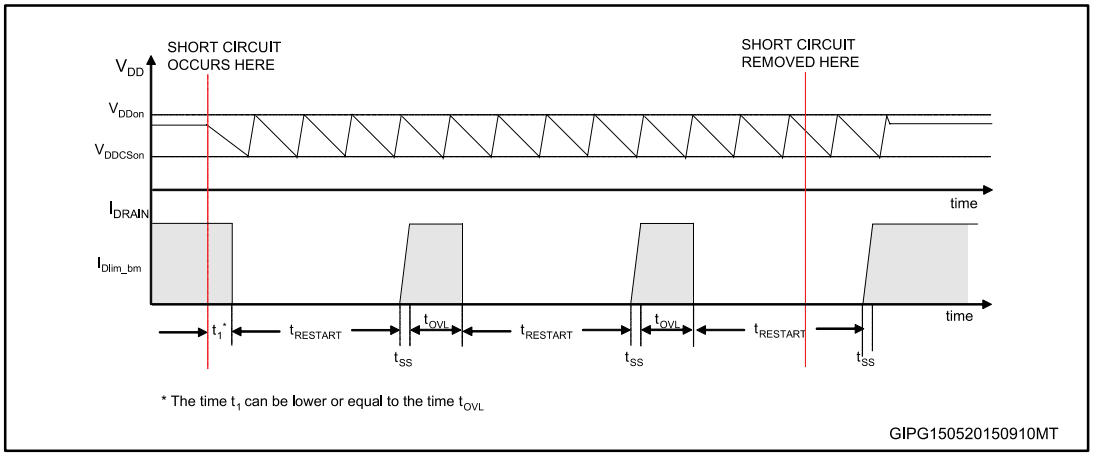
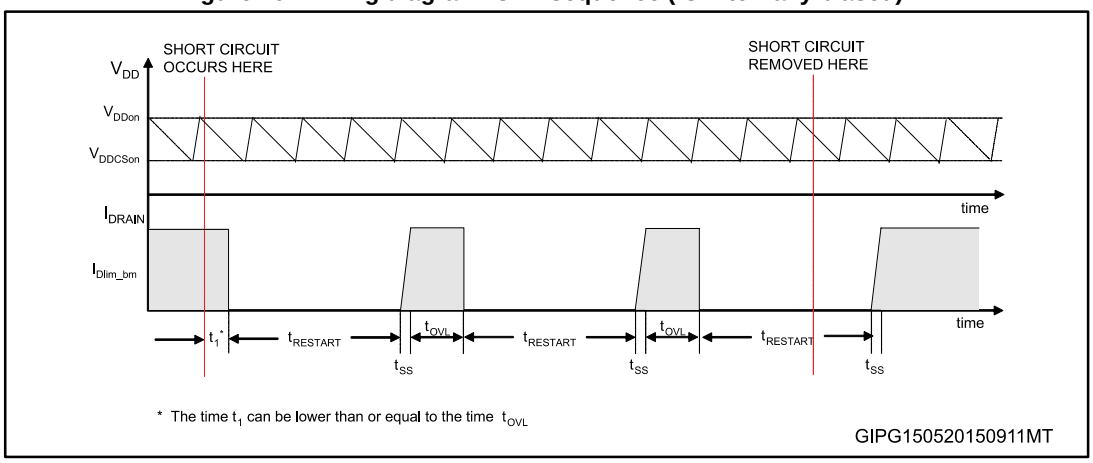


Figure 26: Timing diagram: OLP sequence (IC internally biased)



15 Open loop failure protection

In case the power supply is built in flyback topology and the VIPerA16 is supplied by an auxiliary winding, as shown in *Figure 27: "FB pin connection for non-isolated flyback"* and *Figure 28: "FB pin connection for isolated flyback"*, the converter is protected against feedback loop failure or accidental disconnections of the winding.

The following description is applicable for the schematics of *Figure 27: "FB pin connection for non-isolated flyback"* and *Figure 28: "FB pin connection for isolated flyback"*, respectively the non-isolated flyback and the isolated flyback.

If R_H is opened or R_L is shorted, the VIPerA16 works at its drain current limitation. The output voltage, V_{OUT}, increases and also the auxiliary voltage, V_{AUX}, which is coupled with the output through the secondary-to-auxiliary turns ratio.

As the auxiliary voltage increases up to the internal V_{DD} active clamp, $V_{DDclamp}$ (the value is reported in *Table 8: "Controller section "*) and the clamp current injected on the VDD pin exceeds the latch threshold, I_{DDol} (the value is reported in *Table 8: "Controller section "*), a fault signal is internally generated.

In order to distinguish an actual malfunction from a bad auxiliary winding design, both the above conditions (drain current equal to the drain current limitation and current higher than I_{DDol} through the VDD clamp) must be verified to reveal the fault.

If R_L is opened or R_H is shorted, the output voltage, V_{OUT}, is clamped to the reference voltage V_{REF_FB} (in case of non-isolated flyback) or to the external TL voltage reference (in case of isolated flyback).

Figure 27: FB pin connection for non-isolated flyback

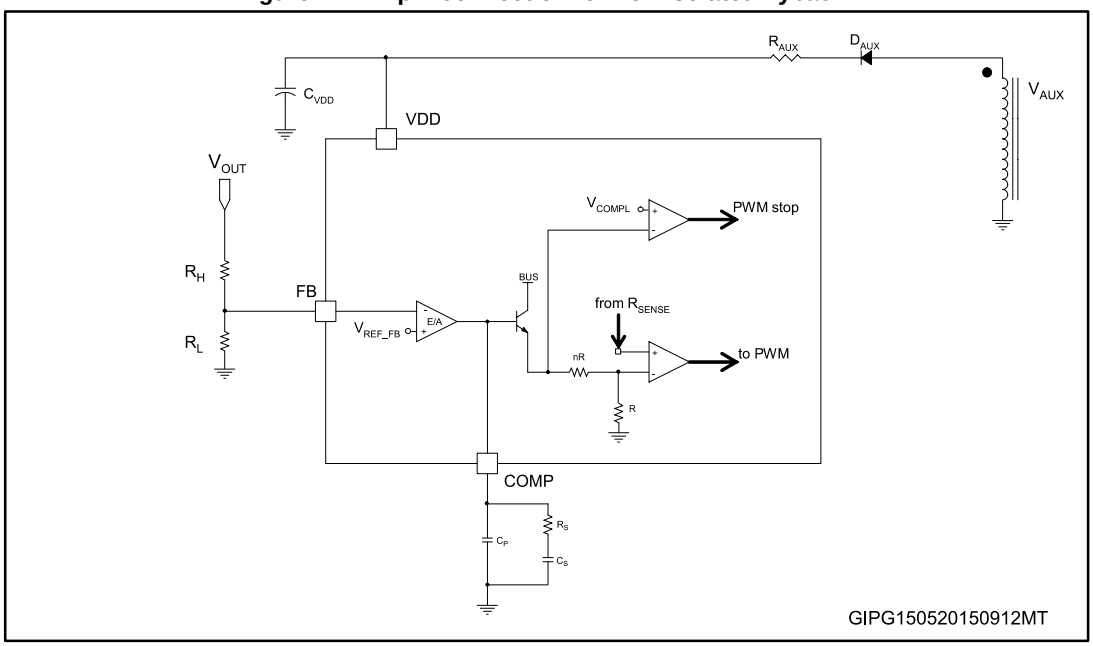
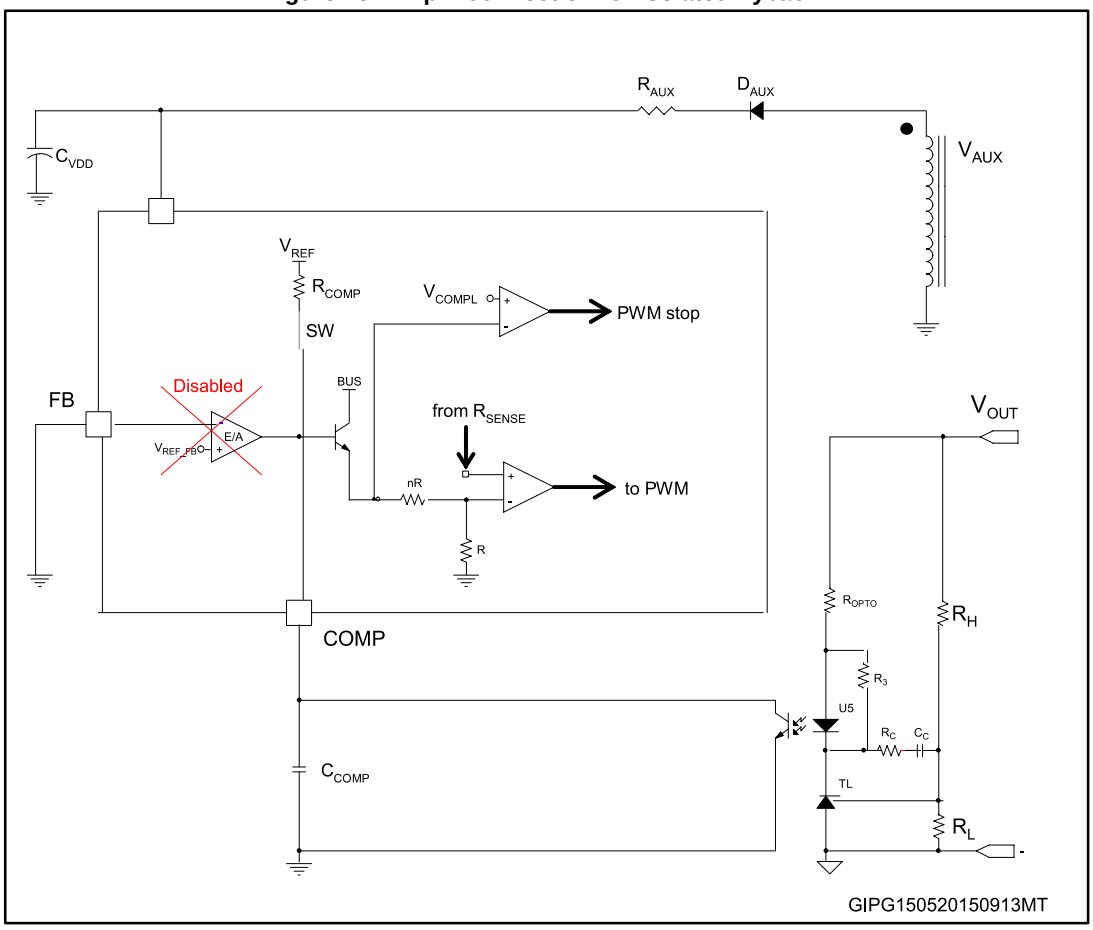


Figure 28: FB pin connection for isolated flyback



16 Layout guidelines and design recommendations

A proper printed circuit board layout is essential for correct operation of any switch-mode converter and this is true for the VIPerA16 as well. Also some trick can be used to make the design rugged versus external influences.

Careful component placing, correct traces routing, appropriate traces widths and compliance with isolation distances are the major issues.

The main reasons to have a proper PCB routing are:

- Provide a noise free path for the signal ground and for the internal references, ensuring good immunity against switching noises
- Minimize the pulsed loops (both primary and secondary) to reduce the electromagnetic interferences, both radiated and conducted and passing more easily the EMC regulations.

The below list can be used as guideline when designing a SMPS using VIPerA16.

- Signal ground routing should be routed separately from power ground and, in general, from any pulsed high current loop;
- Connect all the signal ground traces to the power ground, using a single "star point", placed close to the IC GND pin;
- With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VDD capacitor on the auxiliary return and then to the main GND using a single track;
- The compensation network should be connected as close as possible to the COMP pin, maintaining the trace for the GND as short as possible;
- A small bypass capacitor (a few hundreds pF up to 0.1 µF) to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor should be used, placed as close as possible to the VDD pin;
- When using SO16N package it is recommended to connect the pin 4 to GND pin, using a signal track, in order to improve the noise immunity. This is highly recommended in case of high nosily environment;
- The IC thermal dissipation takes place through the drain pins. An adequate heat sink copper area has to be designed under the drain pins to improve the thermal dissipation;
- It is not recommended to place large copper areas on the GND pins.
- Minimize the area of the pulsed loops (primary, RCD and secondary loops), in order to reduce its parasitic self- inductance and the radiated electromagnetic field: this will greatly reduce the electromagnetic interferences produced by the power supply during the switching.

Figure 29: Suggested routing for converter: flyback case

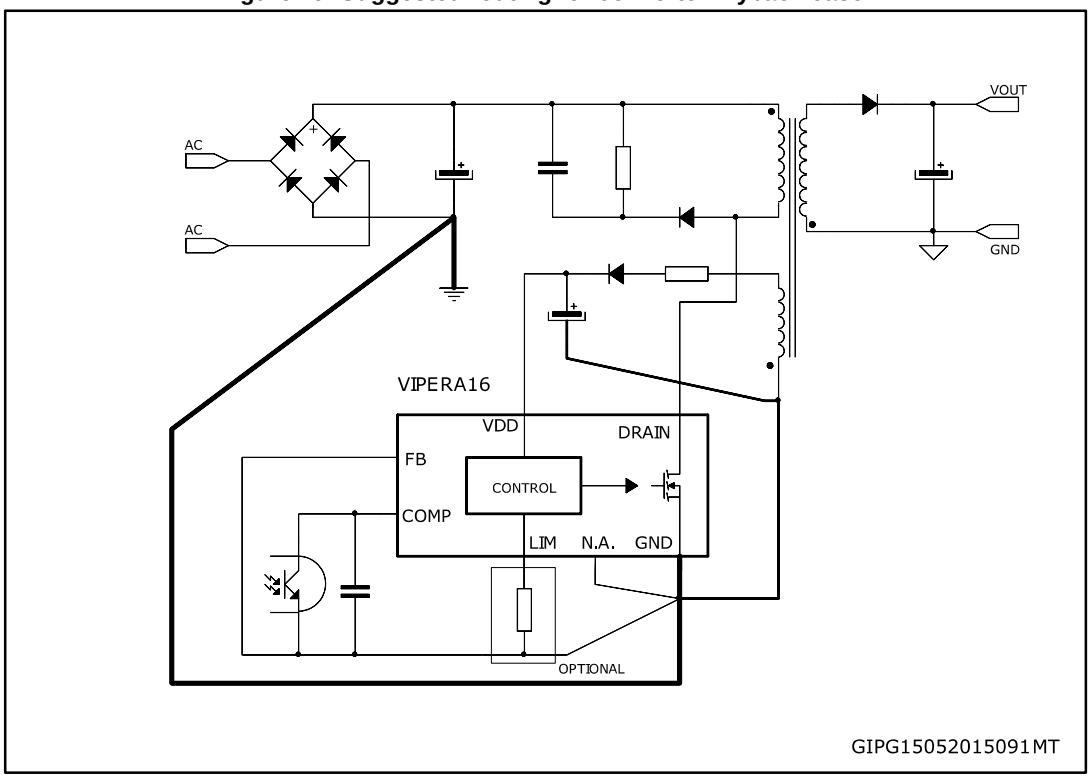
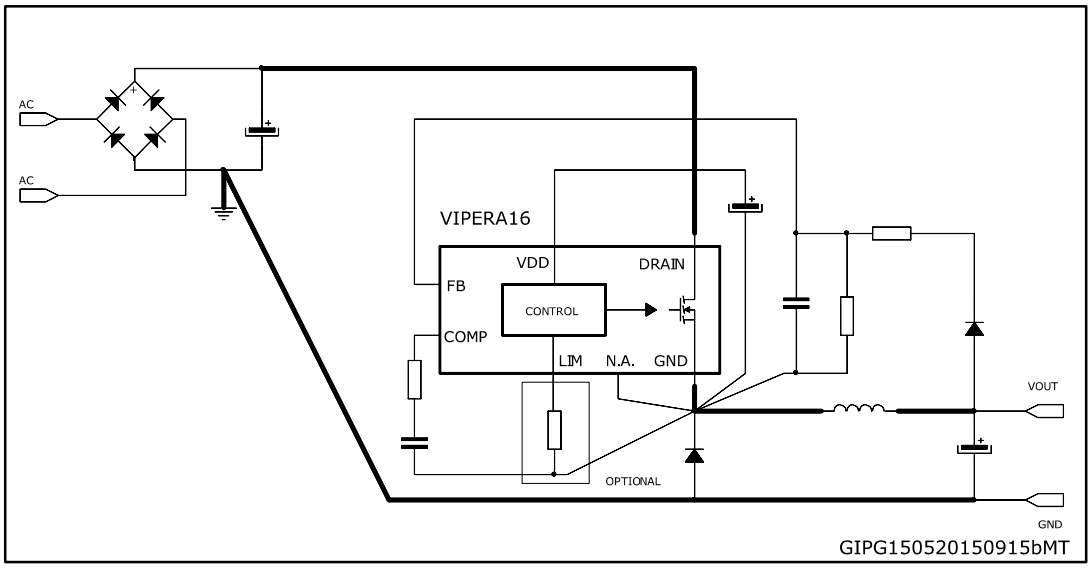


Figure 30: Suggested routing for converter: buck case



17 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

17.1 SO16 narrow package information

Figure 31: SO16 narrow package outline

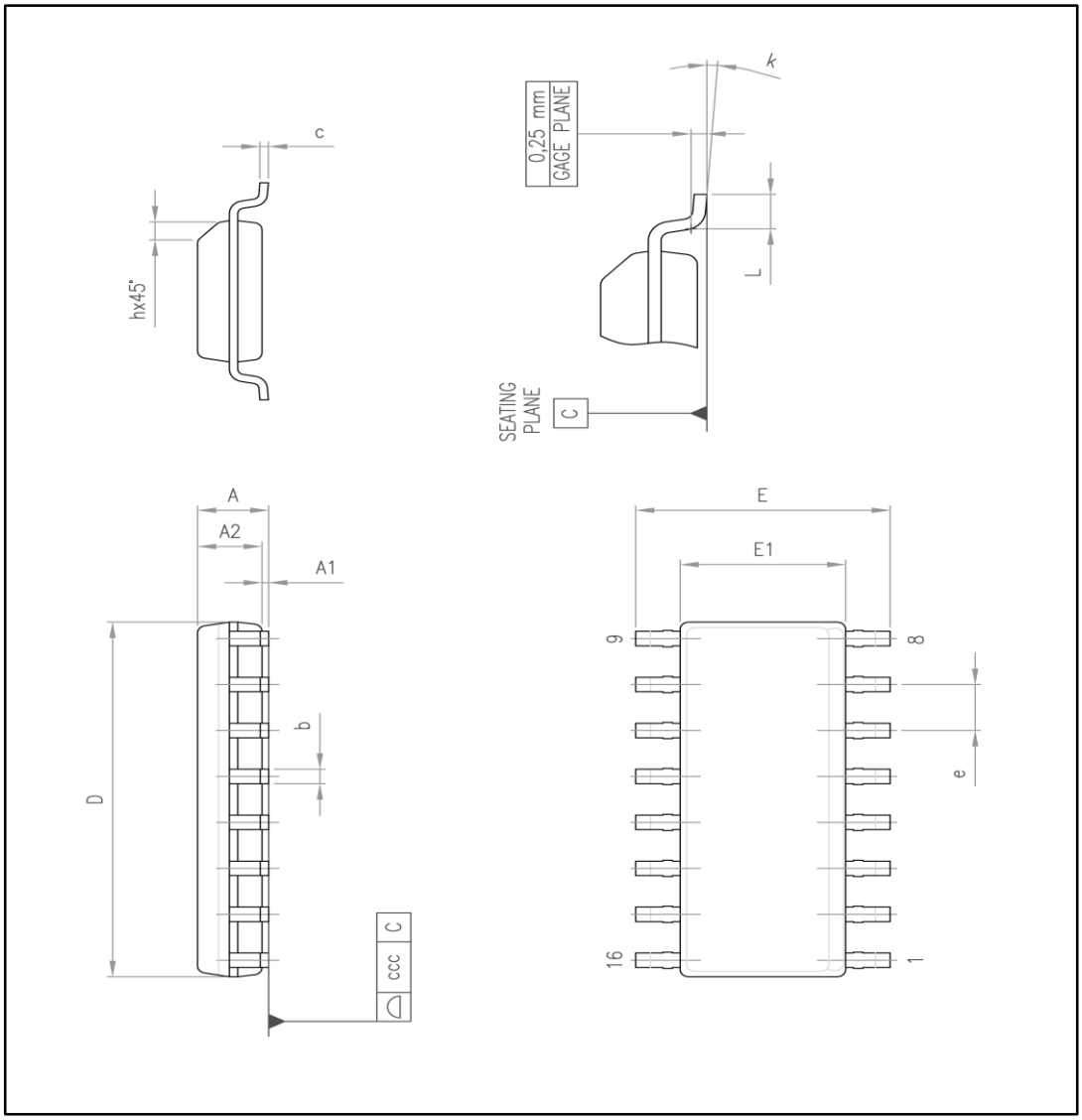


Table 9: SO16 narrow mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.1		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.8	9.9	10
E	5.8	6	6.2
E1	3.8	3.9	4
e		1.27	
h	0.25		0.5
L	0.4		1.27
k	0		8
ccc			0.1

18 Revision history

Table 10: Document revision history

Date	Revision	Changes
10-Jan-2012	1	Initial release.
11-Jul-2016	2	Modified features, applications and description in cover page. Updated *Table 3: "Pin description"*, *Table 5: "Thermal data"*, *Section 5: "Typical electrical characteristics"*, *Section 8: "High voltage current generator"* and *Figure 21: "Power-on and power-off"*. Added *Section 16: "Layout guidelines and design recommendations"*. Minor text changes.

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