

GENERAL DESCRIPTION

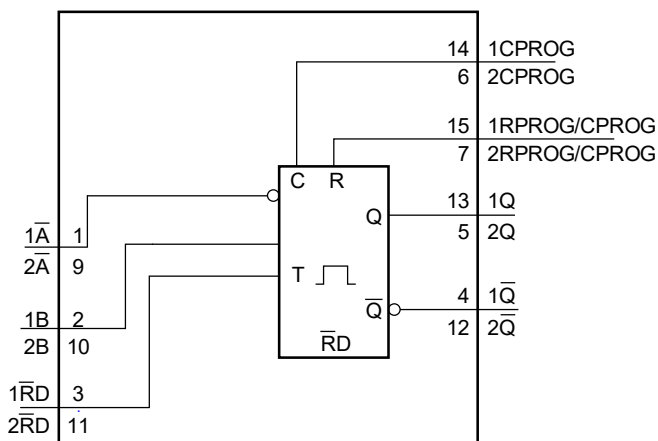
The 74AHC123 is a high-speed Si-gate CMOS device. It is a dual retriggerable monostable multivibrator.

The device has three ways of output pulse-duration control. First, when $\overline{nA}$ input sets low, the nB input goes high. Second, when nB input sets high, the $\overline{nA}$ input goes low. Third, when $\overline{nA}$ input sets low and nB input sets high, the $\overline{nRD}$ input goes high. Figure 3 shows the output pulse control using retrigger pulse and Figure 4 illustrates the output pulse control using reset input $\overline{nRD}$.

The output pulse-duration can be set through the selection of external resistance (R_{PROG}) and capacitance (C_{PROG}) values. All of the inputs have Schmitt-Trigger actions with sufficient hysteresis to handle slow input rise and fall times.

When started, the gated active low-going edge ($\overline{nA}$) input or the active high-going edge (nB) input can help to prolong the basic output pulse-duration. Through it, an ideal output pulse period ($nQ = \text{high}$, $\overline{nQ} = \text{low}$) can be achieved. Pulse duration can be reduced by a low-going edge on $\overline{nRD}$ input.

LOGIC DIAGRAM



FEATURES

- Supply Voltage Range: 2.0V to 5.5V
- Inputs Accept Voltages Higher than the Supply Voltage
- All Inputs with Schmitt-Trigger Actions
- Triggered from Gated Active High or Active Low Edge Inputs
- Retriggerable for Very Long Pulses
- Direct Reset Stops Output Pulse
- CMOS Level Inputs
- -40°C to +125°C Operating Temperature Range
- Available in Green SOIC-16 and TSSOP-16 Packages

FUNCTION TABLE

INPUT			OUTPUT	
$\overline{nRD}$	$\overline{nA}$	nB	nQ	$\overline{nQ}$
L	X	X	L	H
X	H	X	L*	H*
X	X	L	L*	H*
H	L	↑	⌊	⌋
H	↓	H	⌊	⌋
↑	L	H	⌊	⌋

H = High Voltage Level

L = Low Voltage Level

↑ = Low-to-High Transition

↓ = High-to-Low Transition

⌊ = One High-Level Output Pulse

⌋ = One Low-Level Output Pulse

X = Don't Care

* If the monostable multivibrator starts without this condition, the pulse will continue as set.

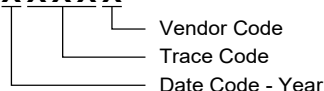
PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
74AHC123	SOIC-16	-40°C to +125°C	74AHC123XS16G/TR	74AHC123XS16 XXXXX	Tape and Reel, 2500
	TSSOP-16	-40°C to +125°C	74AHC123XTS16G/TR	74AHC123 XTS16 XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Supply Voltage Range, V_{CC}	-0.5V to 7V
Input Voltage Range, V_I	-0.5V to 7V
Input Clamp Current, $I_{IK}^{(2)}$ ($V_I < -0.5V$)	-20mA
Output Clamp Current, $I_{OK}^{(2)}$ ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$)	-20mA
Output Current, I_O ($V_O = -0.5V$ to $V_{CC} + 0.5V$)	$\pm 25mA$
Supply Current, I_{CC}	75mA
Ground Current, I_{GND}	-75mA
Junction Temperature ⁽³⁾	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	3000V
CDM	1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC}	2.0V to 5.5V
Input Voltage Range, V_I	0V to 5.5V
Output Voltage Range, V_O	0V to V_{CC}
Input Transition Rise or Fall Rate, $\Delta t/\Delta V$	
$V_{CC} = 3.3V \pm 0.3V$	100ns/V (MAX)
$V_{CC} = 5.0V \pm 0.5V$	20ns/V (MAX)
Operating Temperature Range	-40°C to +125°C

OVERSTRESS CAUTION

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.
2. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.
3. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

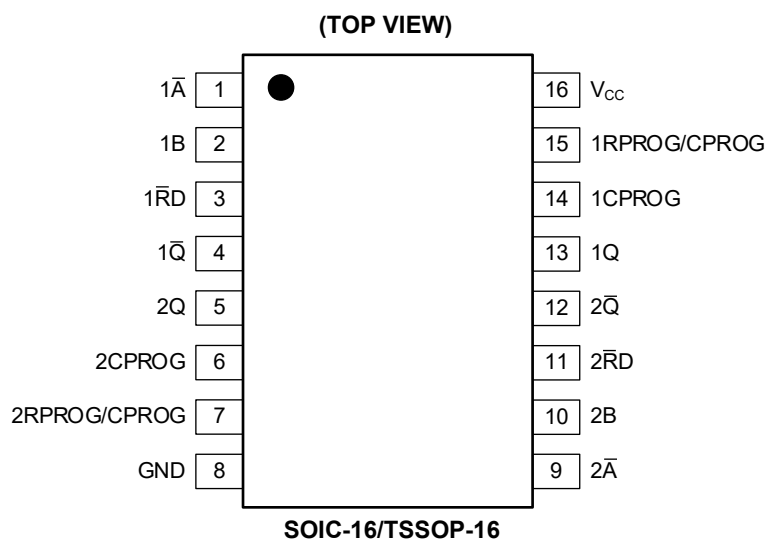
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	FUNCTION
1, 9	1 $\bar{A}$, 2 $\bar{A}$	Negative-Edge Triggered Inputs.
2, 10	1B, 2B	Positive-Edge Triggered Inputs.
3, 11	1 $\bar{R}D$, 2 $\bar{R}D$	Direct Reset Low and Positive-Edge Triggered Inputs.
4, 12	1 $\bar{Q}$, 2 $\bar{Q}$	Active Low Outputs.
13, 5	1Q, 2Q	Active High Outputs.
14, 6	1CPROG, 2CPROG	External Capacitor Connections.
15, 7	1RPROG/CPROG, 2RPROG/CPROG	External Resistor and Capacitor Connections.
8	GND	Ground.
16	V _{CC}	Supply Voltage.

ELECTRICAL CHARACTERISTICS

(Full = -40°C to +125°C, all typical values are measured at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP	MIN	TYP	MAX	UNITS
High-Level Input Voltage	V _{IH}	V _{CC} = 2.0V		Full	1.5			V
		V _{CC} = 3.0V		Full	2.1			
		V _{CC} = 5.5V		Full	3.85			
Low-Level Input Voltage	V _{IL}	V _{CC} = 2.0V		Full			0.5	V
		V _{CC} = 3.0V		Full			0.9	
		V _{CC} = 5.5V		Full			1.65	
High-Level Output Voltage	V _{OH}	V _I = V _{IH} or V _{IL}	I _O = -50μA, V _{CC} = 2.0V	+25°C	1.98	1.995		V
				Full	1.97			
			I _O = -50μA, V _{CC} = 3.0V	+25°C	2.98	2.995		
				Full	2.97			
			I _O = -50μA, V _{CC} = 4.5V	+25°C	4.48	4.495		
				Full	4.47			
			I _O = -4.0mA, V _{CC} = 3.0V	+25°C	2.75			
				Full	2.65			
I _O = -8.0mA, V _{CC} = 4.5V	+25°C	4.15						
	Full	4.05						
Low-Level Output Voltage	V _{OL}	V _I = V _{IH} or V _{IL}	I _O = 50μA, V _{CC} = 2.0V	+25°C		0.005	0.02	V
				Full			0.03	
			I _O = 50μA, V _{CC} = 3.0V	+25°C		0.005	0.02	
				Full			0.03	
			I _O = 50μA, V _{CC} = 4.5V	+25°C		0.005	0.02	
				Full			0.03	
			I _O = 4.0mA, V _{CC} = 3.0V	+25°C			0.25	
				Full			0.35	
I _O = 8.0mA, V _{CC} = 4.5V	+25°C			0.35				
	Full			0.45				
Input Leakage Current	I _I	V _{CC} = 0V to 5.5V, V _I = 5.5V or GND	nRPROG/CPROG ⁽¹⁾	+25°C		±0.05	±1	μA
				Full			±2	
			Pins n $\bar{A}$, nB and n $\bar{R}$ D	+25°C		±0.05	±1	
				Full			±2	
Supply Current	I _{CC}	V _{CC} = 5.5V, V _I = V _{CC} or GND, I _O = 0A		+25°C			1	μA
				Full			2	
		Active state (per circuit) ⁽¹⁾ , V _I = V _{CC} or GND	V _{CC} = 3.0V	+25°C		220	280	μA
				Full			350	
			V _{CC} = 4.5V	+25°C		300	500	
				Full			600	
		V _{CC} = 5.5V	+25°C		400	600		
Full				800				
Input Capacitance	C _I			+25°C		3.9		pF

NOTE:

1. Voltage on nRPROG/CPROG = 0.5 × V_{CC} and pin nRPROG/CPROG in off-state during test.

DYNAMIC CHARACTERISTICS

(See Figure 1 for test circuit. Full = -40°C to +125°C, all typical values are measured at $T_A = +25^\circ\text{C}$, $V_{CC} = 3.3\text{V}$ and $V_{CC} = 5.0\text{V}$ respectively, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				TEMP	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNITS
Propagation Delay ⁽²⁾	t _{PD}	n $\bar{A}$ and nB to nQ and n $\bar{Q}$, see Figure 2	V _{CC} = 3.0V to 3.6V	C _L = 15pF	Full	0.5	7.0	22.0	ns	
				C _L = 50pF	Full	0.5	9.0	26.0		
			V _{CC} = 4.5V to 5.5V	C _L = 15pF	Full	0.5	5.0	14.0		
				C _L = 50pF	Full	0.5	6.0	16.0		
		n $\bar{RD}$ to nQ and n $\bar{Q}$, see Figure 2	V _{CC} = 3.0V to 3.6V	C _L = 15pF	Full	0.5	8.0	23.0		
				C _L = 50pF	Full	0.5	9.0	28.0		
			V _{CC} = 4.5V to 5.5V	C _L = 15pF	Full	0.5	5.5	15.0		
				C _L = 50pF	Full	0.5	6.5	18.0		
		n $\bar{RD}$ to nQ and n $\bar{Q}$ (reset), see Figure 2	V _{CC} = 3.0V to 3.6V	C _L = 15pF	Full	0.5	7.0	17.5		
				C _L = 50pF	Full	0.5	8.0	21.5		
			V _{CC} = 4.5V to 5.5V	C _L = 15pF	Full	0.5	5.0	11.5		
				C _L = 50pF	Full	0.5	6.0	13.5		
Pulse Width ⁽³⁾	t _w	Inputs, n $\bar{A}$ = low, see Figure 2	V _{CC} = 3.0V to 3.6V		Full	5.0			ns	
			V _{CC} = 4.5V to 5.5V		Full	5.0				
		Inputs, nB = high, see Figure 2	V _{CC} = 3.0V to 3.6V		Full	5.0				
			V _{CC} = 4.5V to 5.5V		Full	5.0				
		Inputs, n $\bar{RD}$ = low, see Figure 2	V _{CC} = 3.0V to 3.6V		Full	5.0				
			V _{CC} = 4.5V to 5.5V		Full	5.0				
	t _w	Outputs, n $\bar{Q}$ = low and nQ = high, C _L = 50pF, see Figure 2, Figure 3, Figure 4 and Figure 5	V _{CC} = 3.0V to 3.6V	C _{PROG} = 28pF, R _{PROG} = 2k Ω	+25°C		200	240	ns	
					Full			300		
			V _{CC} = 4.5V to 5.5V		+25°C		180	220		
					Full			240		
			V _{CC} = 3.0V to 3.6V	C _{PROG} = 0.01 μ F, R _{PROG} = 10k Ω	+25°C	90	100	110	μ s	
					Full	85		115		
			V _{CC} = 4.5V to 5.5V		+25°C	90	100	110		
					Full	85		115		
			V _{CC} = 3.0V to 3.6V	C _{PROG} = 0.1 μ F, R _{PROG} = 10k Ω	+25°C	0.9	1	1.1	ms	
					Full	0.85		1.15		
			V _{CC} = 4.5V to 5.5V		+25°C	0.9	1	1.1		
					Full	0.85		1.15		
Retrigger Time	t _{RTRIG}	n $\bar{A}$ to nB, C _L = 50pF, see Figure 3 and Figure 5	V _{CC} = 3.0V to 3.6V	C _{PROG} = 100pF, R _{PROG} = 1k Ω	+25°C		60		ns	
			V _{CC} = 4.5V to 5.5V		+25°C		60			
			V _{CC} = 3.0V to 3.6V	C _{PROG} = 0.01 μ F, R _{PROG} = 1k Ω	+25°C		1		μ s	
			V _{CC} = 4.5V to 5.5V		+25°C		1			
Power Dissipation Capacitance ⁽⁴⁾	C _{PD}	C _L = 50pF, f _i = 1MHz, V _I = GND to V _{CC}				+25°C		98		pF
External Resistance	R _{PROG}	V _{CC} = 2.0V				+25°C	5			k Ω
		V _{CC} $\geq$ 3.0V				+25°C	1			
External Capacitance ⁽⁵⁾	C _{PROG}	V _{CC} = 2.0V				+25°C	-			pF
		V _{CC} $\geq$ 3.0V				+25°C	-			

NOTES:

1. Specified by design and characterization, not production tested.

2. t_{PD} is the same as t_{PLH} and t_{PHL} .

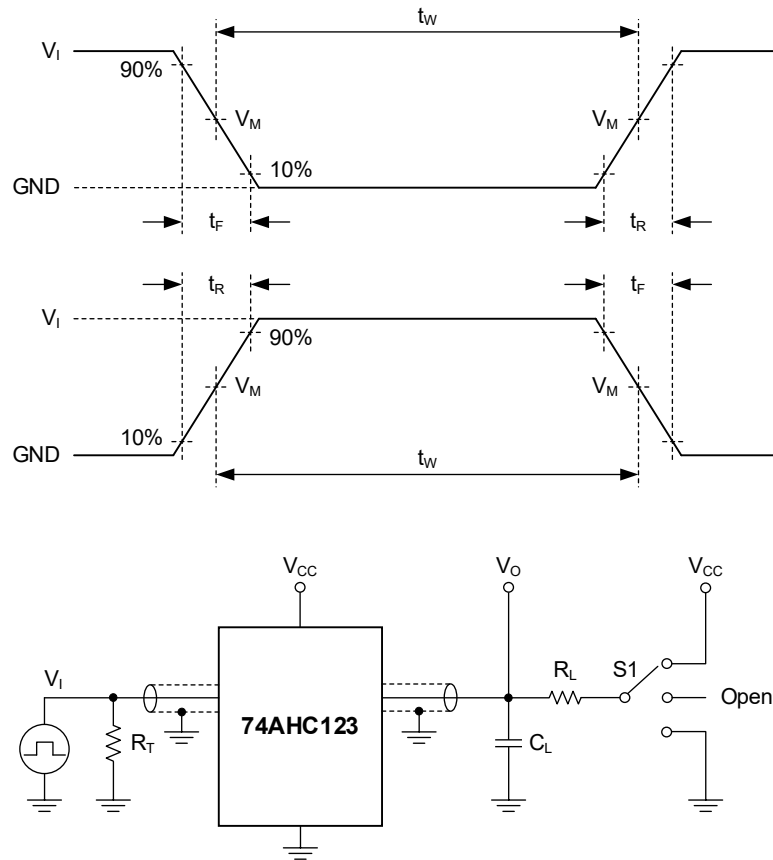
3. For $C_{PROG} \geq 10\text{nF}$, typical $t_W (\mu\text{s}) = C_{PROG} (\text{nF}) \times R_{PROG} (\text{k}\Omega)$.

4. C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$

where: f_i = Input frequency in MHz. f_o = Output frequency in MHz. C_L = Output load capacitance in pF. V_{CC} = Supply voltage in Volts. $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = Sum of outputs.

5. There is no limitation on C_{PROG} .

TEST CIRCUIT



Test conditions are given in Table 1.

Definitions for test circuit:

R_L : Load resistance.

C_L : Load capacitance (includes jig and probe).

R_T : Termination resistance (equals to output impedance Z_O of the pulse generator).

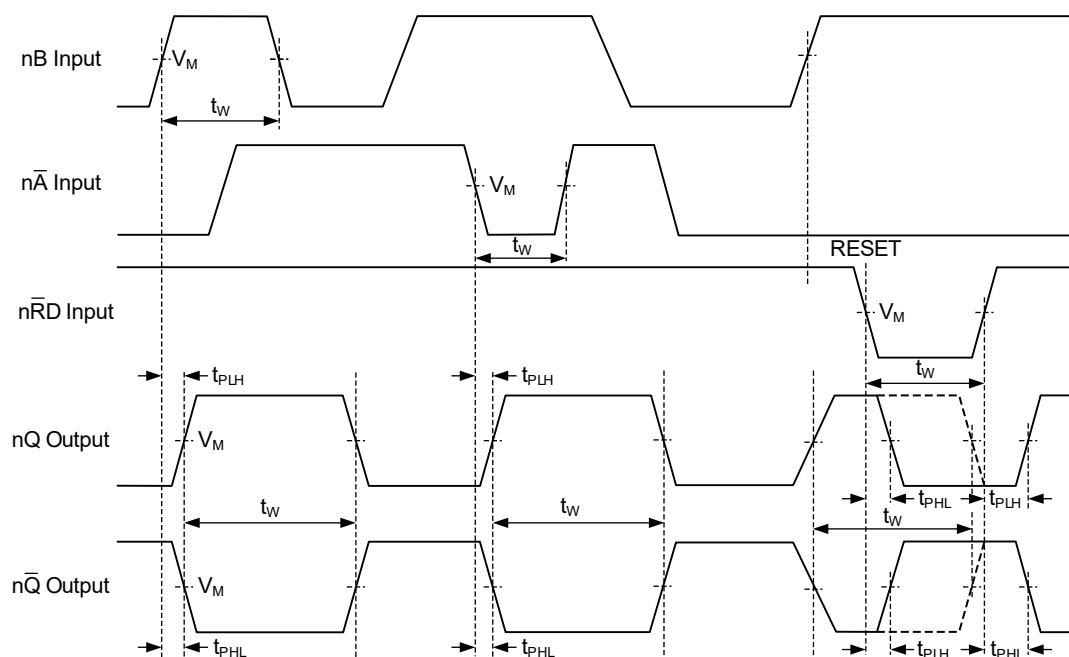
S1: Test selection switch.

Figure 1. Test Circuit for Measuring Switching Times

Table 1. Test Conditions

SUPPLY VOLTAGE	INPUT		LOAD		S1 POSITION		
V_{CC}	V_I	t_R, t_F	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.0V to 5.5V	V_{CC}	$\leq 3.0\text{ns}$	15pF, 50pF	1k Ω	Open	GND	V_{CC}

WAVEFORMS



Test conditions are given in Table 1.

Measurement points are given in Table 2.

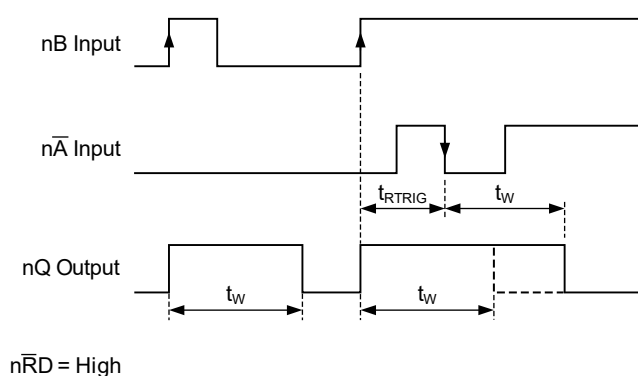
Figure 2. Pulse Width and Propagation Delay Times

Table 2. Measurement Points

SUPPLY VOLTAGE	INPUT	OUTPUT
V_{CC}	$V_M^{(1)}$	V_M
2.0V to 5.5V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

NOTE:

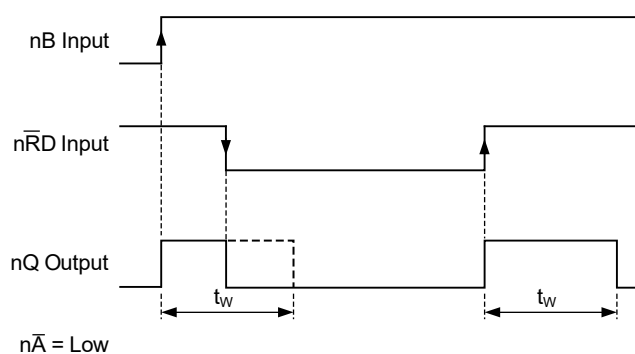
1. The measurement points should be V_{IH} or V_{IL} when the input rising or falling time exceeds 3.0ns.



Test conditions are given in Table 1.

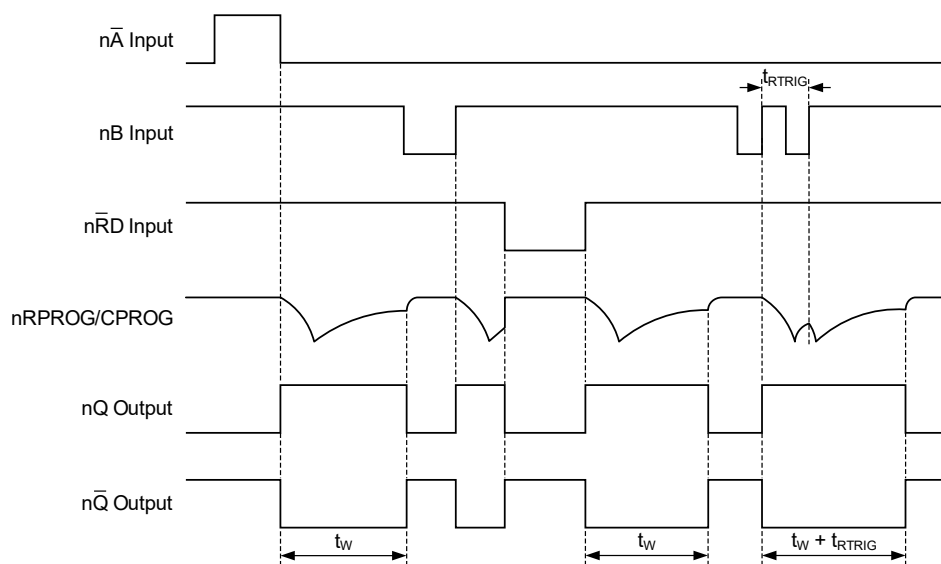
Figure 3. Output Pulse Control Using Retrigger Pulse

WAVEFORMS (continued)



Test conditions are given in Table 1.

Figure 4. Output Pulse Control Using Reset Input $\overline{nRD}$



Test conditions are given in Table 1.

Figure 5. Input and Output Timing

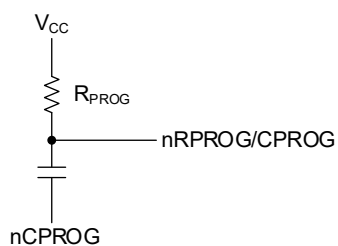


Figure 6. Timing Component Connections

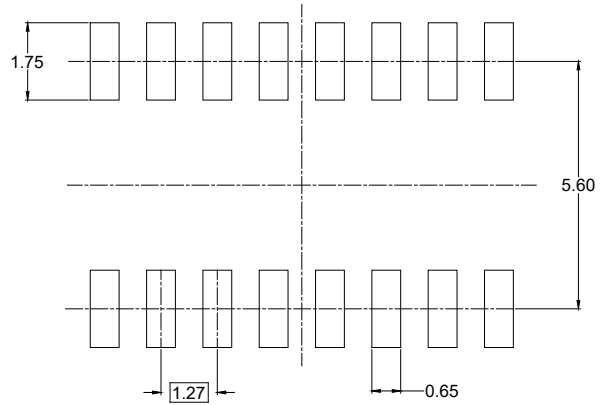
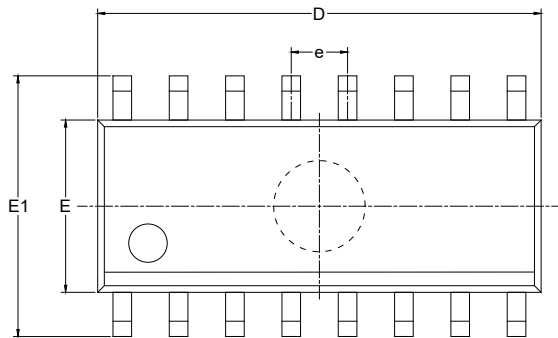
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

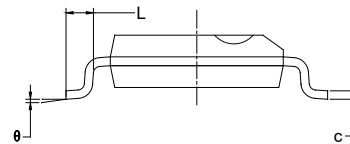
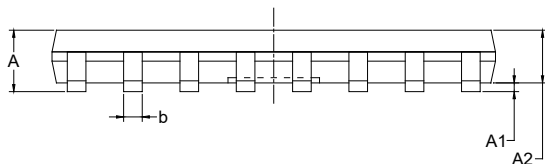
OCTOBER 2025 – REV.A.1 to REV.A.2	Page
Updated Electrical Characteristics section	4
SEPTEMBER 2022 – REV.A to REV.A.1	Page
Updated Electrical Characteristics section	4
Updated Dynamic Characteristics section.....	5
Added TSSOP-16 package.....	All
Changes from Original (JUNE 2021) to REV.A	Page
Changed from product preview to production data.....	All

PACKAGE OUTLINE DIMENSIONS

SOIC-16



RECOMMENDED LAND PATTERN (Unit: mm)



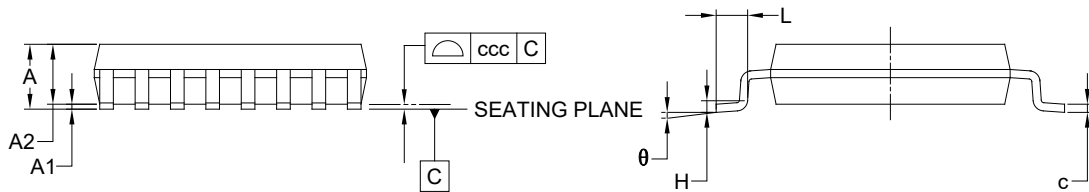
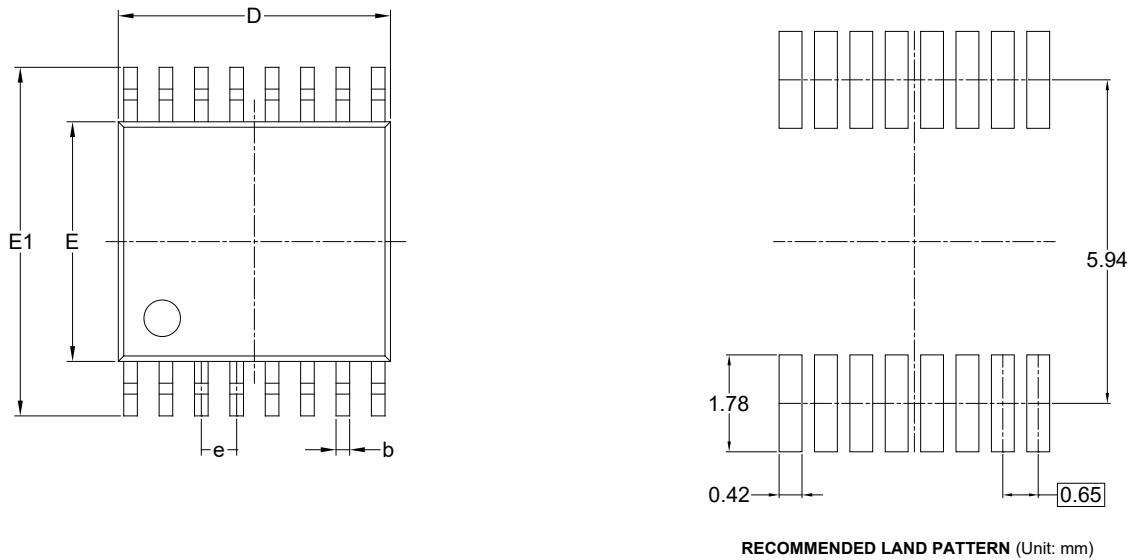
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.200
A1	0.050	-	0.150
A2	0.800	-	1.050
b	0.190	-	0.300
c	0.090	-	0.200
D	4.860	-	5.100
E	4.300	-	4.500
E1	6.200	-	6.600
e	0.650 BSC		
L	0.450	-	0.750
H	0.250 TYP		
θ	0°	-	8°
ccc	0.100		

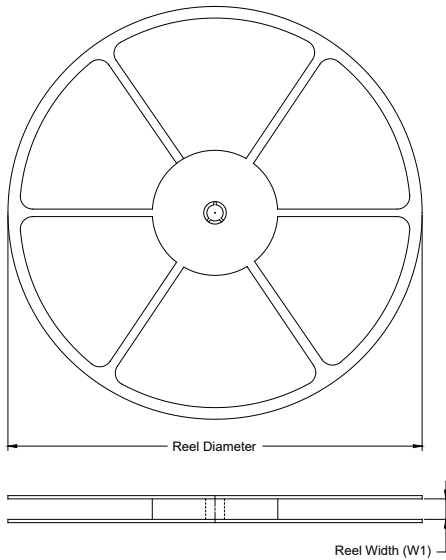
NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-153.

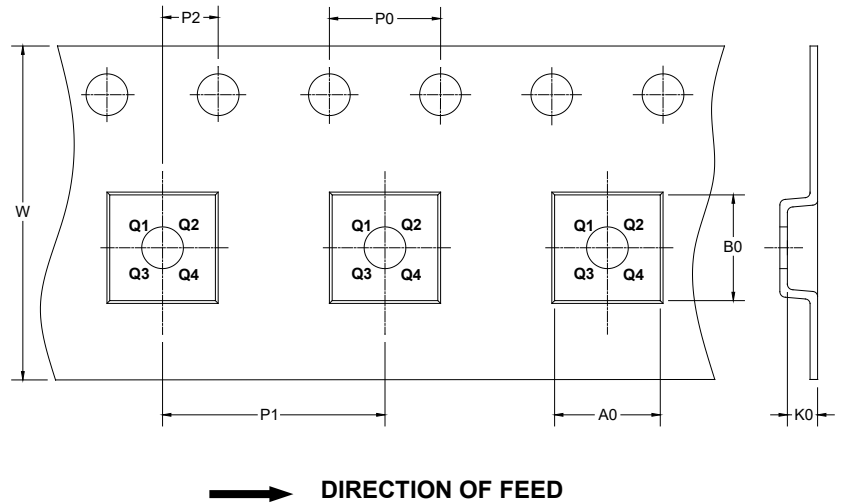
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

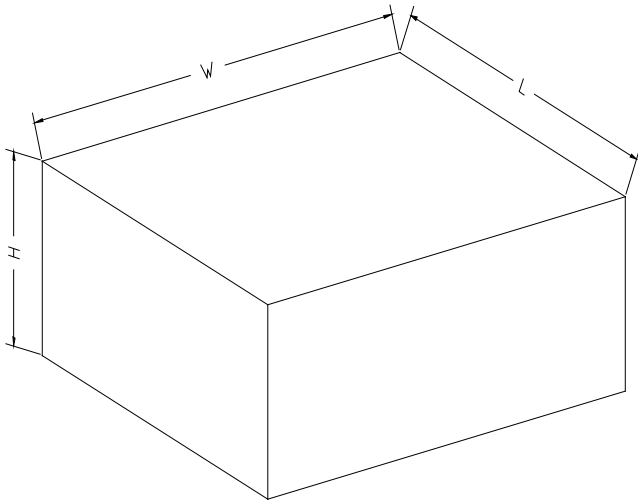
KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-16	13"	16.4	6.50	10.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-16	13"	12.4	6.90	5.60	1.50	4.0	8.0	2.0	12.0	Q1

DD00001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13"	386	280	370	5

DD0002