

PROTECTION PRODUCTS

Description

TClamp®2472S is specifically designed to provide secondary surge and ESD protection for Class-H VDSL2 line drivers. TClamp2472S integrates low capacitance, surge-rated steering diodes with a high power transient voltage suppressor (TVS). The TVS utilizes snap-back or “crow-bar” technology to minimize device clamping voltage and features high surge current capability of 20A ($t_p=8/20\mu s$).

TClamp2472S capacitance is limited to 3.5pF maximum with a typical capacitance variation of 0.10pF over the operating voltage range. This ensures correct signal transmission on VDSL lines. The biased bridge structure allows the device to be used in VDSL2 applications that utilize asymmetrical Class-H line drivers with operating voltages up to 24Vp-p.

TClamp2472S is in a 6-pin SOT-23 package. The leads are finished with lead-free matte tin. The flow-through package design simplifies PCB layout.

Features

- Transient Protection to
 - ♦ IEC 61000-4-2 (ESD) Level 4
 - ♦ IEC 61000-4-4 (EFT) 2kV (5/50ns)
 - ♦ IEC 61000-4-5 (Lightning) 20A (8/20 μs)
- Bias diodes prevent charging of TVS capacitance
- Working Voltage: 24V
- Low Capacitance: 3.5pF Maximum
- Capacitance variation <1.5pF (1V to 24V)
- Solid-State Silicon-Avalanche Technology

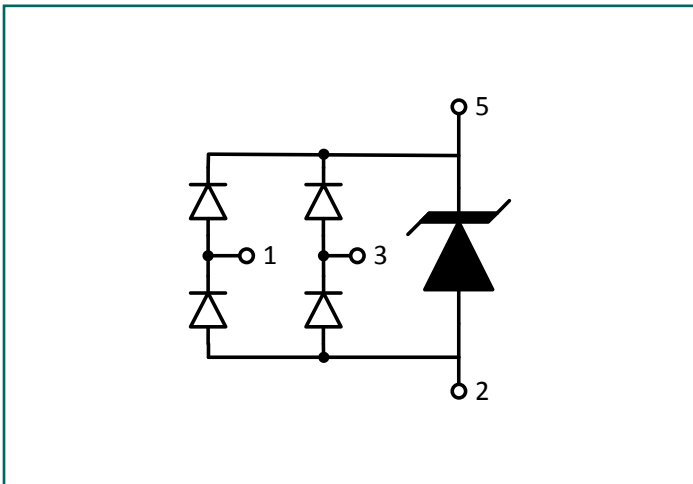
Mechanical Characteristics

- JEDEC SOT-23 6L package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Finish: matte Tin
- Molding Compound Flammability Rating: UL 94V-0
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

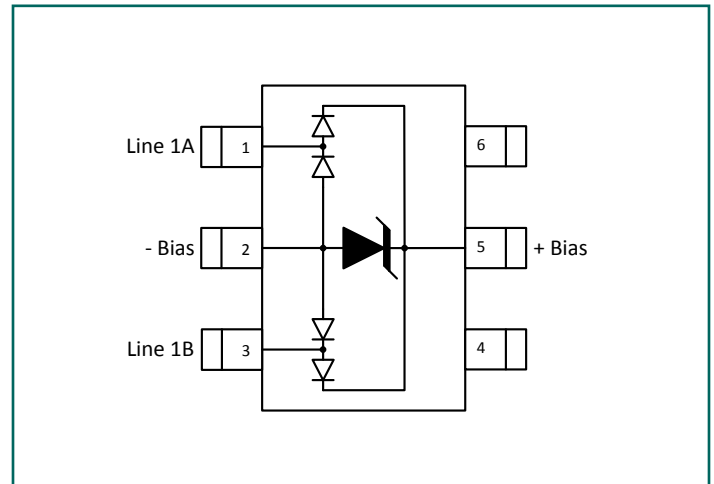
Applications

- ADSLx / VDSLx Secondary Protection
- VDSL2 Class-H Line Driver Secondary Protection
- Modems
- Access Equipment
- Central Office Equipment
- Customer Premise Equipment

Circuit Diagram



Pin Configuration



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 1.2/50µs)	P _{PK}	150	W
Peak Pulse Current (tp = 1.2/50µs)	I _{PP}	20	A
ESD per IEC 61000-4-2 (Contact) ^{(1), (3)}	V _{ESD}	±8	kV
Operating Temperature	T _J	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units	
Reverse Stand-Off Voltage	V _{RWM}	-40°C to 85°C Pin 1 to Pin 2, Pin 3 to Pin 2, Pin 1 to Pin 3			24	V	
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 10mA, T = -40°C to 85°C Pin 1 to Pin 3	27	31	35	V	
Reverse Leakage Current	I _R	V _{RWM} = 24V	T = 25°C		0.01	0.100	µA
			T = 85°C		0.02	0.100	µA
Holding Current ⁽³⁾	I _H		50	200		mA	
Clamping Voltage ^{(2), (3)}	V _C	I _{pp} = 10A, tp = 1.2/50µs, 8/20µs Combination Waveform Pin 1 to Pin 3		6		V	
		I _{pp} = 20A, tp = 1.2/50µs, 8/20µs Combination Waveform Pin 1 to Pin 3		7.5		V	
Breakover Voltage ⁽³⁾	V _{BO}	I _{BO} = 50mA Pin 1 to Pin 3		35		V	
Junction Capacitance	C _J	V _R = 0V, f = 1MHz Pin 1 to 2 or Pin 3 to Pin 2	T = 25°C		2	3.5	pF
		V _R = 0V, f = 1MHz Pin 1 to Pin 3			1.2	2	pF
Variation in Junction Capacitance ⁽³⁾	ΔC _J	V _R = 1V - 24V, f = 1MHz Pin 1 to Pin 3		0.1	1.5	pF	

Notes:

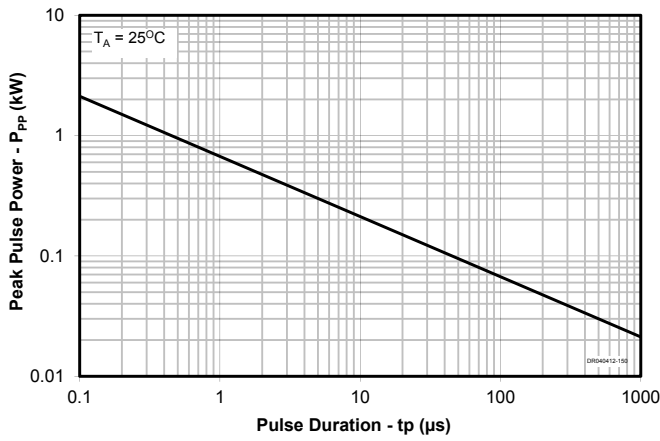
(1): ESD Gun return path to Ground Reference Plane (GRP)

(2): Measured using a 1.2/50µs voltage, 8/20µs current combination waveform, RS = 8 Ohms. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.

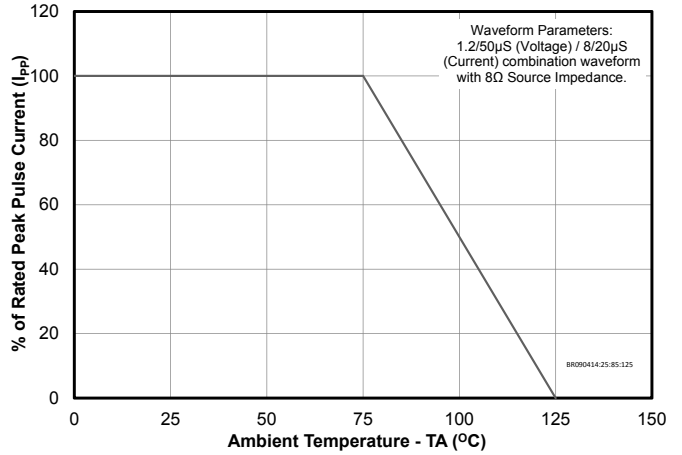
(3): Guaranteed by design. Not production tested

Typical Characteristics

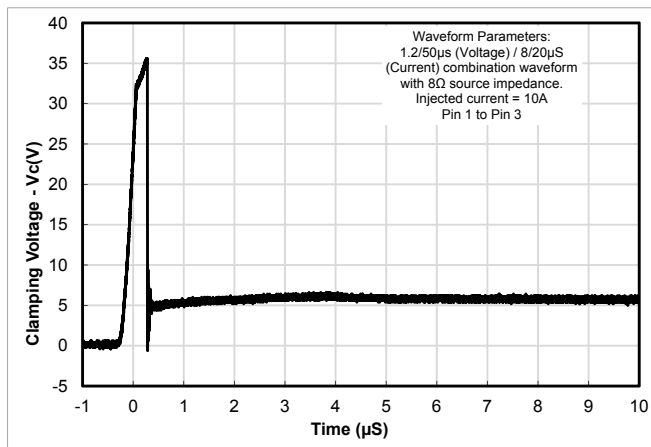
Non-Repetitive Peak Pulse Power vs. Pulse Time



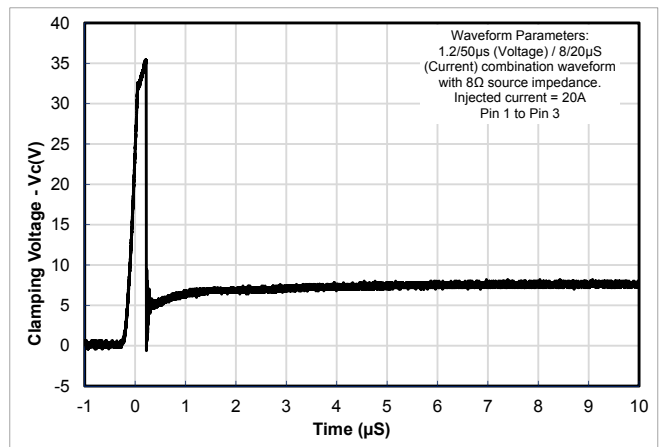
Power Derating Curve



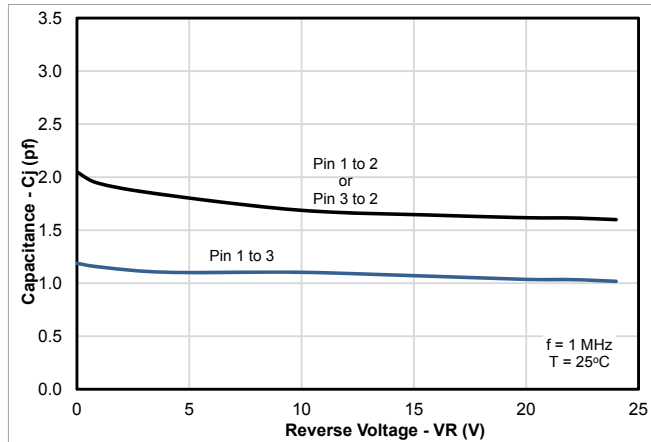
Clamping Characteristic (10A, Combination Waveform)



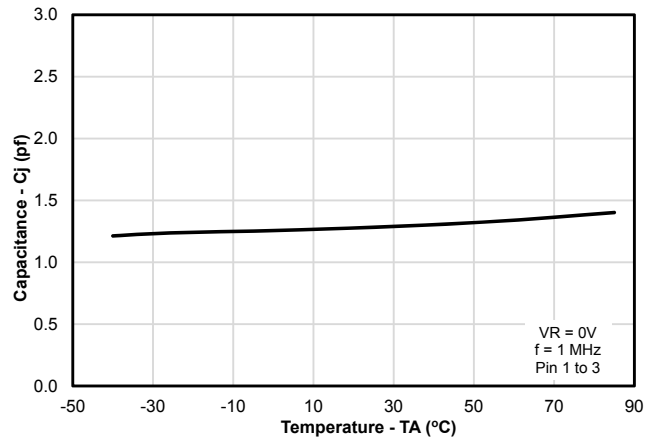
Clamping Characteristic (20A, Combination Waveform)



Capacitance vs. Reverse Voltage

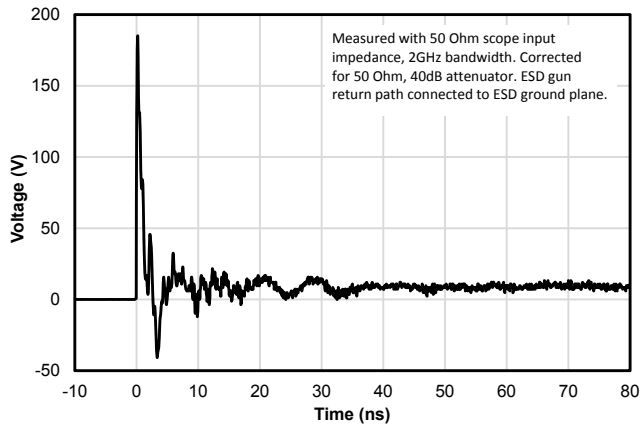


Capacitance vs. Temperature

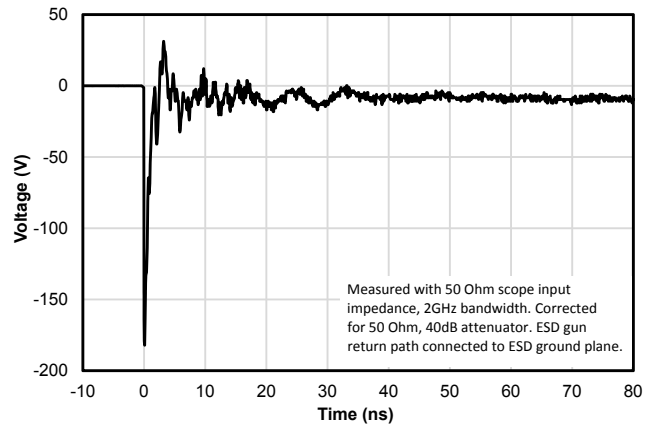


Typical Characteristics

ESD Clamping (+8kV Contact per IEC 61000-4-2), Pin 1 to 3



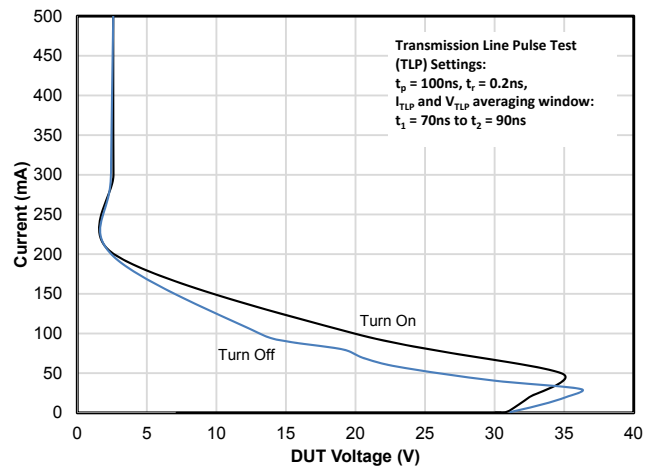
ESD Clamping (-8kV Contact per IEC 61000-4-2), Pin 1 to 3



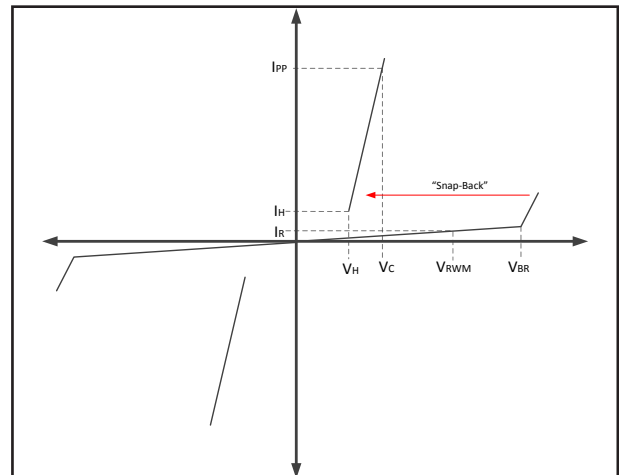
Device Operation

This device utilizes a multi-junction structure that is designed to switch to a low voltage state when triggered by ESD, EOS, or other transient events. During normal operation, the device will present a high-impedance to the circuit for voltage up to the working voltage (V_{RWM}) of the device. When the voltage across the device terminals exceeds the breakdown voltage (V_{BR}), avalanche breakdown occurs in the blocking junction causing the device to “snap-back” or switch to a low impedance on-state. This has the advantage of lowering the overall clamping voltage (V_C) as ESD peak pulse current (I_{PP}) flows through the device. Once the current decreases below the holding current (I_H), the device will return to a high-impedance off-state.

Typical Low Current IV Characteristic



Characteristic Curve



Symbol	Parameter
V_{RWM}	Maximum Working Voltage
V_{BR}	Breakdown Voltage
V_C	Clamping Voltage
I_H	Holding Current
I_R	Reverse Leakage Current
I_{PP}	Peak Pulse Current

Applications Information

VDSL Protection Design

TClamp2472S is designed to protect VDSL interfaces from transient over-voltages which result from lightning and ESD. An example of how to implement the TClamp2472S for secondary (line driver side) protection is shown in Figure 1 below. When connected as shown, it will limit the differential voltage across the driver inputs during ESD and high current surge events. Pins 1 and 3 of the device are connected directly to the transmit and receive lines. Steering diodes at these pins route the surge current through the internal transient voltage suppressor (TVS). Pins 2 and 5 are connected

to the voltage supply lines via resistors R1 and R2. This connection serves to limit capacitance fluctuation of the TVS. The resistors should be large enough value as to minimize leakage current (typically 1 Meg Ohm). For single supply applications, only one resistor (R1) would be needed. Depending on immunity requirements, A primary protection device, such as a gas discharge tube (GDT), may be required to limit the voltage (and thus current) delivered to the line side of the transformer. Series resistors (RS) with a value of 1 - 2 Ohms may be needed to reduce current flow into the driver IC.

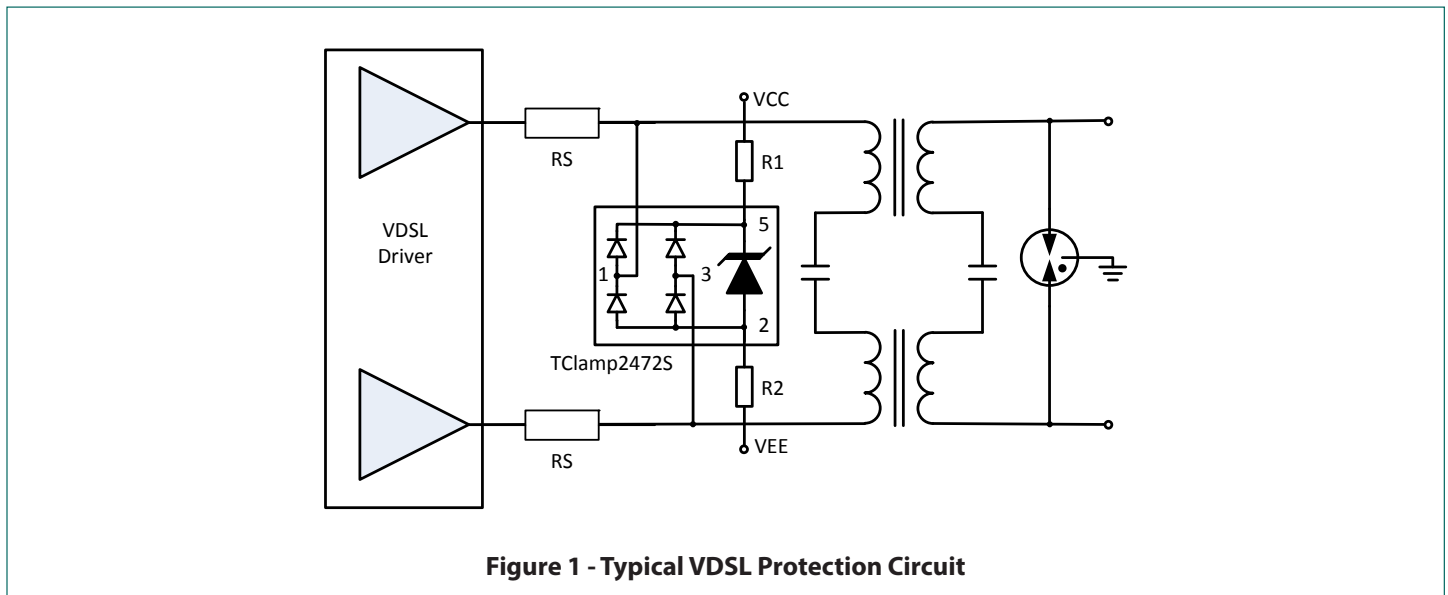


Figure 1 - Typical VDSL Protection Circuit

Device Connection and PCB Routing

The flow-through design of TClamp2472S simplifies board layout and PCB trace routing. Figure 2 shows an example of how to connect the differential lines and bias voltages to the device. Line 1A is connected at pin1 and its trace can continue under the part and connect to pin 6, which is not connected internally to the part. A similar connection can be made for Line 1B. This layout makes it easy to keep the differential signal traces symmetrical. Bias voltage should be applied at pins 5 (positive polarity voltage) and 2 (negative polarity voltage). For single supply applications, Pin 2 can be connected to ground.

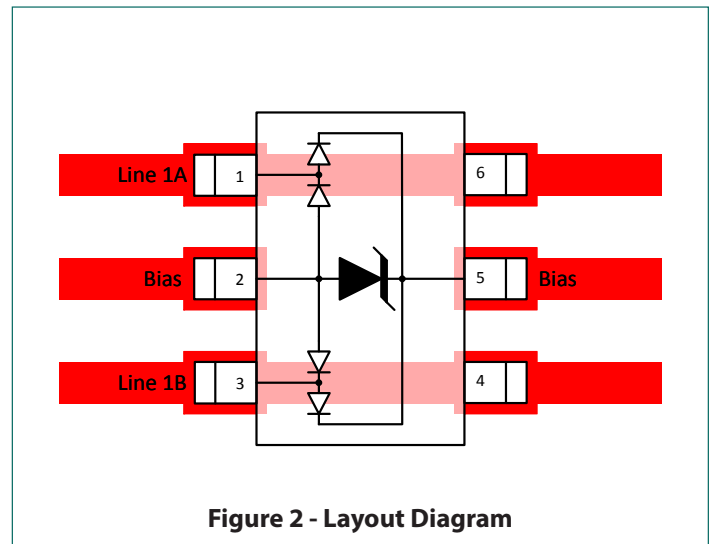
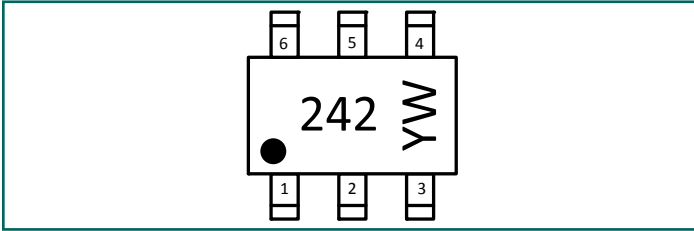


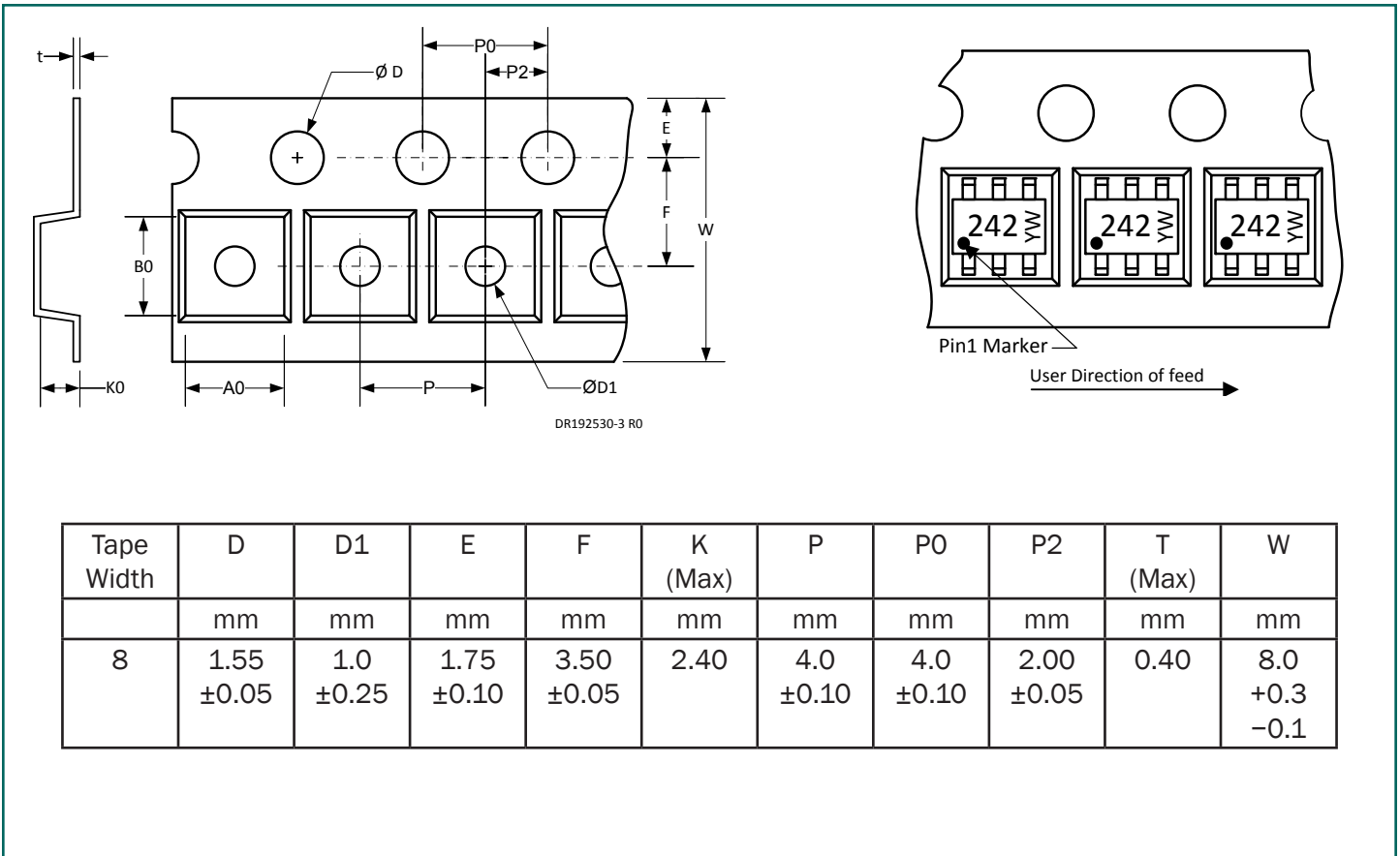
Figure 2 - Layout Diagram

Marking Code



Notes: YW = Alphanumeric character Date Code

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
TClamp2472S.TCT	3000	7 Inch

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