Clock OSC

SG-210SCBA

Product name SG-210SCBA 12.288000 MHz L Conforms to AEC-Q200

Product Number / Ordering code X1G004591A078xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 15 mg

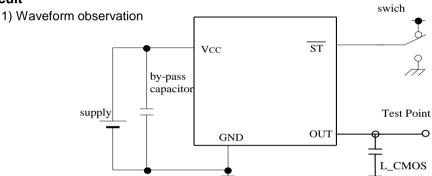
1.Absolute maximum ratings									
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks			
Maximum supply voltage	Vcc-GND	-0.3	-	+5	V	-			
Storage temperature	T_stg	-40	-	+125	°C	Storage as single product			
Input voltage	Vin	-0.3	-	Vcc+0.3	V	ST terminal			

2.Specifications(characteri	stics)					
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Output frequency	f0		12.288000		MHz	
Supply voltage	Vcc	2.7	3.3	3.6	V	-
Operating temperature	T_use	-40	-	+85	°C	-
Frequency tolerance	f_tol	-50	-	50	x10 ⁻⁶	T_use
Current consumption	Icc	-	-	3	mA	No load condition
Stand-by current	I_std	-	-	1.0	μA	ST = GND
Symmetry	SYM	45	-	55	%	50% Vcc Level L_CMOS=<15pF
Output voltage	V _{OH}	0.9Vcc	-	-		IOH=-1mA
	V _{OL}	-	-	0.1Vcc		IOL=1mA
Output load condition	L_CMOS	-	-	15	рF	CMOS Load
Input voltage	V_{IH}	0.8Vcc	-	•		ST terminal
	V_{IL}	-	-	0.2Vcc		ST terminal
Rise time	t _r	-	-	3	ns	0.2Vcc to 0.8Vcc Level, L_CMOS=15pF
Fall time	tf	-	-	3	ns	0.2Vcc to 0.8Vcc Level, L_CMOS=15pF
Start-up time	t_str	-	-	3	ms	t = 0 at 0.9Vcc
Jitter	t _{DJ}	-	3.4	-	ps	Deterministic Jitter, Vcc = 3.3 V
	t _{RJ}	-	2.3	ı	ps	Random Jitter, Vcc = 3.3 V
	t _{RMS}	-	1.7	-	ps	$\sigma(RMS \text{ of total distribution}), Vcc = 3.3 V$
	t _{p-p}	-	16.4	•	ps	Peak to Peak, Vcc = 3.3 V
	t _{acc}	-	1.8	-	ps	Accumulated Jitter(σ), n = 2 to 50 000 cycles
Phase jitter	t _{PJ}	-	0.27	-	ps	Offset Frequency: 12 kHz to 5 MHz, Vcc = 3.3 V
Phase noise	L(f)	-	-	-	dBc/Hz	-
		-	-109.8	-	dBc/Hz	Offset 10 Hz, Vcc=3.3 V
		-	-134.6	-	dBc/Hz	Offset 100 Hz, Vcc = 3.3 V
		-	-146	-	dBc/Hz	Offset 1 kHz, Vcc = 3.3 V
		-	-153.1	-	dBc/Hz	Offset 10 kHz, Vcc = 3.3 V
		-	-158.7	-	dBc/Hz	Offset 100 kHz, Vcc = 3.3 V
		-	-164	•	dBc/Hz	Offset 1 MHz, Vcc = 3.3 V
Frequency aging	f_age	-3	-	3	x10 ⁻⁶	@+25°C first year
		-	-	-		-

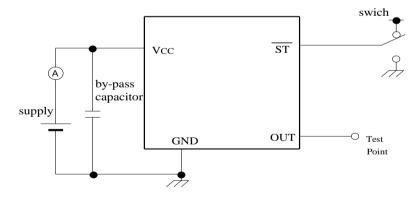
3.Timing chart

VCC 80 %VCC 20 %VCC GND

4.Test circuit

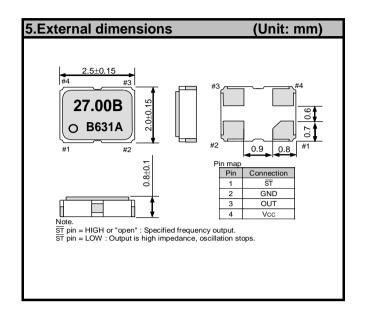


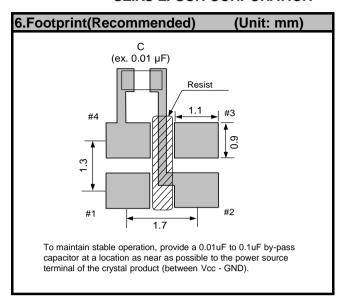
2) Current consumption

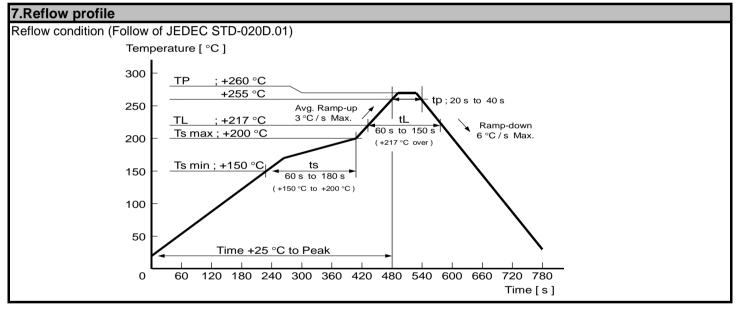


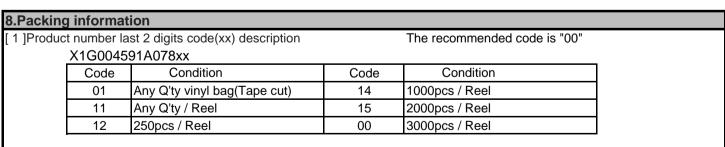
*Current consumption under the disable function should be = GND.

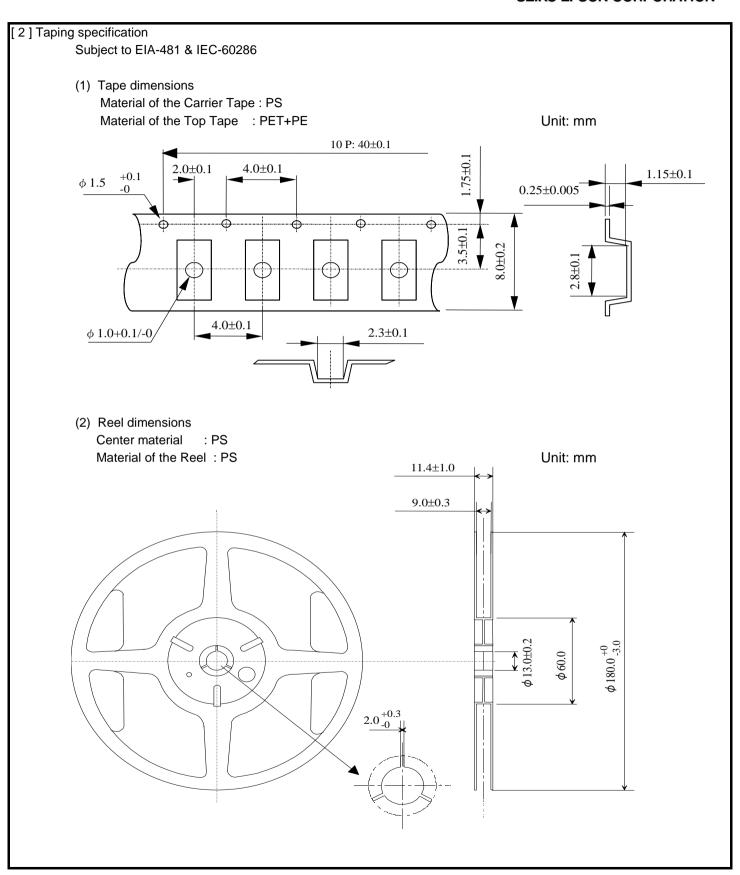
- 3) Condition
- (1) Oscilloscope
- · Band width should be minimum 5 times higher (wider) than measurement frequency.
- · Probe earth should be placed closely from test point and lead length should be as short as possible
- * Recommendable to use miniature socket. (Don't use earth lead.)
- (2) L_CMOS also includes probe capacitance.
- (3) By-pass capacitor (0.01 μF to 0.1 $\mu F)$ is placed closely between VCC and GND.
- (4) Use the current meter whose internal impedance value is small.
- (5) Power supply
- · Start up time (0 %VCC to 90 %VCC) of power source should be more than 150 µs.
- · Impedance of power supply should be as lowest as possible.











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