

Programmable Clock OSC

SG-8018CA

SEIKO EPSON CORPORATION

Product name SG-8018CA 20.000000 MHz TJHPA

Product Number / Ordering code X1G0055710013xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 143 mg

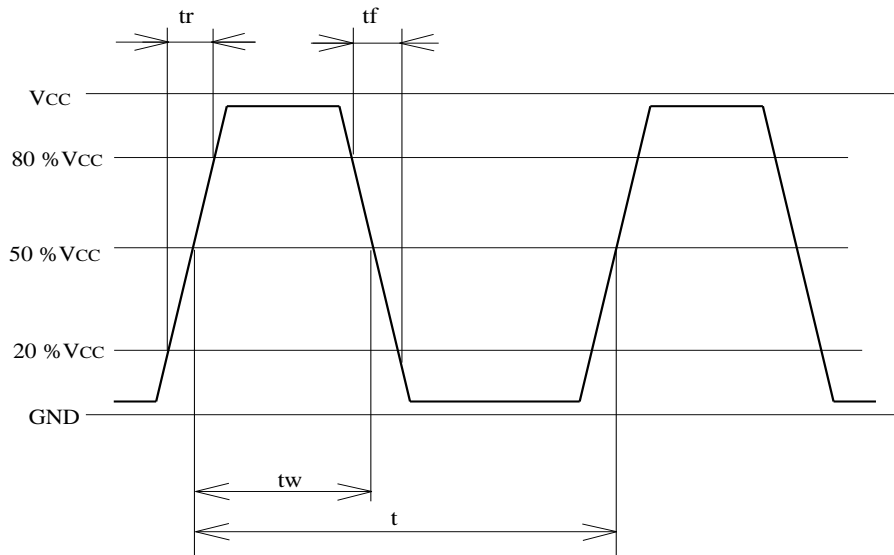
1. Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+4.0	V	-
Storage temperature	T_stg	-40	-	+125	°C	Stored as bare product after unpacking
Input voltage	Vin	GND-0.5	-	Vcc+0.3	V	ST or OE terminal

2. Specifications(characteristics)

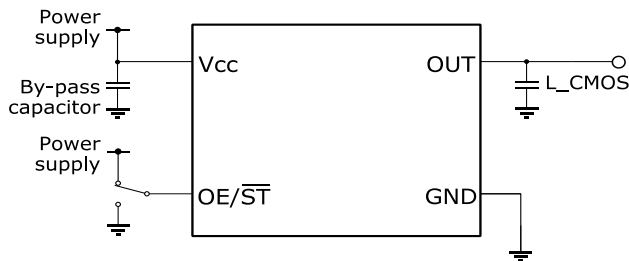
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0		20.000000		MHz	
Supply voltage	Vcc	1.62	-	3.63	V	Typ. 1.8V / 2.5V / 3.3V
Operating temperature	T_use	-40	-	+105	°C	-
Frequency tolerance	f_tol	-50	-	+50	x10 ⁻⁶	T_use : -40 to +105°C
Current consumption	Icc	-	-	3.5	mA	Vcc=3.3V Typ., No load
Stand-by current	I_std	-	-	-	µA	-
Disable current	I_dis	-	-	3.5	mA	Vcc=3.3V Typ., OE=GND
Symmetry	SYM	45	-	55	%	50%Vcc, L_CMOS=<15pF
Output voltage	V _{OH}	90%Vcc	-	-	V	-
	V _{OL}	-	-	10%Vcc	V	-
Output load condition	L_CMOS	-	-	15	pF	CMOS Load
Input voltage	V _{IH}	70%Vcc	-	-	V	OE Terminal
	V _{IL}	-	-	30%Vcc	V	OE Terminal
Rise time	t _r	-	-	6	ns	20% to 80%Vcc, L_CMOS=15pF
Fall time	t _f	-	-	6	ns	20% to 80%Vcc, L_CMOS=15pF
Disable time	t _{stp}	-	-	1	µs	Measured from the time OE or ST pin crosses 30%Vcc
Enable time	t _{sta}	-	-	1	µs	Measured from the time OE pin crosses 70%Vcc
Resum time	t _{res}	-	-	-	ms	-
Start-up time	t _{str}	-	-	3	ms	Measured from the time Vcc reaches its rated minimum value, 1.62V
Frequency aging	f_age	-	-	-	x10 ⁻⁶ /Year	Included in Frequency tolerance 10 years

3. Timing chart

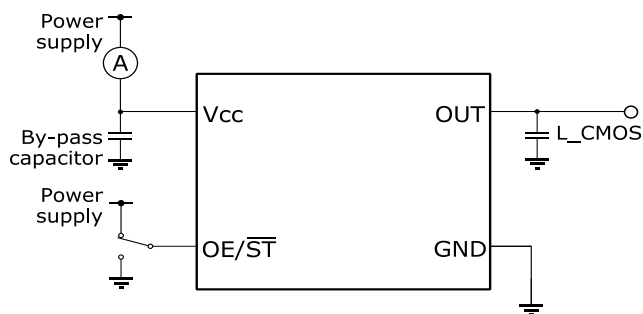


4. Test circuit

1) Waveform observation



2) Current consumption



* Current consumption under the disable function should be OE = GND
 Current consumption under the standby function should be ST = GND.

3) Measurement conditions

- (1) L_CMOS includes probe capacitance.
- (2) Mount a by-pass capacitor (approx. 0.01 to 0.1 μ F) near the mains terminals of the oscillator (between Vcc and GND)

5.External dimensions (Unit: mm)

Top view dimensions: 7.0±0.2 (width), 5.0±0.2 (height). Pin positions: #1, #2, #3, #4.

Side view dimensions: 1.3±0.1 (height).

Pin map table:

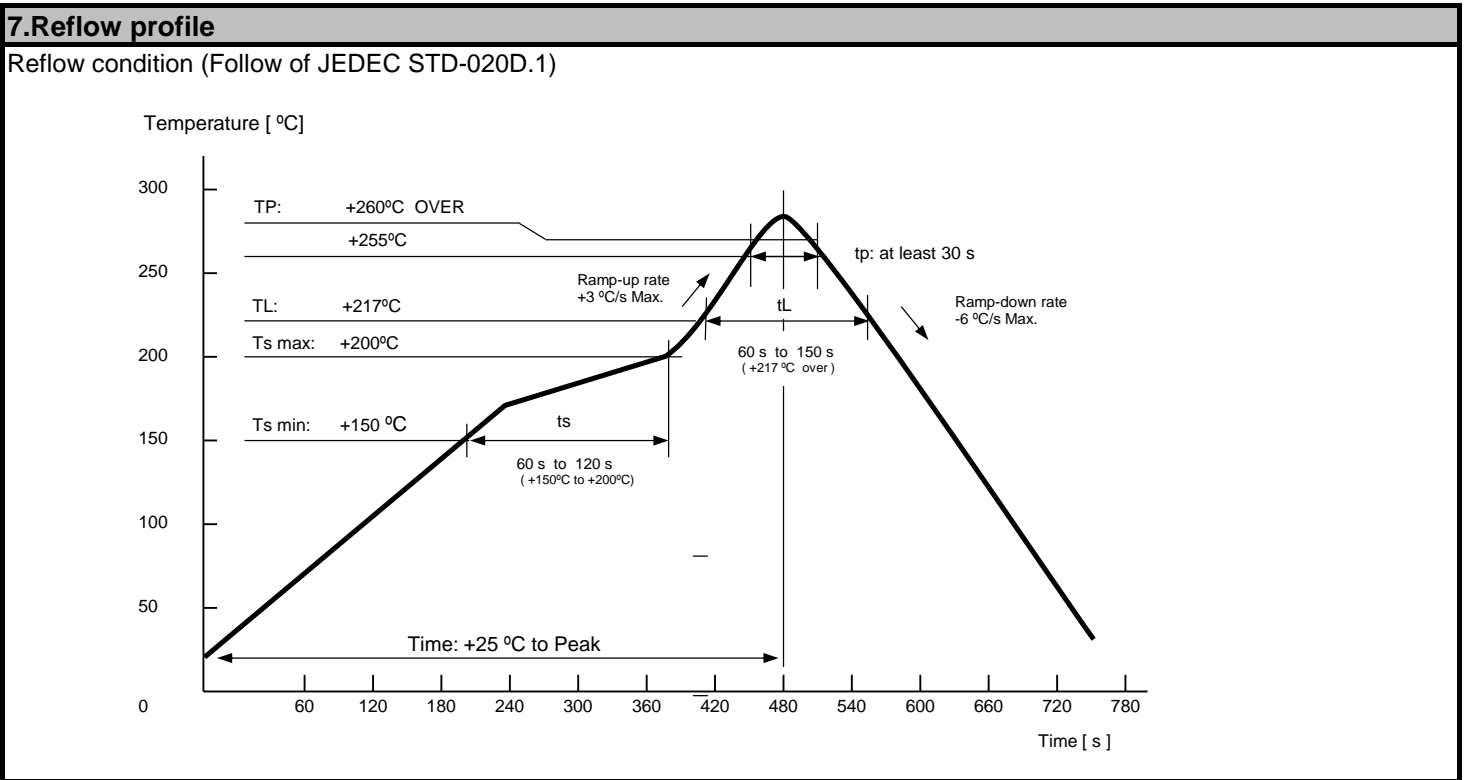
Pin	Connection
1	OE or \overline{ST}
2	GND
3	OUT
4	VCC

OE Pin = "H" : Specified frequency output.
 OE Pin = "L" : Output is low level (weak pull - down)
 ST Pin = "H" : Specified frequency output.
 ST Pin = "L" : Output is low level (weak pull - down), oscillation stops.

6.Footprint(Recommended) (Unit: mm)

Footprint dimensions: 5.08mm (width), 4.2mm (height). Pad dimensions: 1.8mm (width), 2.0mm (height).

In order to achieve optimum jitter performance, the 0.1 μ F capacitor between VCC and GND should be placed. It is also recommended that the capacitors are placed on the device side of the PCB, as close to the device as possible and connected together with short wiring pattern.



8.Packing information

[1] Product number last 2 digits code(xx) description The recommended code is "00"

X1G0055710013xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[2] Taping specification

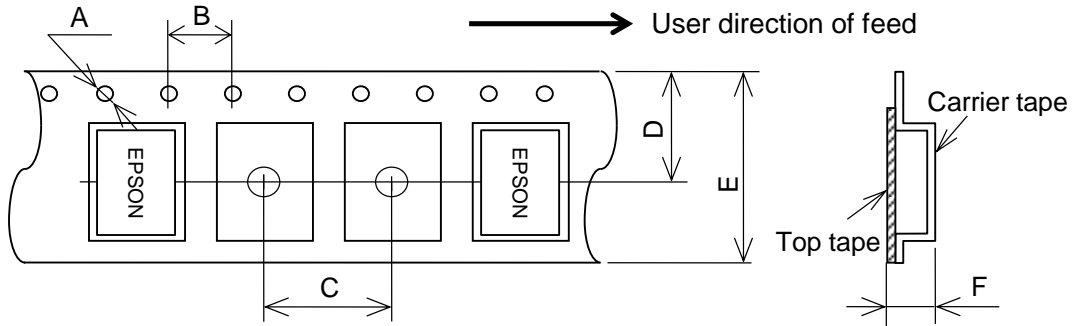
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET

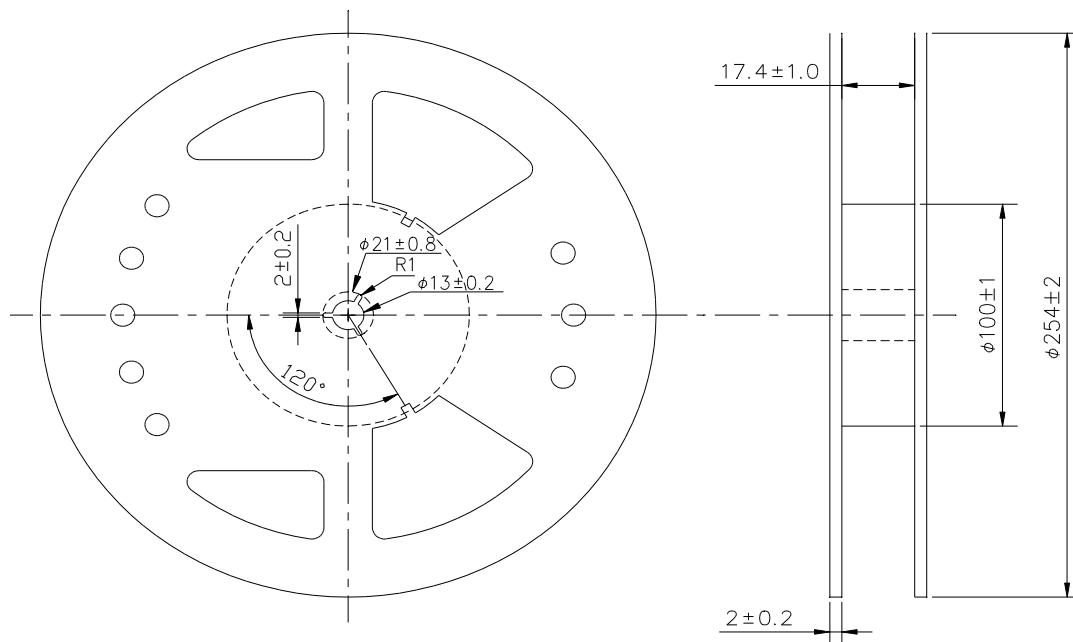
Unit: mm



Symbol	A	B	C	D	E	F
Value	Φ1.5	4.0	8.0	9.25	16.0	2.3

(2) Reel dimensions

Material of the Reel : PS



Form and Size of reel window shows are one of the example

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