

## Clock OSC

## SG5032CAN

SEIKO EPSON CORPORATION

Product name SG5032CAN 48.000000 MHz TJGA  
 Product Number / Ordering code X1G0044510007xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 52 mg

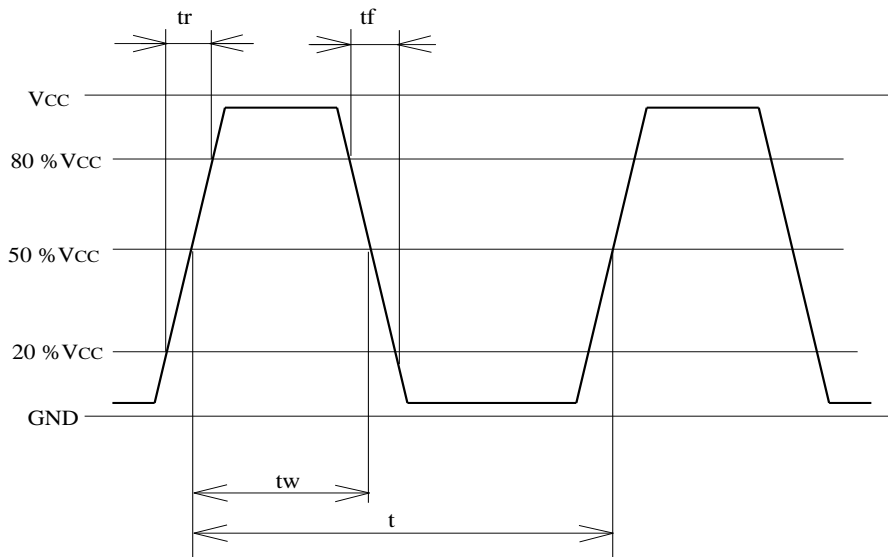
**1.Absolute maximum ratings**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	V <sub>cc</sub> -GND	-0.3	-	+4	V	-
Storage temperature	T <sub>stg</sub>	-40	-	+125	°C	Storage as single product
Input voltage	V <sub>in</sub>	-0.3	-	V <sub>cc</sub> +0.3	V	ST terminal

**2.Specifications(characteristics)**

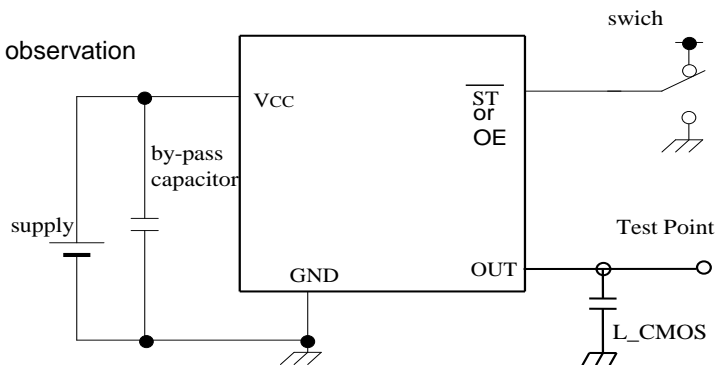
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f <sub>0</sub>		48.000000		MHz	
Supply voltage	V <sub>cc</sub>	1.6	-	3.63	V	-
Operating temperature	T <sub>use</sub>	-40	-	+85	°C	-
Frequency tolerance	f <sub>tol</sub>	-50	-	50	×10 <sup>-6</sup>	T <sub>use</sub>
Current consumption	I <sub>cc</sub>	-	-	2.6	mA	No load condition V <sub>cc</sub> = 3.6V
Stand-by current	I <sub>std</sub>	-	-	2.7	μA	ST = GND
Disable current	I <sub>dis</sub>	-	-	-	mA	-
Symmetry	SYM	45	-	55	%	50% V <sub>cc</sub> Level L <sub>CMOS</sub> ≤15pF
Output voltage	V <sub>OH</sub>	V <sub>cc</sub> -0.4	-	-		-
	V <sub>OL</sub>	-	-	0.4		-
Output load condition	L <sub>CMOS</sub>	-	-	15	pF	CMOS Load
Input voltage	V <sub>IH</sub>	0.8V <sub>cc</sub>	-	-		ST terminal
	V <sub>IL</sub>	-	-	0.2V <sub>cc</sub>		ST terminal
Rise time	t <sub>r</sub>	-	-	3.5	ns	V <sub>cc</sub> 1.8V±10% : 0.2V <sub>cc</sub> to 0.8V <sub>cc</sub> Level, L <sub>CMOS</sub> ≤15pF
Fall time	t <sub>f</sub>	-	-	3.5	ns	V <sub>cc</sub> 1.8V±10% : 0.2V <sub>cc</sub> to 0.8V <sub>cc</sub> Level, L <sub>CMOS</sub> ≤15pF
Start-up time	t <sub>str</sub>	-	-	3	ms	t = 0 at 0.9V <sub>cc</sub>
Jitter	t <sub>DJ</sub>	-	0	-	ps	Deterministic Jitter V <sub>cc</sub> =3.3V
	t <sub>RJ</sub>	-	2.4	-	ps	Random Jitter V <sub>cc</sub> =3.3V
	t <sub>RMS</sub>	-	2.3	-	ps	δ(RMS of total distribution) V <sub>cc</sub> =3.3V
	t <sub>p-p</sub>	-	20	-	ps	Peak to Peak V <sub>cc</sub> =3.3V
	t <sub>acc</sub>	-	2.5	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t <sub>PJ</sub>	-	0.22	-	ps	Off set Frequency: 12kHz to 20MHz, V <sub>cc</sub> =3.3V
Phase noise	L(f)	-	-	-	dBc/Hz	-
		-	-91	-	dBc/Hz	Off set 10Hz V <sub>cc</sub> =3.3V
		-	-120	-	dBc/Hz	Off set 100Hz V <sub>cc</sub> =3.3V
		-	-143	-	dBc/Hz	Off set 1kHz V <sub>cc</sub> =3.3V
		-	-154	-	dBc/Hz	Off set 10kHz V <sub>cc</sub> =3.3V
		-	-158	-	dBc/Hz	Off set 100kHz V <sub>cc</sub> =3.3V
		-	-158	-	dBc/Hz	Off set 1MHz V <sub>cc</sub> =3.3V
Frequency aging	f <sub>age</sub>	-3	-	3	×10 <sup>-6</sup>	@+25°C first year
		-	-	-		-

### 3. Timing chart

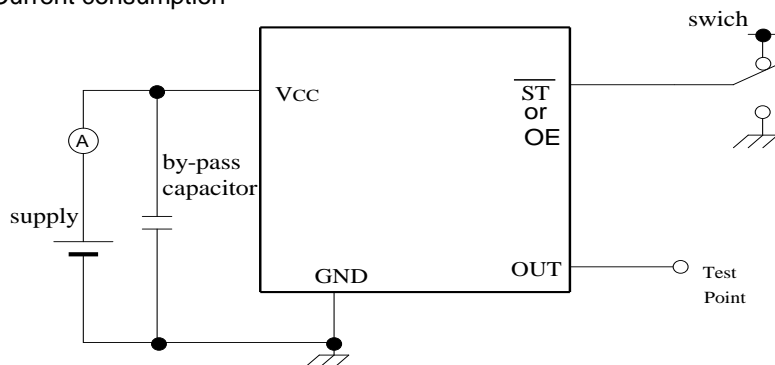


### 4. Test circuit

#### 1) Waveform observation



#### 2) Current consumption



\*Current consumption under the disable function should be = GND.

#### 3) Condition

##### (1) Oscilloscope

- Band width should be minimum 5 times higher (wider) than measurement frequency.
- Probe earth should be placed closely from test point and lead length should be as short as possible

\* Recommendable to use miniature socket. (Don't use earth lead.)

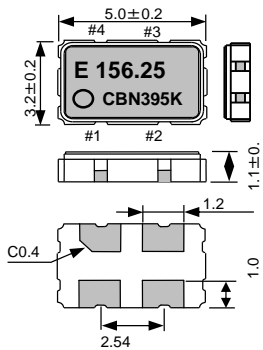
##### (2) L\_CMOS also includes probe capacitance.

(3) By-pass capacitor (0.01  $\mu$ F to 0.1  $\mu$ F) is placed closely between VCC and GND.

(4) Use the current meter whose internal impedance value is small.

##### (5) Power supply

- Start up time (0 %VCC to 90 %VCC) of power source should be more than 150  $\mu$ s.
- Impedance of power supply should be as lowest as possible.

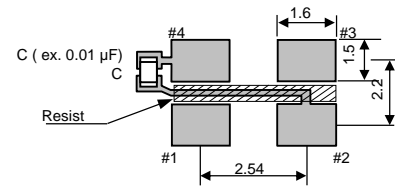
**5.External dimensions (Unit: mm)**

Pin map

Pin	Connection
1*	OE or ST
2	GND
3	OUT
4	V <sub>cc</sub>

\*OE function is only available for 80000000 Hz

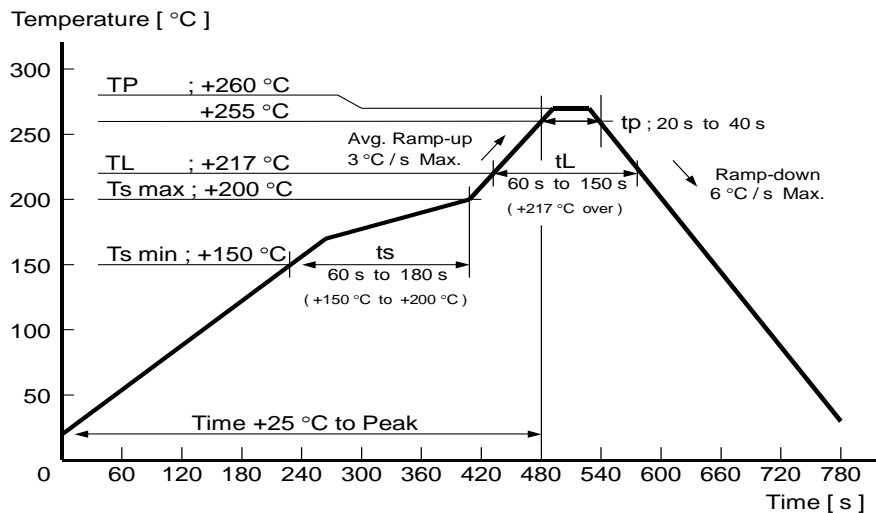
Note.  
 OE pin = "H" or "open" : Specified frequency output.  
 OE pin = "L" : Output is high impedance.  
 ST pin = "H" or "open" : Specified frequency output.  
 ST pin = "L" : Output is high impedance, oscillation stops.

**6.Footprint(Recommended) (Unit: mm)**

To maintain stable operation, provide a 0.01μF to 0.1μF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between V<sub>cc</sub> - GND).

**7.Reflow profile**

Reflow condition (Follow of JEDEC STD-020D.01)

**8.Packing information**

[ 1 ] Product number last 2 digits code(xx) description

The recommended code is "00"

X1G0044510007xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

## [ 2 ] Taping specification

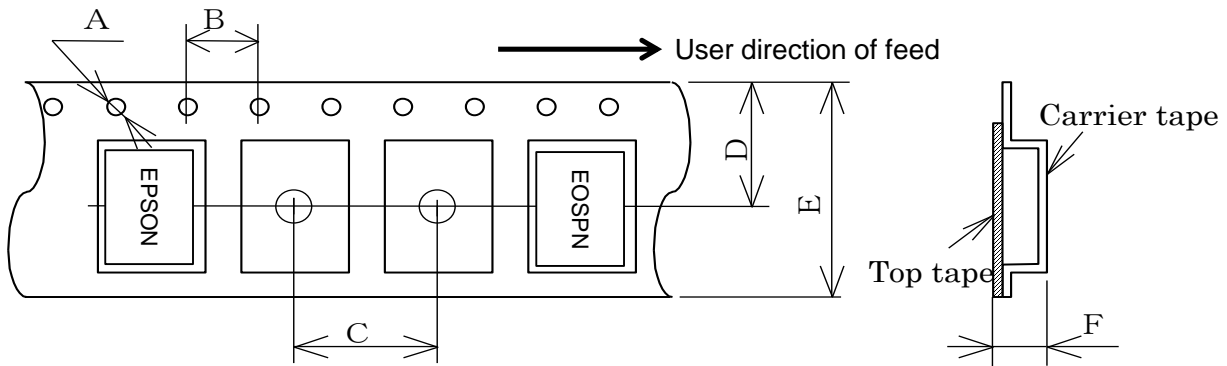
Subject to EIA-481 &amp; IEC-60286

## (1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

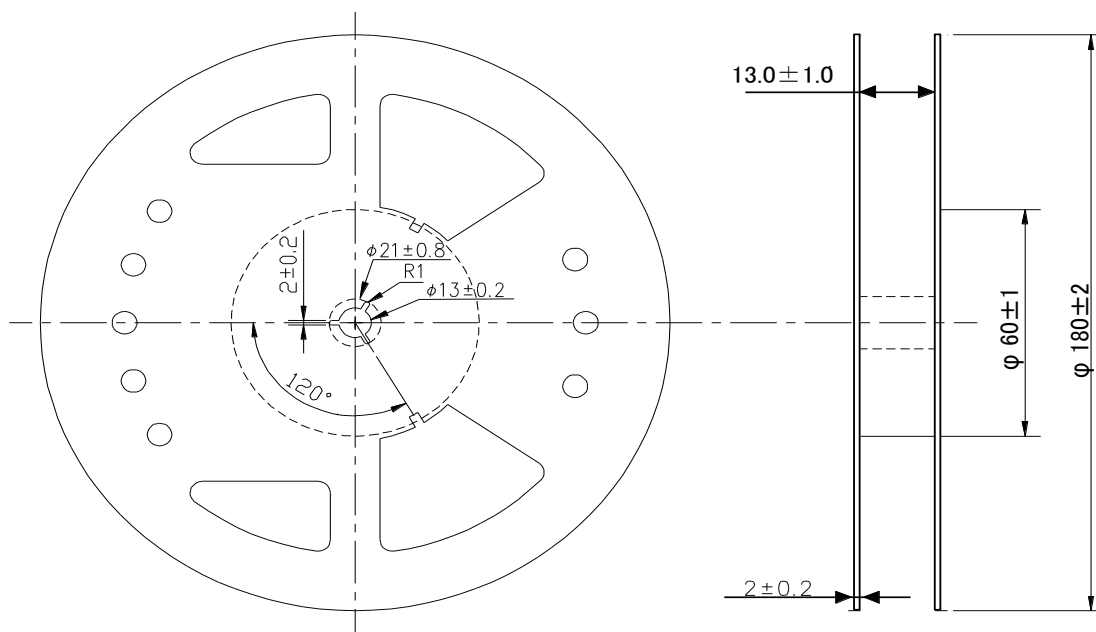


Symbol	A	B	C	D	E	F	G	H
Value	$\phi 1.5$ $+0.1/-0$	$4.0 \pm 0.1$	$8.0 \pm 0.1$	$7.25 \pm 0.2$	$12.0 \pm 0.2$	$1.40 \pm 0.1$	$3.5 \pm 0.1$	$5.4 \pm 0.1$

## (2) Reel dimensions

Center material : PS

Material of the Reel : PS



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