512KB Synchronous Pipeline Burst SRAM Module

FEATURES

- Implemented based on **COAST 3.1**
- Supports Interleave Burst and Linear Burst Mode
- Zero-wait-state operation at 75/66MHz
- TTL compatible inputs/outputs
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- 160-pin DIMM with gold plated Tap
- Series 22 ohm resistors for noise immunity
- Product Family : KMM764V80G-13/15

GENERAL DESCRIPTION

The KMM764V80G is 512K byte high frequency Synchronous Pipeline Burst Static Random Access Memory module organized as 64K words by 64 bits. The module is specially designed as the secondary cache in Pentium and Power PC-based systems. The device for this module is fabricated by SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. The module uses two SAMSUNG's KM732V688G and one KM68257C for 8-bits tag RAM.

PIN NAMES

Name	Function
CLK[1:0]	Clock Inputs
A[18:3]	Cache RAM Address Inputs
D[63:0]	Cache RAM Data Inputs/Outputs
TIO[7:0]	Tag RAM Data Inputs/Outputs
$\overline{TWE}$	Tag RAM Write Enable Input
$\overline{CCS}$	Chip Select Input
$\overline{CWE}$[7:0]	Write Enable Inputs
$\overline{COE}$	Output Enable Input
$\overline{ADSP}$	Address Status Processor
$\overline{CADS}$	Address Status Controller
$\overline{CADV}$	Burst Address Advance
$\overline{BWE}$	Byte Write Enable Input
$\overline{GWE}$	Global Write Enable Input
$\overline{LBO}$	Burst Mode Control
V_{CC5}	Power Supply(5V)
V_{CC3}	Power Supply(3.3V)
V_{SS}	Ground
N.C	No Connections

PD PIN INFORMATION

PD Pin Allocation				Module Part No
PD_3	PD_2	PD_1	PD_0	
Vss	N.C	N.C	N.C	KMM764V80G

PIN CONFIGURATION *(Top View)*

V_{SS}	81	1	V_{SS}	D_{57}	122	42	D_{56}
TIO_1	82	2	TIO_0				
TIO_7	83	3	TIO_2				
TIO_5	84	4	TIO_6	V_{SS}	123	43	V_{SS}
TIO_3	85	5	TIO_4	D_{55}	124	44	D_{54}
N.C	86	6	N.C	D_{53}	125	45	D_{52}
V_{CC5}	87	7	V_{CC3}	D_{51}	126	46	D_{50}
N.C	88	8	$\overline{TWE}$	D_{49}	127	47	D_{48}
$\overline{CADV}$	89	9	$\overline{CADS}$	V_{SS}	128	48	V_{SS}
V_{SS}	90	10	V_{SS}	D_{47}	129	49	D_{46}
$\overline{COE}$	91	11	$\overline{CWE_4}$	D_{45}	130	50	D_{44}
$\overline{CWE_5}$	92	12	$\overline{CWE_6}$	D_{43}	131	51	D_{42}
$\overline{CWE_7}$	93	13	$\overline{CWE_0}$	V_{CC5}	132	52	V_{CC3}
$\overline{CWE_1}$	94	14	$\overline{CWE_2}$	D_{41}	133	53	D_{40}
V_{CC5}	95	15	V_{CC3}	D_{39}	134	54	D_{38}
$\overline{CWE_3}$	96	16	$\overline{CCS}$	D_{37}	135	55	D_{36}
N.C	97	17	$\overline{GWE}$	V_{SS}	136	56	V_{SS}
N.C	98	18	$\overline{BWE}$	D_{35}	137	57	D_{34}
V_{SS}	99	19	V_{SS}	D_{33}	138	58	D_{32}
N.C	100	20	A_3	D_{31}	139	59	D_{30}
A_4	101	21	A_7	V_{CC5}	140	60	V_{CC3}
A_6	102	22	A_5	D_{29}	141	61	D_{28}
A_8	103	23	A_{11}	D_{27}	142	62	D_{26}
A_{10}	104	24	A_{16}	D_{25}	143	63	D_{24}
V_{CC5}	105	25	V_{CC3}	V_{SS}	144	64	V_{SS}
A_{17}	106	26	A_{18}	D_{23}	145	65	D_{22}
V_{SS}	107	27	V_{SS}	D_{21}	146	66	D_{20}
A_9	108	28	A_{12}	D_{19}	147	67	D_{18}
A_{14}	109	29	A_{13}	V_{CC5}	148	68	V_{CC3}
A_{15}	110	30	$\overline{ADSP}$	D_{17}	149	69	D_{16}
N.C	111	31	N.C	D_{15}	150	70	D_{14}
PD_0	112	32	N.C	D_{13}	151	71	D_{12}
PD_2	113	33	PD_1	V_{SS}	152	72	V_{SS}
$\overline{LBO}$(1)	114	34	PD_3	D_{11}	153	73	D_{10}
V_{SS}	115	35	V_{SS}	D_9	154	74	D_8
CLK_0	116	36	N.C/CLK_1	D_7	155	75	D_6
V_{SS}	117	37	V_{SS}	V_{CC5}	156	76	V_{CC3}
D_{63}	118	38	D_{62}	D_5	157	77	D_4
V_{CC5}	119	39	V_{CC3}	D_3	158	78	D_2
D_{61}	120	30	D_{60}	D_1	159	79	D_0
D_{59}	121	41	D_{58}	V_{SS}	160	80	V_{SS}

NOTE :

1. Default is no connect for Intel processor based design because this pin is pulled up with 4.7Kohm resistor on the module.

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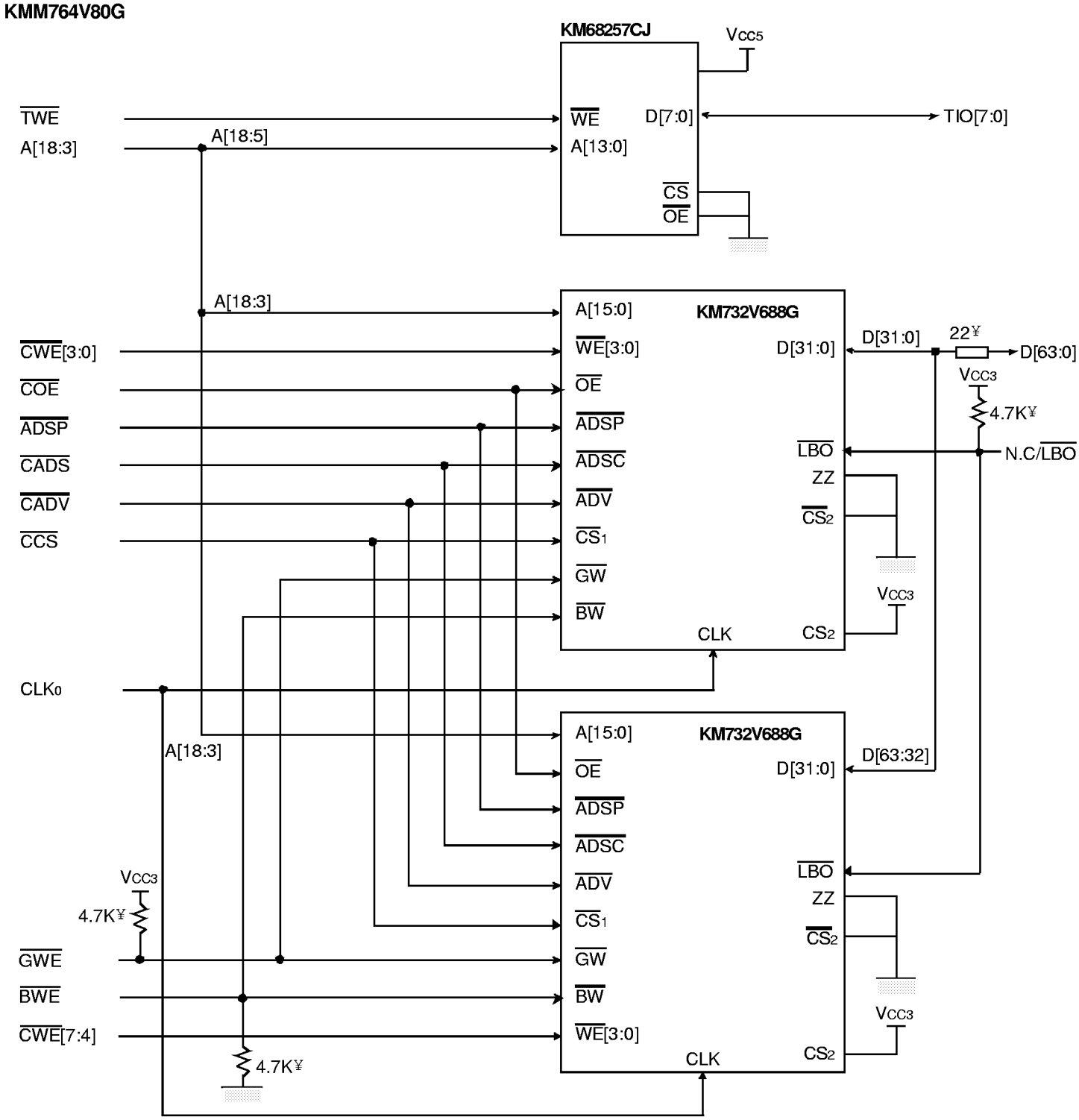
FUNCTIONAL BLOCK DIAGRAM

KMM764V80G



NOTE :

1. ZZ pin is internally connected to Vss and not pinout on the module.
2. $\overline{LBO}$ is pulled up with 4.7Kohm resistor.
3. $\overline{GWE}$ is pulled up with 4.7Kohm resistor and $\overline{BWE}$ is pulled down with 4.7Kohm resistor.

A-1. SYNCHRONOUS PIPELINE BURST TRUTH TABLE (Data field)

$\overline{CCS}$	$\overline{ADSP}$	$\overline{CADS}$	$\overline{CADV}$	$\overline{WRITE}$	K	Address Accessed	Operation
H	X	L	X	X	¡Ł	N/A	Not Selected
H	L	X	X	X	¡Ł	N/A	Not Selected
L	L	X	X	X	¡Ł	External Address	Begin Burst Read Cycle
L	H	L	X	L	¡Ł	External Address	Begin Burst Write Cycle
L	H	L	X	H	¡Ł	External Address	Begin Burst Read Cycle
X	H	H	L	H	¡Ł	Next Address	Continue Burst Read Cycle
H	X	H	L	H	¡Ł	Next Address	Continue Burst Read Cycle
X	H	H	L	L	¡Ł	Next Address	Continue Burst Write Cycle
H	X	H	L	L	¡Ł	Next Address	Continue Burst Write Cycle
X	H	H	H	H	¡Ł	Current Address	Suspend Burst Read Cycle
H	X	H	H	H	¡Ł	Current Address	Suspend Burst Read Cycle
X	H	H	H	L	¡Ł	Current Address	Suspend Burst Write Cycle
H	X	H	H	L	¡Ł	Current Address	Suspend Burst Write Cycle

NOTE :
1. X means "Don't Care"
2. The rising edge of clock is symbolized by ¡Ł
3. $\overline{WRITE}$=L means Write operation in A-2. Synchronous Pipeline Butst Write Truth Table
   $\overline{WRITE}$=H means Read operation in A-2. Synchronous Pipeline Butst Write Truth Table
4. Operation finally depends on status of asynchronous input pin ($\overline{COE}$)

A-2. SYNCHRONOUS PIPELINE BURST WRITE TRUTH TABLE (Data field)

$\overline{GWE}$	$\overline{BWE}$	$\overline{CWE}$ [1:0]	$\overline{CWE}$ [3:2]	$\overline{CWE}$ [5:4]	$\overline{CWE}$ [7:6]	Operation
H	H	X	X	X	X	Read
H	L	H	H	H	H	Read
H	L	L	H	H	H	Write Byte D[15:0]
H	L	H	L	H	H	Write Byte D[31:16]
H	L	H	H	L	L	Write Byte D[63:32]
H	L	L	L	L	L	Write All Bytes
L	X	X	X	X	X	Write All Bytes

NOTE :
1. X means "Don't Care"
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(¡Ł).

B-1. ASYNCHRONOUS TRUTH TABLE (Tag field)

$\overline{TWE}$	Mode	I/O Pin	Supply Current
H	Read	D_{OUT}	I_{CC}
L	Write	D_{IN}	I_{CC}

NOTE : X means "Don't Care"

C. BURST SEQUENCE

Addresses are generated for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

INTERLEAVE BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	High	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	0	0	1	1	1	0
Third Address		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

NOTE :

1. When this pin is no connects, $\overline{LBO}$ should be high.
2. Default is no connect for Intel processor based designs.

LINEAR BURST SEQUENCE TABLE

Pin 114	Pin state	Case 1		Case 2		Case 3		Case 4	
*$\overline{LBO}$	Low	A1	A0	A1	A0	A1	A0	A1	A0
First Address		0	0	0	1	1	0	1	1
Second Address		0	1	1	0	1	1	0	0
Third Address		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

NOTE : $\overline{LBO}$ must be tied to low because this pin is pulled up with 4.7K ¥ on the module.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on V_{CC3} Supply Relative to V_{SS}	V_{CC3}	-0.3 to 4.6	V
Voltage on V_{CC5} Supply Relative to V_{SS}	V_{CC5}	-0.3 to 6.0	V
Voltage on Any Other Pin Relative to V_{SS}	V_{IN}	-0.3 to 6.0	V
Storage Temperature	T_{STG}	-65 to 150	¡
Operating Temperature	T_A	0 to 70	¡
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	¡

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specific ation is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS (T_A =0 to 70¡)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC3}	3.13	3.3	3.6	V
	V_{CC5}	4.75	5.0	5.25	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IL}*	-0.3	-	0.8	V
Input High Voltage	V_{IH}*	2.2	-	Vcc***+0.3	V

* V_{IL3}(min) = -1.4 (Pulse Width ¡´10ns), V_{IL5}(min) = -2.0 (Pulse Width ¡´10ns)

** V_{IH3}(max) = 5.0V (Pulse Width ¡´10ns) ; In case of I/O pins, the maximum V_{IH3}(max) = 4.1V (Pulse Width ¡´10ns)
V_{IH5}(max) = 7.0V (Pulse width ¡´10ns)

*** V_{CC} =V_{CC3} or V_{CC5}

DC ELECTRICAL CHARACTERISTICS* (T_A =0 to 70¡ ,V_{CC}3=3.3V+10%/-5%)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage current	I_{LI}**	V_{CC3}=Max, V_{IN}=Vss to V_{CC3}		-5	5	¥ A
Output Leakage Current	I_{LO}	Output Disable, V_{OUT}=V_{SS} to V_{CC3}		-5	5	¥ A
Operating Current	I_{CC}	f=Max, 100% Duty V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	75MHz	-	400	mA
			66MHz	-	360	
Standby Current	I_{SB}	f=Max, 100% Duty, Device deselected, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA		-	60	mA
	I_{SB1}	f=0MHz, Device deselected, V_{IN} ¡ˆV_{CC3} -0.2V or V_{IL}, V_{IN} ¡´0.2V, I_{OUT}=0mA		-	10	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

* Excludes Tag field.

** ILI for $\overline{LBO}$, $\overline{GWE}$ and $\overline{BWE}$ is ¡ 1mA (Max.)

CAPACITANCE* (f=1MHz,T_A=25¡)

Item	Symbol	Test Condition	Min.	Max.	Unit
Address, $\overline{ECS}$ Input Capacitance	C_{IN1}	V_{IN}=0V	-	35	pF
$\overline{TWE}$, $\overline{CWE}$, CLK Input Capacitance	C_{IN2}	V_{IN}=0V	-	20	pF
$\overline{COE}$, $\overline{ADSP}$, $\overline{CADS}$, $\overline{CADV}$, $\overline{CCS}$ $\overline{GWE}$, $\overline{BWE}$ Input Capacitance	C_{IN3}	V_{IN}=0V	-	30	pF
Data and Tag Input/Output Capacitance	$C_{I/O1}$	$V_{I/O}$=0V	-	15	pF

* **NOTE** : Capacitance is sampled and not 100% tested.

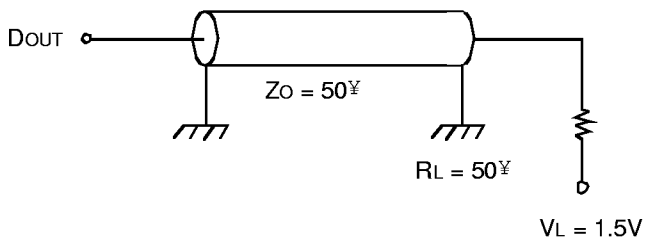
AC CHARACTERISTICS

TEST CONDITIONS ON DATA RAM

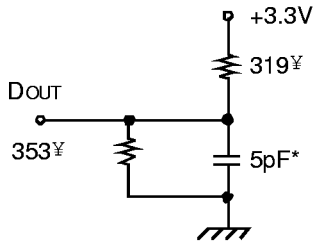
(T_A=0 to 70 ¡ ,V_{CC3}=3.3V+10%/-5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	2ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tLZC, tLZOE, tHZOE & tHZC)



* Including Scope and Jig Capacitance

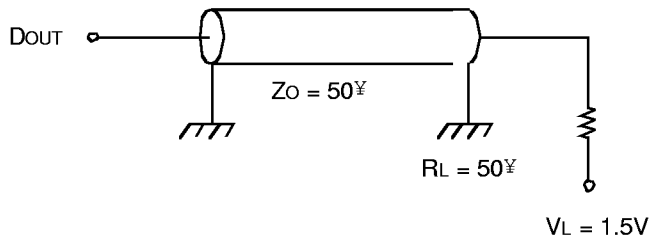
Fig. 1

TEST CONDITIONS ON TAG RAM

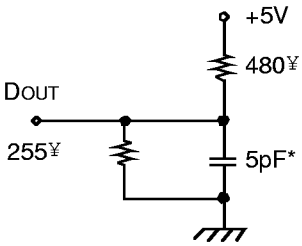
(T_A =0 to 70 ¡ ,V_{CC5}=5.0V ¡ 5%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Time (Measured at 0.3V and 2.7V)	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig 1

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ & tOW)



* Including Scope and Jig Capacitance

Fig. 2

AC TIMING CHARACTERISTICS ON DATA RAM

(T_A =0 to 70 ¡ ,V_{CC3}=3.3V+10%/-5%)

Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V80G-13		KMM764V80G-15		Unit
		Min	Max	Min	Max	
Cycle Time	tCYC	13	-	15	-	ns
Clock Access Time	tCD	-	7	-	8	ns
Output Enable to Data Valid	tOE	-	6	-	7	ns
Clock High to Output Low-Z	tLZC	6	-	6	-	ns
Output Hold from Clock High	tOH	3	-	3	-	ns
Output Enable Low to Output Low-Z	tLZOE	2	-	2	-	ns
Output Enable High to Output High-Z	tHZOE	2	5	2	6	ns
Clock High to Output High-Z	tHZC	-	7	-	7	ns
Clock High Pulse Width	tCH	4.5	-	5.5	-	ns
Clock Low Pulse Width	tCL	4.5	-	5.5	-	ns
Address Setup to Clock High	tAS	2.5	-	2.5	-	ns
Address Status Setup to Cock High	tSS	2.5	-	2.5	-	ns
Data Setup to Cock High	tDS	2.5	-	2.5	-	ns
Write Setup to Clock High ($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWS	2.5	-	2.5	-	ns
Address Advance Setup to Clock High	tADVS	2.5	-	2.5	-	ns
Chip Select Setup to Clock High	tCSS	2.5	-	2.5	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GWE}$, $\overline{BWE}$, $\overline{CWEx}$)	tWH	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	ns

NOTE :

1. All address inputs must meet the specified setup and hold times for all rising clock(Clk) edges whenever $\overline{CADS}$ and/or $\overline{ADSP}$ is sampled low and this device is chip selected. All other synchronous inputs must meet the specified sample and hold times whenever this device is chi p selected.
2. Both chip selects must be active whenever $\overline{CADS}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enable.

AC TIMING CHARACTERISTICS ON TAG RAM

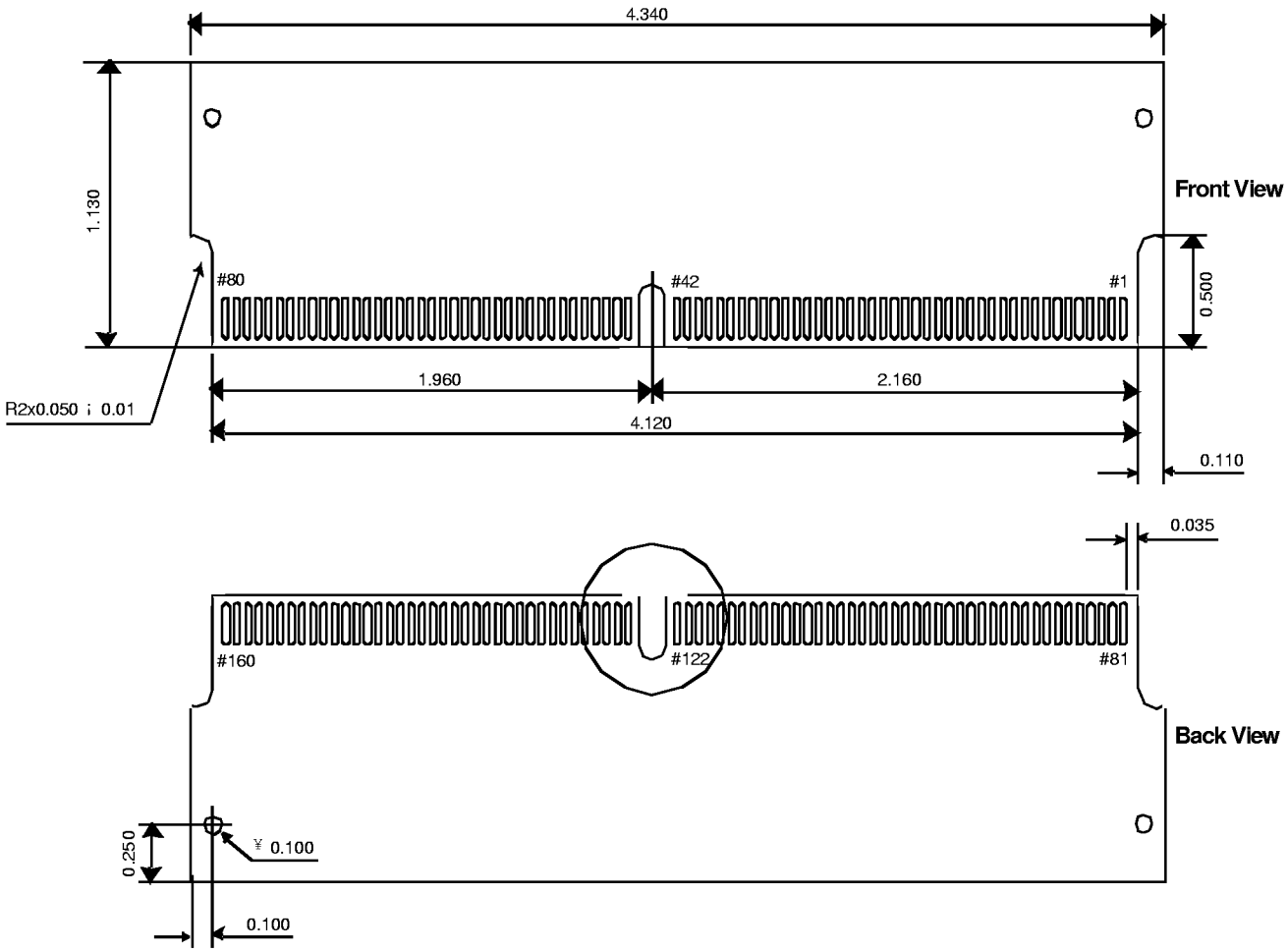
(T_A =0 to 70 ¡ ,V_{CC5}=5.0V ¡ 5%)

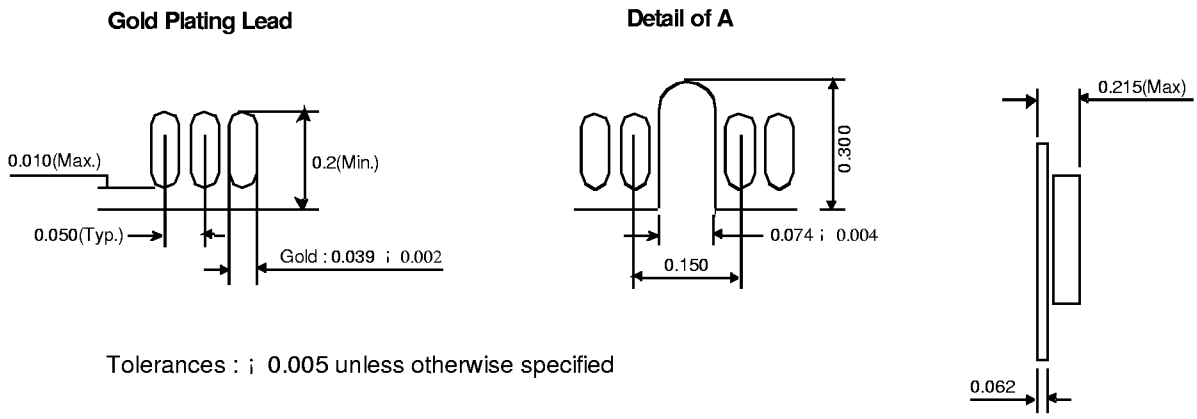
Refers to the individual components, not the whole module

Parameter	Symbol	KMM764V80G-13		KMM764V80G-15		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	12	-	15	-	ns
Address Access Time	tAA	-	12	-	15	ns
Output Hold from Address Change	tOH	3	-	3	-	ns
Write cycle Time	tWC	12	-	15	-	ns
Chip Select to End of Write	tCW	9	-	11	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Address Valid to End of Write	tAW	9	-	12	-	ns
Write Pulse Width	tWP	12	-	15	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Write to Output High-Z	tWHZ	0	6	0	8	ns
Data to Write Time Overlap	tDW	7	-	8	-	ns
Data Hold from Write Time	tDH	0	-	0	-	ns
End Write to Output Low-Z	tOW	0	-	0	-	ns

PACKAGE DIMENSIONS

Units : Inches





Tolerances : ¡ 0.005 unless otherwise specified