Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS SEMICONDUCTOR

IRFP140, IRFP141, IRFP142, IRFP143

27A and 31A, 80V and 100V, 0.077 and 0.099 Ohm, N-Channel Power MOSFETs

January 1998

Features

- 27A and 31A, 80V and 100V
- $r_{DS(ON)}$ = 0.077Ω and 0.099Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRFP140	TO-247	IRFP140
IRFP141	TO-247	IRFP141
IRFP142	TO-247	IRFP142
IRFP143	TO-247	IRFP143

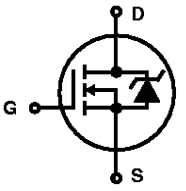
NOTE: When ordering, include the entire part number.

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

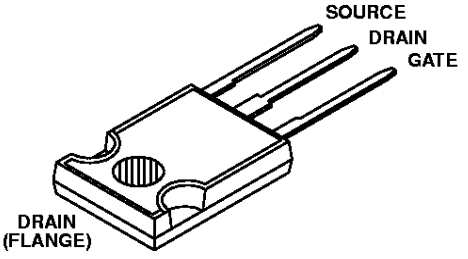
Formerly developmental type TA17421.

Symbol



Packaging

JEDEC STYLE TO-247



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2086.2**

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	IRFP140	IRFP141	IRFP142	IRFP143	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DS}	100	80	100	80	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . . V_{DGR}	100	80	100	80	V
Continuous Drain Current . . . . . I_D	31	31	27	27	A
$T_C = 100^oC$ . . . . . I_D	22	22	19	19	A
Pulsed Drain Current (Note 3) . . . . . I_{DM}	120	120	110	110	A
Gate to Source Voltage . . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . . P_D	180	180	180	180	W
Linear Derating Factor	1.2	1.2	1.2	1.2	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4) . . . . . E_{AS}	100	100	100	100	mJ
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 175	-55 to 175	-55 to 175	-55 to 175	^{o}C
Maximum Temperature for Soldering					
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	300	300	300	^{o}C
Package Body for 10s, See Techbrief 334 . . . . . T_{pkg}	260	260	260	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

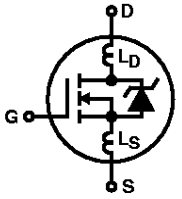
NOTE:

1. $T_J = 25^oC$ to 150^oC.

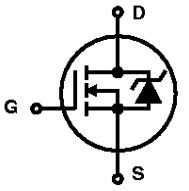
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA, (Figure 10)				
IRFP140, IRFP142			100	-	-	V
IRFP141, IRFP143			80	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V				
IRFP140, IRFP141			31	-	-	A
IRFP142, IRFP143			27	-	-	A
Gate to Source Leakage	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 19A, (Figures 8, 9)				
IRFP140, IRFP141			-	0.055	0.077	Ω
IRFP142, IRFP143			-	0.077	0.099	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 19A, (Figure 12)	9.3	14	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, $I_D \approx 28A$, $R_G = 9.1\Omega$, $R_L = 1.7\Omega$, V_{GS} = 10V, (Figure 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	15	23	ns
Rise Time	t_r		-	72	110	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	40	60	ns
Fall Time	t_f		-	50	75	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, $I_D \approx 27A$, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)}$ = 1.5mA, (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	38	59	nC
Gate to Source Charge	Q_{gs}		-	10	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	21	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	V_{GS} = 0V, $V_{DS} \approx$ 25V, f = 1.0MHz, (Figure 11)		-	1275	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	160	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on Header That is Closer to Source and Gate Pins and Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	12.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.83	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	30	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode		-	-	31	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	120	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, I_{SD} = 31A, V_{GS} = 0V, (Figure 13)		-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, I_{SD} = 28A, dI_{SD}/dt = 100A/μs		70	150	300	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, I_{SD} = 28A, dI_{SD}/dt = 100A/μs		0.44	0.91	1.9	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. V_{DD} = 25V, starting $T_J = 25^oC$, L = 160μH, R_G = 50Ω, peak I_{AS} = 31A. (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

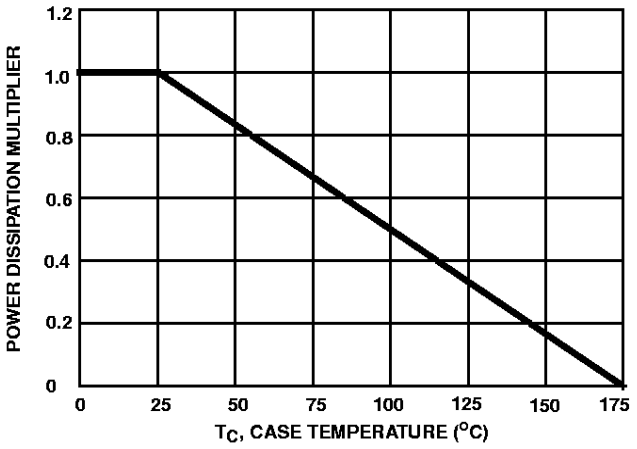


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURW

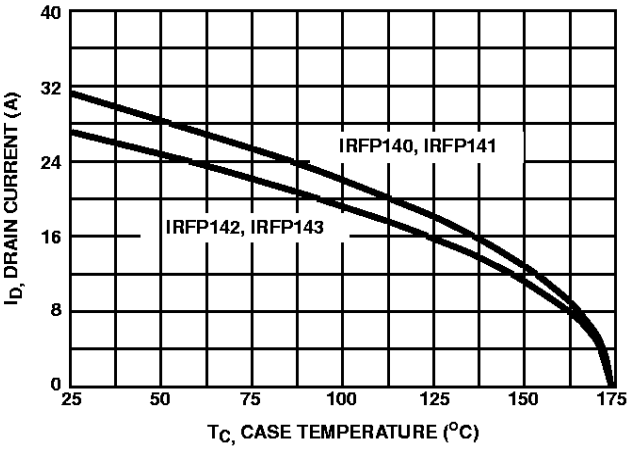


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

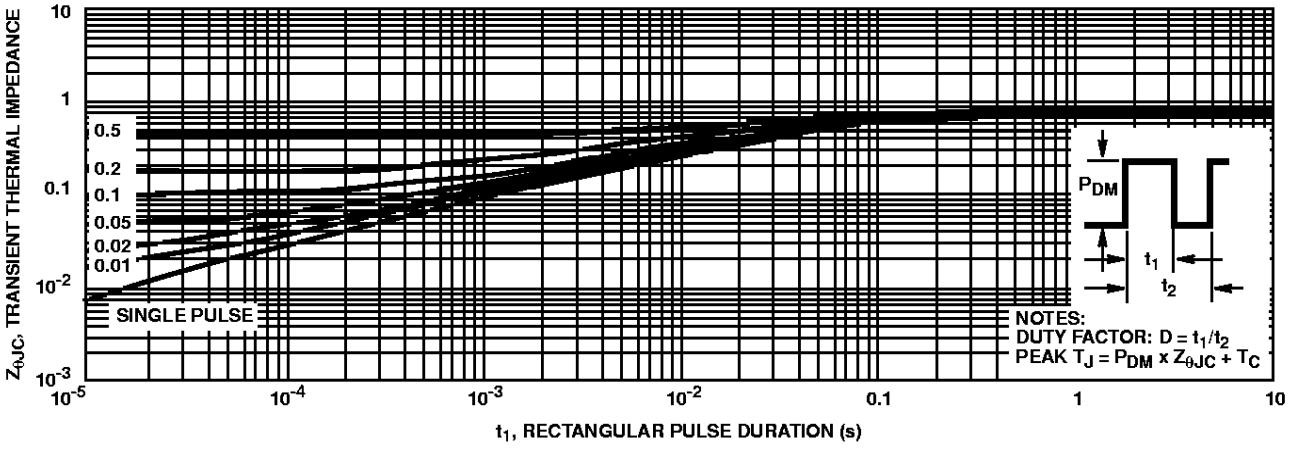


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

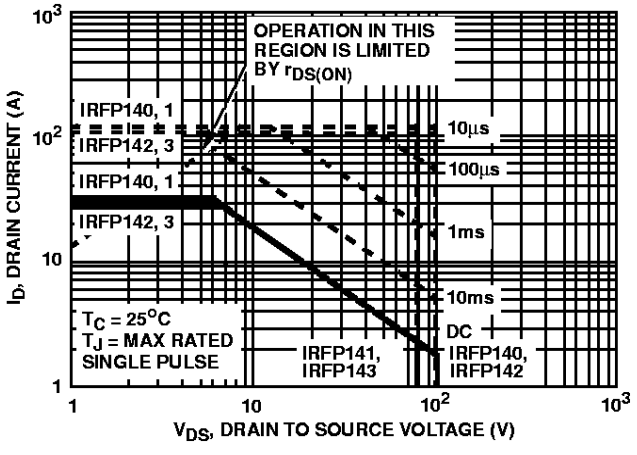


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

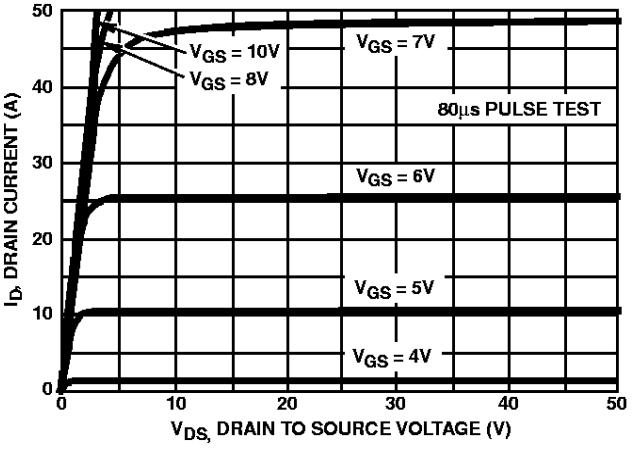


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves Unless Otherwise Specified (Continued)

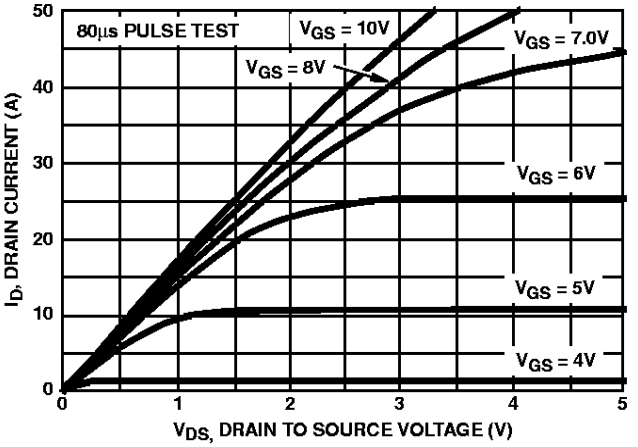


FIGURE 6. SATURATION CHARACTERISTICS

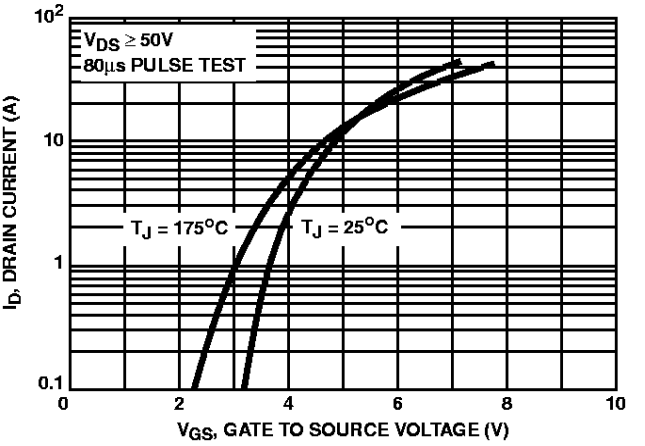
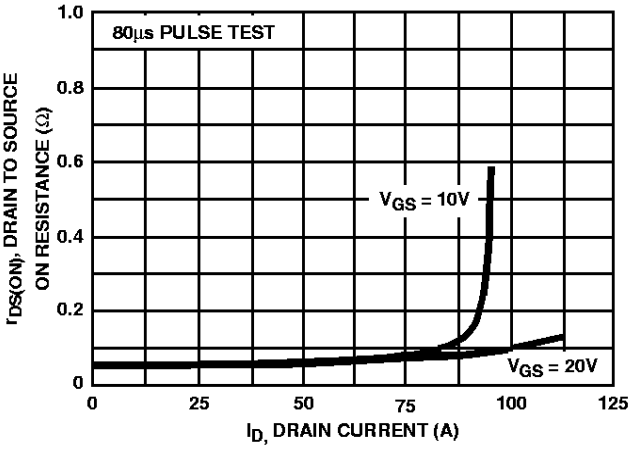


FIGURE 7. TRANSFER CHARACTERISTICS



NOTE: Heating effect of 2μs pulse is minimal.

FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

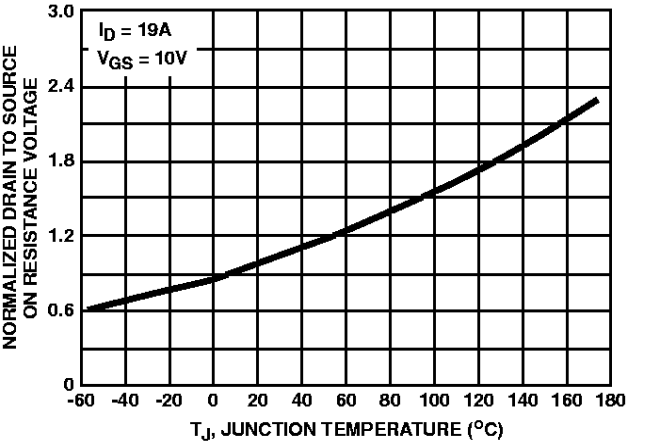


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

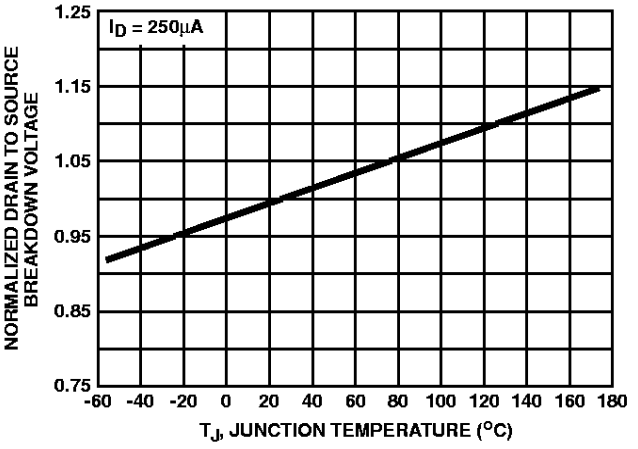


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

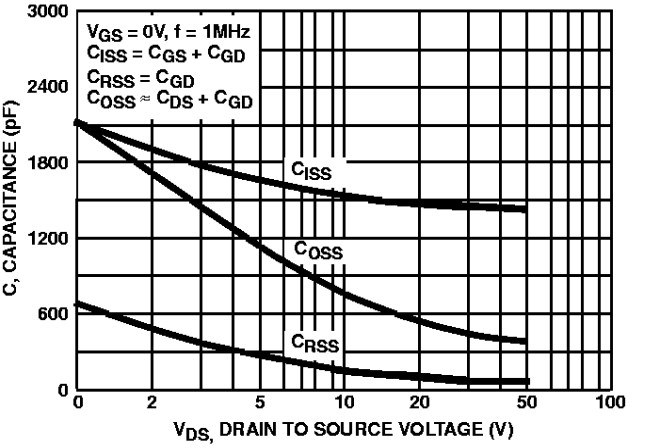


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves Unless Otherwise Specified (Continued)

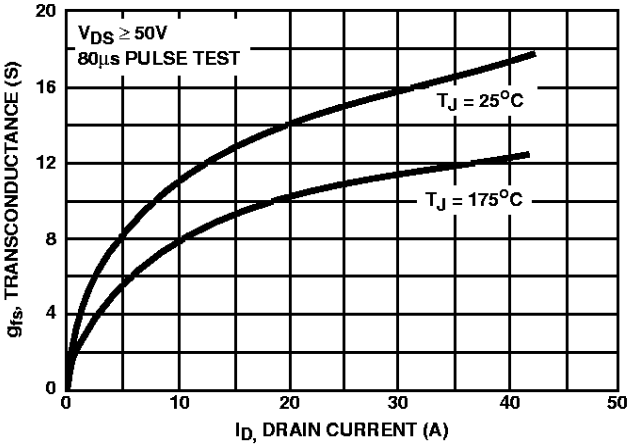


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

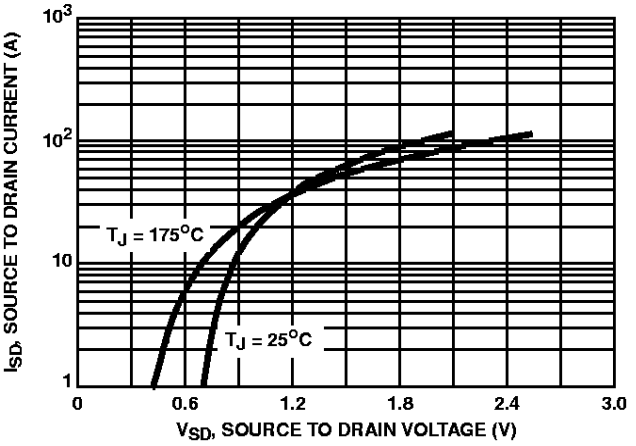


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

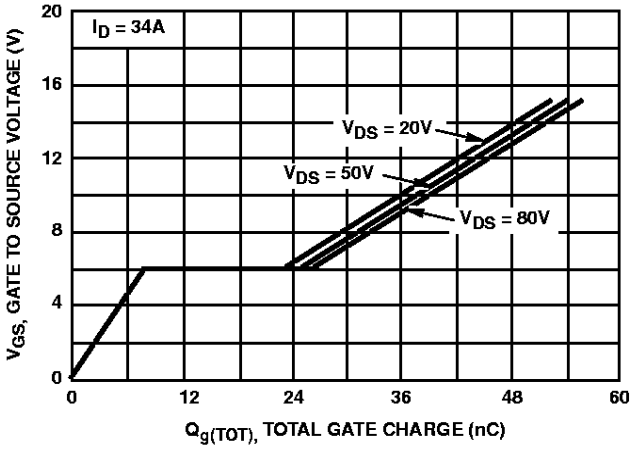


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

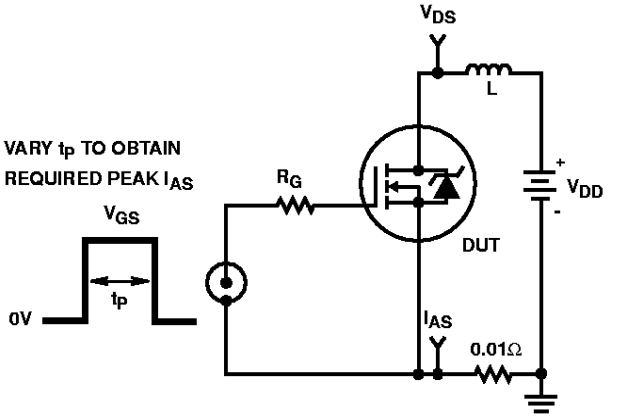


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

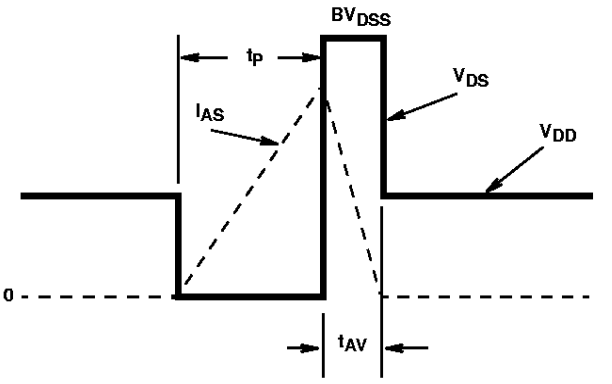


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

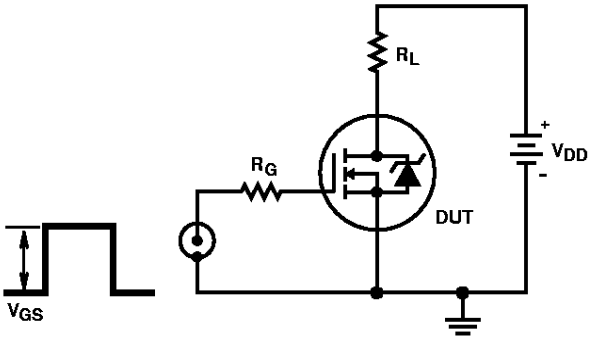


FIGURE 17. SWITCHING TIME TEST CIRCUIT

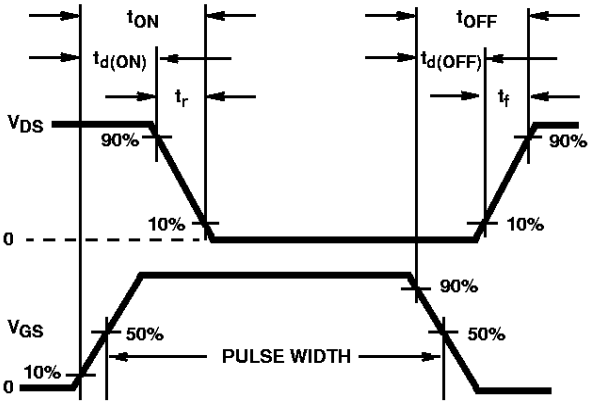


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

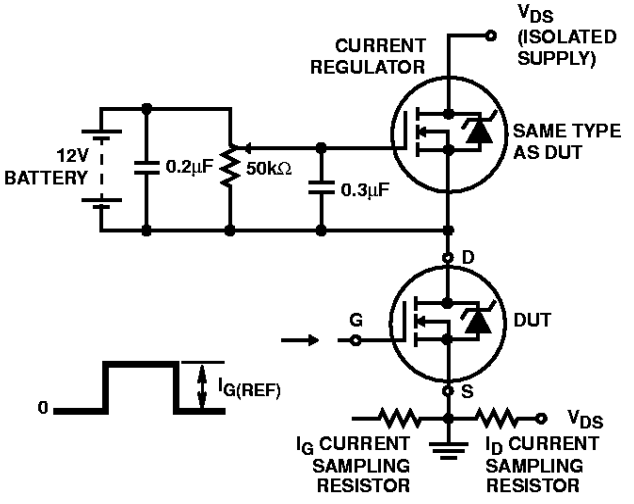


FIGURE 19. GATE CHARGE TEST CIRCUIT

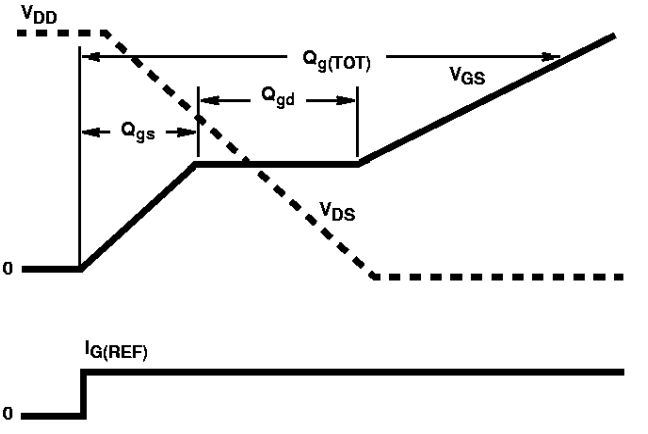


FIGURE 20. GATE CHARGE WAVEFORMS