

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

August 1997

Quad SPST, CMOS Analog Switches

Features

- **Input Signal Range** $\pm 15V$
- **Low $r_{DS(ON)}$** $\leq 175\Omega$
- **TTL, CMOS Compatible**
- **Latch Proof**
- **True Second Source**
- **Maximum Supply Ratings** $44V$
- **Logic Inputs Accept Negative Voltages**

Ordering Information

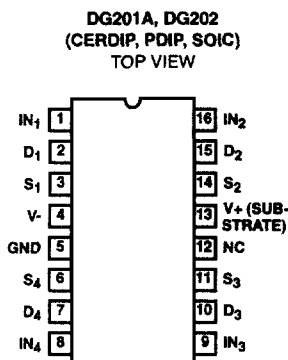
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
DG201AAK	-55 to 125	16 Ld CERDIP	F16.3
DG201ABK	-25 to 85	16 Ld CERDIP	F16.3
DG201AAK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG201ACK	0 to 70	16 Ld CERDIP	F16.3
DG201ACJ	0 to 70	16 Ld PDIP	E16.3
DG201ACY	0 to 70	16 Ld SOIC	M16.3
DG202AK	-55 to 125	16 Ld CERDIP	F16.3
DG202AK/883B	-55 to 125	16 Ld CERDIP	F16.3
DG202BK	-25 to 85	16 Ld CERDIP	F16.3
DG202CJ	0 to 70	16 Ld PDIP	E16.3

Description

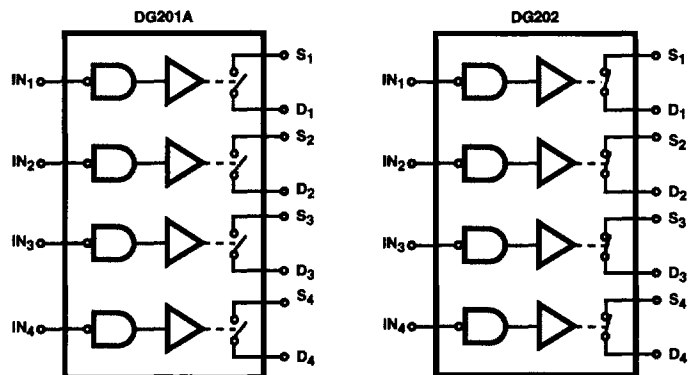
The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Harris' 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to 30V_{p-p} in the OFF state, the DG201A and DG202 offer the advantages of low ON resistance ($\leq 175\Omega$), wide input signal range ($\pm 15V$) and provide both TTL and CMOS compatibility.

The DG201A and DG202 are specification and pinout compatible with the industry standard devices.

Pinout



Functional Block Diagrams



NOTES:

1. Four SPST switches per package.
2. Switches shown for logic "1" input.

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" $\leq 0.8V$, Logic "1" $\geq 2.4V$

DG201A, DG202

Absolute Maximum Ratings

V+ to V-	44V
V- to Ground	-25V
V _{IN} to Ground (Note 1)	(V- -2V), (V+ +2V)
V _S or V _D to V+ (Note 1)	+2, (V- -2V)
V _S or V _D to V- (Note 1)	-2, (V+ +2V)
Current, any Terminal Except S or D	30mA
Continuous Current, S or D	20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max)	70mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	75	20
PDIP Package	100	N/A
SOIC Package	100	N/A
Maximum Junction Temperature		
CERDIP Package	175°C	
PDIP Package	150°C	
Maximum Storage Temperature Range		
C Suffix	-65°C to 125°C	
A and B Suffix	-65°C to 150°C	
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on V_S, V_D, or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_+ = 15V, V_- = -15V, GND = 0V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS	
		MIN	(NOTE 3) TYP	MAX	MIN	(NOTE 3) TYP	MAX		
DYNAMIC CHARACTERISTICS									
Turn-On Time, t_{ON}	See Figure 1	-	480	600	-	480	-	ns	
Turn-Off Time, t_{OFF}	See Figure 1	-	370	450	-	370	-	ns	
Charge Injection, Q	$C_L = 1000pF, R_S = 0, V_S = 0V$	-	20	-	-	20	-	pC	
Source OFF Capacitance, $C_{S(OFF)}$	$f = 140kHz, V_{IN} = 5V, V_S = 0V$	-	5.0	-	-	5.0	-	pF	
Drain OFF Capacitance, $C_{D(OFF)}$	$f = 140kHz, V_{IN} = 5V, V_D = 0V$	-	5.0	-	-	5.0	-	pF	
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	$f = 140kHz, V_{IN} = 5V, V_S = V_D = 0V$	-	16	-	-	16	-	pF	
OFF Isolation, OIRR	$V_{IN} = 5V, Z_L = 75\Omega, V_S = 2.0V, f = 100kHz$	-	70	-	-	70	-	dB	
Crosstalk (Channel to Channel), CCRR		-	90	-	-	90	-	dB	
INPUT									
Input Current with Voltage High, I_{INH}	$V_{IN} = 2.4V$	-1.0	-0.0004	-	-1.0	-0.0004	-	μA	
	$V_{IN} = 15V$	-	0.003	1.0	-	0.003	1.0	μA	
Input Current with Voltage Low, I_{INL}	$V_{IN} = 0V$	-1.0	-0.0004	-	-1.0	-0.0004	-	μA	
SWITCH									
Analog Signal Range, V_{ANALOG}		-15	-	15	-15	-	15	V	
Drain Source On Resistance, $r_{DS(ON)}$	$V_D = \pm 10V, V_{IN} = 0.8V$ (DG201A) $I_S = 1mA, V_{IN} = 2.4V$ (DG202)	-	115	175	-	115	200	Ω	
Source OFF Leakage Current, $I_{S(OFF)}$	$V_{IN} = 2.4V$ (DG201A) $V_{IN} = 0.8V$ (DG202)	$V_S = 14V, V_D = -14V$	-	0.01	1.0	-	0.01	5.0	nA
		$V_S = -14V, V_D = 14V$	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	$V_{IN} = 2.4V$ (DG201A) $V_{IN} = 0.8V$ (DG202)	$V_S = -14V, V_D = 14V$	-	0.01	1.0	-	0.01	5.0	nA
		$V_S = 14V, V_D = -14V$	-1.0	-0.02	-	-5.0	-0.02	-	nA

DG201A, DG202

Electrical Specifications $V_+ = 15V, V_- = -15V, GND = 0V, T_A = 25^\circ C$ (Continued)

PARAMETER	TEST CONDITIONS		DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS
			MIN	(NOTE 3) TYP	MAX	MIN	(NOTE 3) TYP	MAX	
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	$V_{IN} = 0.8V$ (DG201A) $V_{IN} = 2.4V$ (DG202)	$V_D = V_S = 14V$	-	0.1	1.0	-	0.1	5.0	μA
		$V_D = V_S = -14V$	-1.0	-0.15	-	-5.0	-0.15	-	μA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I_+	All Channels ON or OFF		-	0.9	2	-	0.9	2	mA
Negative Supply Current, I_-			-1	-0.3	-	-1	-0.3	-	mA

Electrical Specifications $V_+ = 15V, V_- = -15V, GND = 0V, T_A$ Over Operating Temperature Range

PARAMETER	TEST CONDITIONS		DG201AA/DG202A			DG201AB, C/DG202B, C			UNITS
			MIN	(NOTE 3) TYP	MAX	MIN	(NOTE 3) TYP	MAX	
INPUT									
Input Current with Voltage High, I_{INH}	$V_{IN} = 2.4V$		-10	-	-	-	-	-	μA
	$V_{IN} = 15V$		-	-	10	-	-	-	μA
Input Current with Voltage Low, I_{INL}	$V_{IN} = 0V$		-10	-	-	-	-	-	μA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-	-	-	V
Drain Source On Resistance, $r_{DS(ON)}$	$V_D = \pm 10V, V_{IN} = 0.8V$ (DG201A) $I_S = 1mA, V_{IN} = 2.4V$ (DG202)		-	-	250	-	-	-	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	$V_{IN} = 2.4V$ (DG201A) $V_{IN} = 0.8V$ (DG202)	$V_S = 14V, V_D = -14V$	-	-	100	-	-	-	nA
		$V_S = -14V, V_D = 14V$	-100	-	-	-	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		$V_S = -14V, V_D = 14V$	-	-	100	-	-	-	nA
		$V_S = 14V, V_D = -14V$	-100	-	-	-	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 5)	$V_{IN} = 0.8V$ (DG201A) $V_{IN} = 2.4V$ (DG202)	$V_D = V_S = 14V$	-	-	200	-	-	-	μA
		$V_D = V_S = -14V$	-200	-	-	-	-	-	μA

NOTES:

3. Typical values are for design aid only, not guaranteed and not subject to production testing.
4. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
5. $I_{D(ON)}$ is leakage from driver into ON switch.

Test Circuits and Waveforms

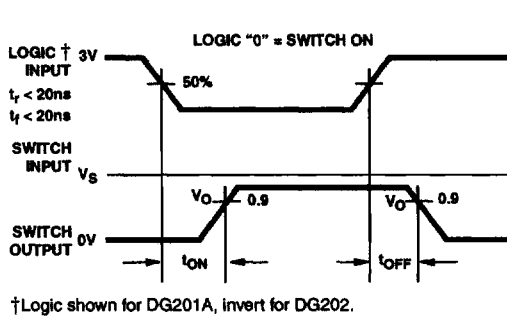
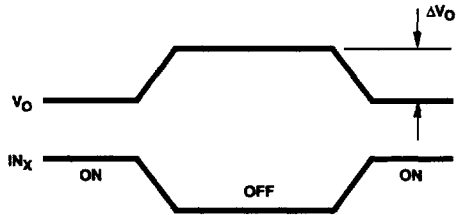
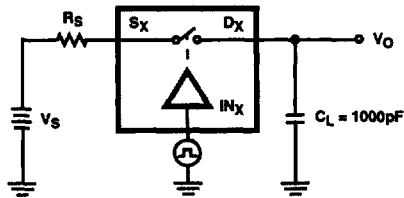
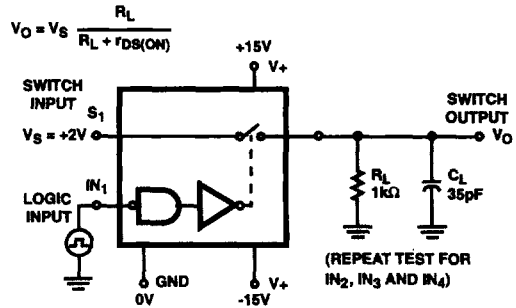


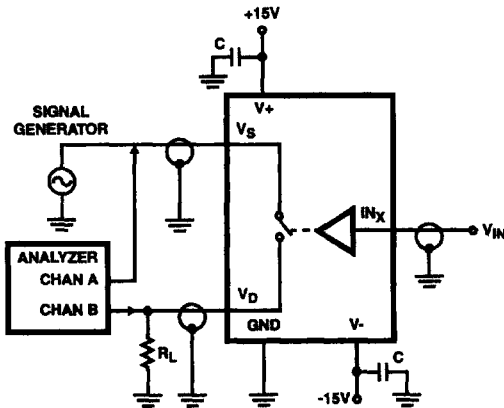
FIGURE 1. t_{ON} AND t_{OFF} SWITCHING TEST CIRCUIT AND WAVEFORM



NOTES:

- 6. ΔV_O = Measured voltage error due to charge injection.
- 7. The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

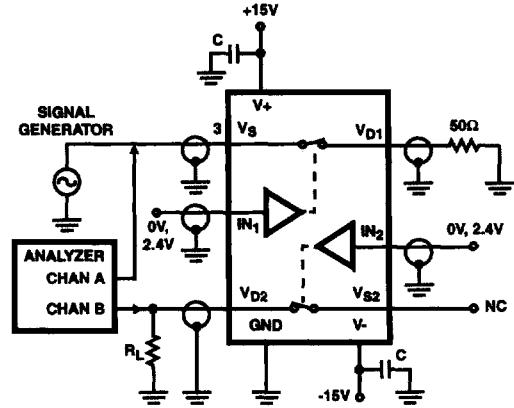
FIGURE 2. CHARGE INJECTION TEST CIRCUIT AND WAVEFORM



$C = 0.001\mu F // 0.1\mu F$
Chip Capacitors

$$OIRR = 20 \log \left| \frac{V_S}{V_D} \right|$$

FIGURE 3. OFF ISOLATION TEST CIRCUIT



$C = 0.001\mu F // 0.1\mu F$
Chip Capacitors

$$CCRR = 20 \log \left| \frac{V_{S1}}{V_{D2}} \right|$$

FIGURE 4. CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT