

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

MM74HC04 Hex Inverter

Features

- Typical propagation delay: 8ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10μW maximum at room temperature
- Low input current: 1μA maximum

General Description

The MM74HC04 inverters utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

The MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Ordering Information

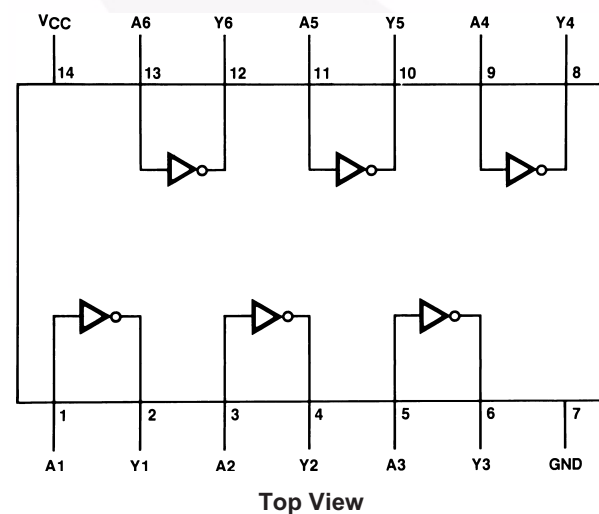
Order Number	Package Number	Package Description
MM74HC04M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC04SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC04MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC04N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Logic Diagram



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5 to +7.0V
V_{IN}	DC Input Voltage	−1.5 to $V_{CC}+1.5V$
V_{OUT}	DC Output Voltage	−0.5 to $V_{CC}+0.5V$
I_{IK}, I_{OK}	Clamp Diode Current	±20mA
I_{OUT}	DC Output Current, per pin	±25mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50mA
T_{STG}	Storage Temperature Range	−65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic “N” package: −12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	2	6	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	−40	+85	°C
t_r, t_f	Input Rise or Fall Times $V_{CC} = 2.0V$		1000	ns
	$V_{CC} = 4.5V$		500	ns
	$V_{CC} = 6.0V$		400	ns

DC Electrical Characteristics⁽³⁾

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	2.0			1.5	1.5	1.5	V
		4.5			3.15	3.15	3.15	
		6.0			4.2	4.2	4.2	
V _{IL}	Maximum LOW Level Input Voltage	2.0			0.5	0.5	0.5	V
		4.5			1.35	1.35	1.35	
		6.0			1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output Voltage	2.0	V _{IN} = V _{IL} , I _{OUT} ≤ 20μA	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	V _{IN} = V _{IL} , I _{OUT} ≤ 4.0mA	4.2	3.98	3.84	3.7	
		6.0	V _{IN} = V _{IL} , I _{OUT} ≤ 5.2mA	5.7	5.48	5.34	5.2	
V _{OL}	Maximum LOW Level Output Voltage	2.0	V _{IN} = V _{IH} , I _{OUT} ≤ 20μA	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	V _{IN} = V _{IH} , I _{OUT} ≤ 4.0mA	0.2	0.26	0.33	0.4	
		6.0	V _{IN} = V _{IH} , I _{OUT} ≤ 5.2mA	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	6.0	V _{IN} = V _{CC} or GND		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	6.0	V _{IN} = V _{CC} or GND, I _{OUT} = 0μA		2.0	20	40	μA

Note:

3. For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics
 $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15pF$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay		8	15	ns

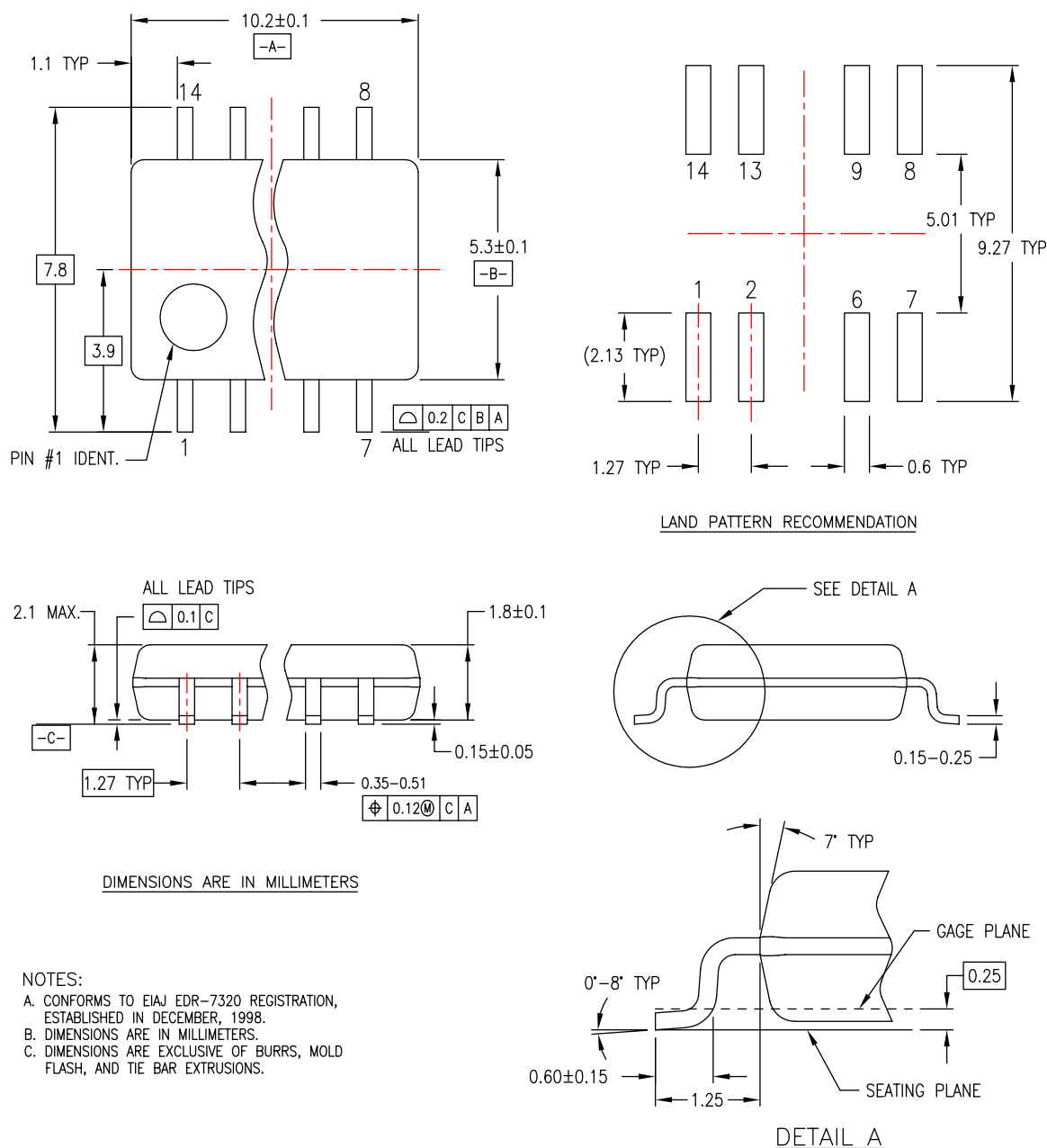
AC Electrical Characteristics
 $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50pF$, $t_r = t_f = 6ns$ (unless otherwise specified)

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A = −40°C to 85°C	T _A = −55°C to 125°C	Units
				Typ.	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay	2.0		55	95	120	145	ns
		4.5		11	19	24	29	
		6.0		9	16	20	24	
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time	2.0		30	75	95	110	ns
		4.5		8	15	19	22	
		6.0		7	13	16	19	
C _{PD}	Power Dissipation Capacitance ⁽⁴⁾		(per gate)	20				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions (Continued)



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)**NOTES: UNLESS OTHERWISE SPECIFIED**

THIS PACKAGE CONFORMS TO

A) JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSIONS.D) DIMENSIONS AND TOLERANCES PER
ASME Y14.5-1994

E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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

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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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