

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# 4-Mbit (256K x 16) Static RAM

## Features

- Pin equivalent to CY7C1041BV33
- Temperature Ranges
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Automotive-A: -40°C to 85°C
  - Automotive-E: -40°C to 125°C
- High speed
  - $t_{AA} = 10$  ns
- Low active power
  - 324 mW (max.)
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in Pb-free and non Pb-free 44-pin 400-mil-SOJ, 44-pin TSOP II and 48-ball FBGA packages

## Functional Description<sup>[1]</sup>

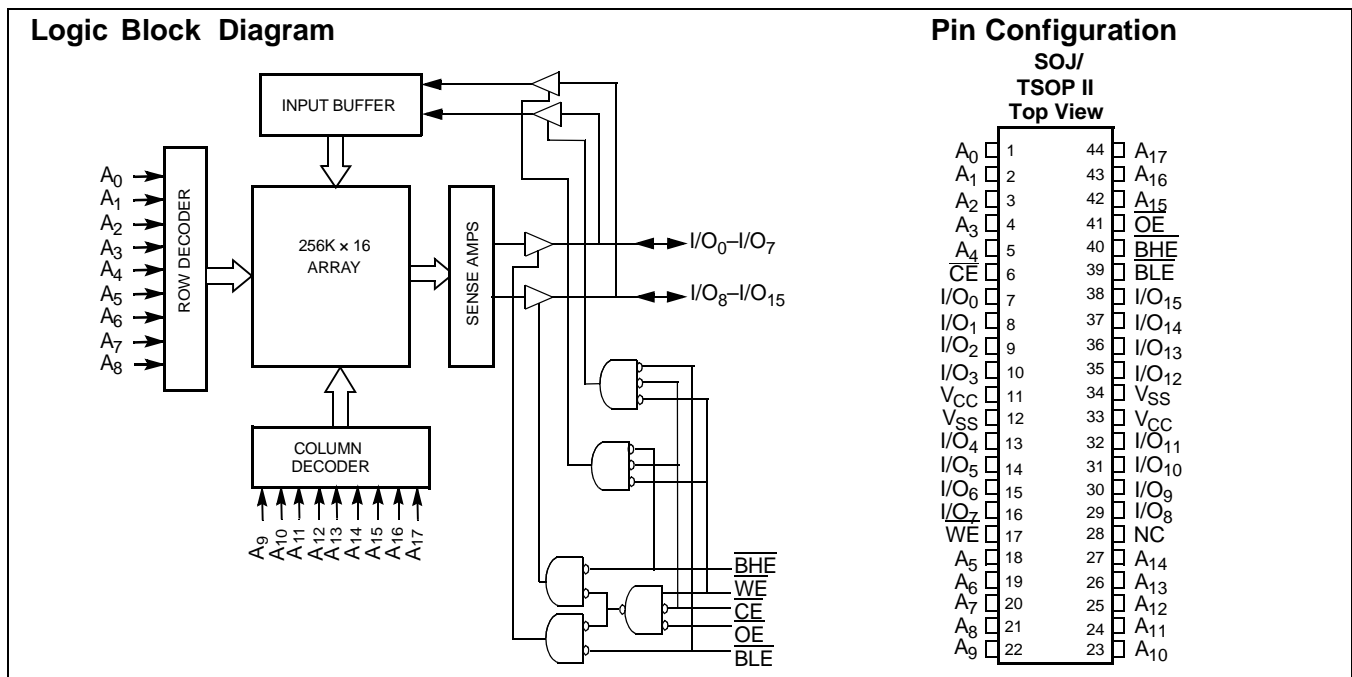
The CY7C1041CV33 is a high-performance CMOS Static RAM organized as 262,144 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte LOW Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$ – $I/O_7$ ), is written into the location specified on the address pins ( $A_0$ – $A_{17}$ ). If Byte HIGH Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$ – $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$ – $A_{17}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte LOW Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  –  $I/O_7$ . If Byte HIGH Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$ – $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1041CV33 is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout, as well as a 48-ball fine-pitch ball grid array (FBGA) package.



**Notes:**

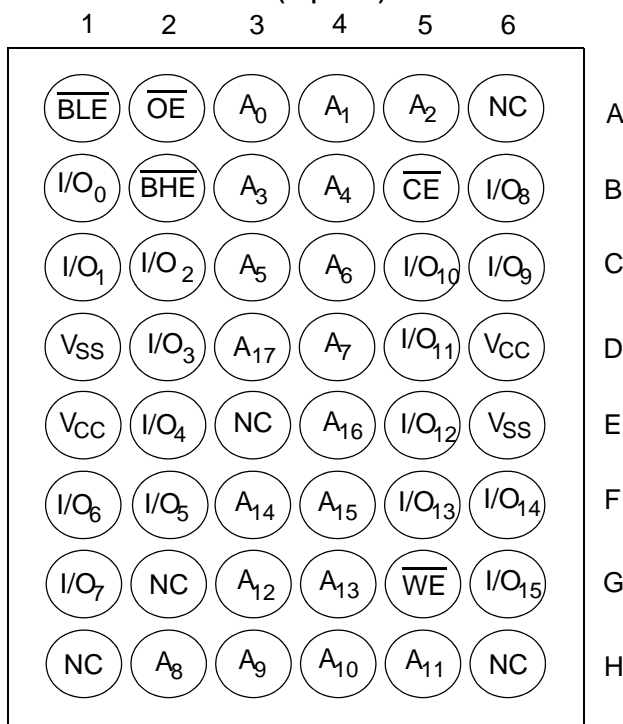
1. For guidelines on SRAM system design, please refer to the "System Design Guidelines" Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).

**Selection Guide**

		<b>-10</b>	<b>-12</b>	<b>-15</b>	<b>-20</b>	<b>Unit</b>
Maximum Access Time		10	12	15	20	ns
Maximum Operating Current	Commercial	90	85	80	75	mA
	Industrial	100	95	90	85	mA
	Automotive-A	100			85	mA
	Automotive-E				90	mA
Maximum CMOS Standby Current	Commercial/ Industrial	10	10	10	10	mA
	Automotive-A	10				mA
	Automotive-E				15	mA

**Pin Configurations**

**48-ball FBGA  
(Top View)**



**Pin Definitions**

Pin Name	44-SOJ, 44-TSOP Pin Number	48-ball FBGA Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>17</sub>	1–5, 18–27, 42–44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3	Input	<b>Address Inputs used to select one of the address locations.</b>
I/O <sub>0</sub> –I/O <sub>15</sub>	7–10,13–16, 29–32, 35–38	B1, C1, C2, D2, E2, F2, F1, G1, B6, C6, C5, D5, E5, F5, F6, G6	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation
NC	28	A6, E3, G2, H1, H6	No Connect	<b>No Connects.</b> This pin is not connected to the die
$\overline{\text{WE}}$	17	G5	Input/Control	<b>Write Enable Input, active LOW.</b> When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
$\overline{\text{CE}}$	6	B5	Input/Control	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	B2, A1	Input/Control	<b>Byte Write Select Inputs, active LOW.</b> $\overline{\text{BHE}}$ controls I/O <sub>15</sub> –I/O <sub>8</sub> , $\overline{\text{BLE}}$ controls I/O <sub>7</sub> –I/O <sub>0</sub>
$\overline{\text{OE}}$	41	A2	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V <sub>SS</sub>	12, 34	D1, E6	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	11, 33	D6, E1	Power Supply	<b>Power Supply inputs to the device.</b>

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage on V <sub>CC</sub> to Relative GND <sup>[2]</sup> ....	-0.5V to +4.6V
DC Voltage Applied to Outputs in High-Z State <sup>[2]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V
DC Input Voltage <sup>[2]</sup> .....	-0.5V to V <sub>CC</sub> + 0.5V
Current into Outputs (LOW) .....	20 mA

Static Discharge Voltage.....>2001V  
(per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	
Automotive-A	-40°C to +85°C	
Automotive-E	-40°C to +125°C	

**DC Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		-20		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>IL</sub> <sup>[2]</sup>	Input LOW Voltage		-0.3	0.8	-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Com'I/Ind'I	-1	+1	-1	+1	-1	+1	-1	+1	μA
			Auto-A	-1	+1					-1	+1	μA
			Auto-E							-20	+20	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	Com'I/Ind'I	-1	+1	-1	+1	-1	+1	-1	+1	μA
			Auto-A	-1	+1					-1	+1	μA
			Auto-E							-20	+20	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Com'I		90		85		80		75	mA
			Ind'I		100		95		90		85	mA
			Auto-A		100						85	mA
			Auto-E								90	mA
I <sub>SB1</sub>	Automatic CE Power-down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Com'I/Ind'I		40		40		40		40	mA
			Auto-A		40						40	mA
			Auto-E								45	mA
I <sub>SB2</sub>	Automatic CE Power-down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V, or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'I/Ind'I		10		10		10		10	mA
			Auto-A		10						10	mA
			Auto-E								15	mA

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 3.3V	8	pF
C <sub>OUT</sub>	I/O Capacitance		8	pF

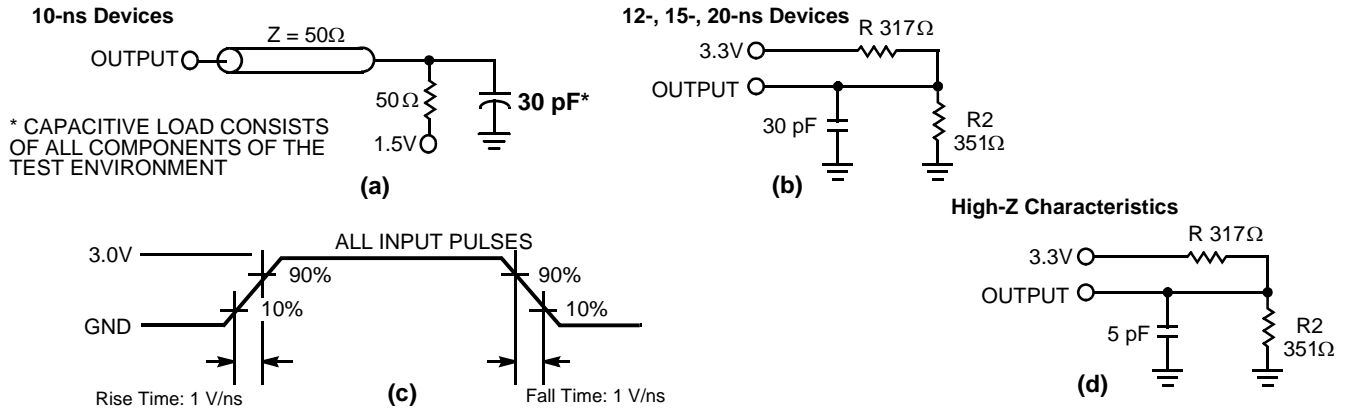
**Notes:**

- V<sub>IL</sub> (min.) = -2.0V and V<sub>IH</sub> (max) = V<sub>CC</sub> + 0.5V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance<sup>[3]</sup>

Parameter	Description	Test Conditions	TSOP-II	FBGA	SOJ	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	42.96	38.15	25.99	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		10.75	9.15	18.8	°C/W

AC Test Loads and Waveforms<sup>[4]</sup>



AC Switching Characteristics<sup>[5]</sup> Over the Operating Range

Parameter	Description	-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
$t_{power}^{[6]}$	$V_{CC}$ (typical) to the first access	100		100		100		100		μs
$t_{RC}$	Read Cycle Time	10		12		15		20		ns
$t_{AA}$	Address to Data Valid		10		12		15		20	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		10		12		15		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		6		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z	0		0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[7, 8]</sup>		5		6		7		8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[8]</sup>	3		3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[7, 8]</sup>		5		6		7		8	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		10		12		15		20	ns
$t_{DBE}$	Byte Enable to Data Valid		5		6		7		8	ns
$t_{LZBE}$	Byte Enable to Low-Z	0		0		0		0		ns
$t_{HZBE}$	Byte Disable to High-Z		6		6		7		8	ns

Notes:

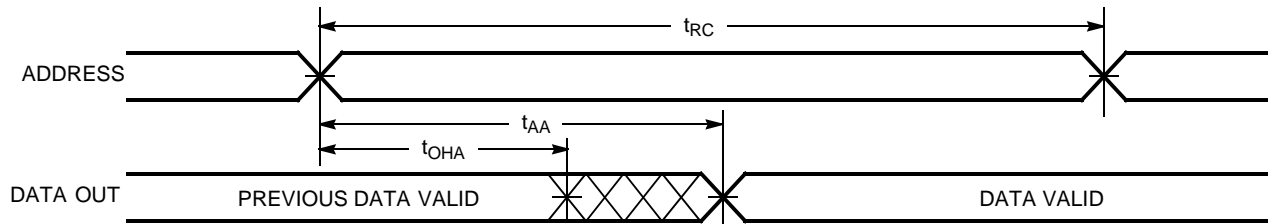
- AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- $t_{power}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

AC Switching Characteristics<sup>[5]</sup> Over the Operating Range (continued)

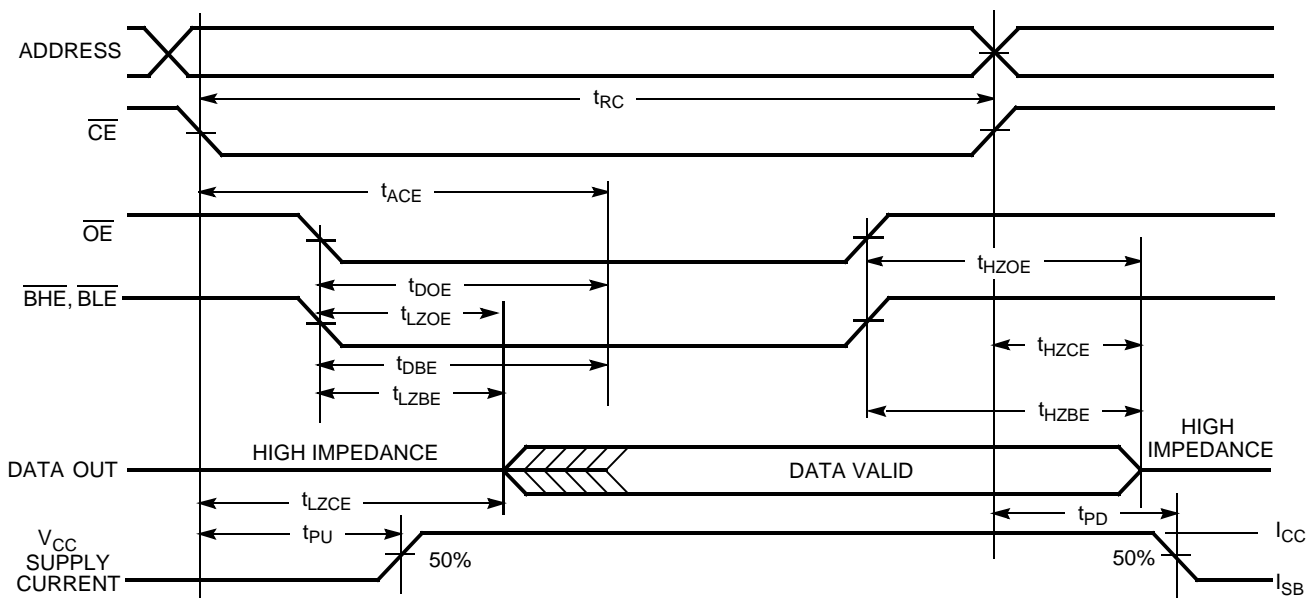
Parameter	Description	-10		-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Write Cycle<sup>[9, 10]</sup></b>										
$t_{WC}$	Write Cycle Time	10		12		15		20		ns
$t_{SCE}$	CE LOW to Write End	7		8		10		10		ns
$t_{AW}$	Address Set-Up to Write End	7		8		10		10		ns
$t_{HA}$	Address Hold from Write End	0		0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		8		10		10		ns
$t_{SD}$	Data Set-Up to Write End	5		6		7		8		ns
$t_{HD}$	Data Hold from Write End	0		0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[7]</sup>	3		3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[7, 8]</sup>		5		6		7		8	ns
$t_{BW}$	Byte Enable to End of Write	7		8		10		10		ns

Switching Waveforms

Read Cycle No. 1<sup>[11, 12]</sup>



Read Cycle No. 2 (OE Controlled)<sup>[12, 13]</sup>

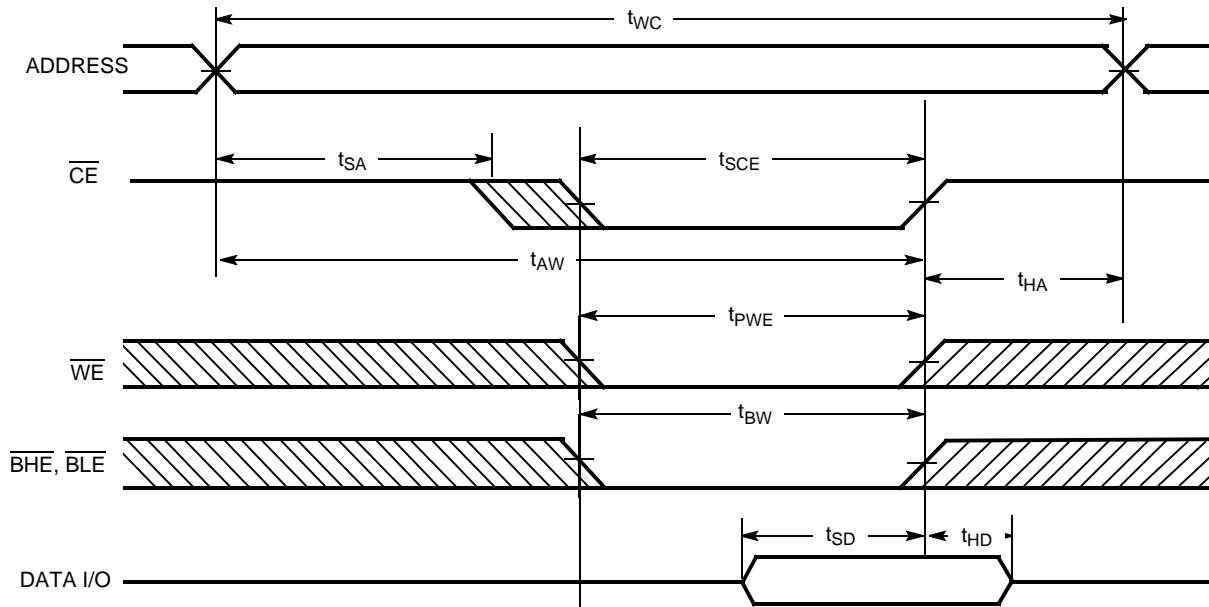


Notes:

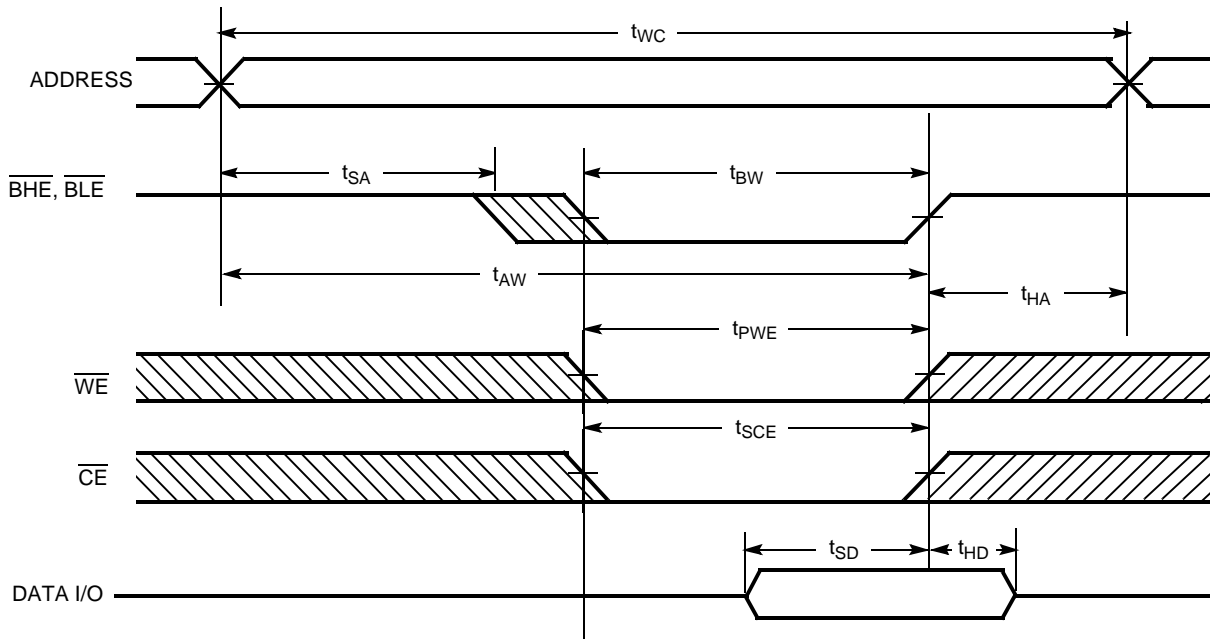
- 10. The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 11. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BLA} = V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for Read cycle.
- 13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled)<sup>[14, 15]</sup>



Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



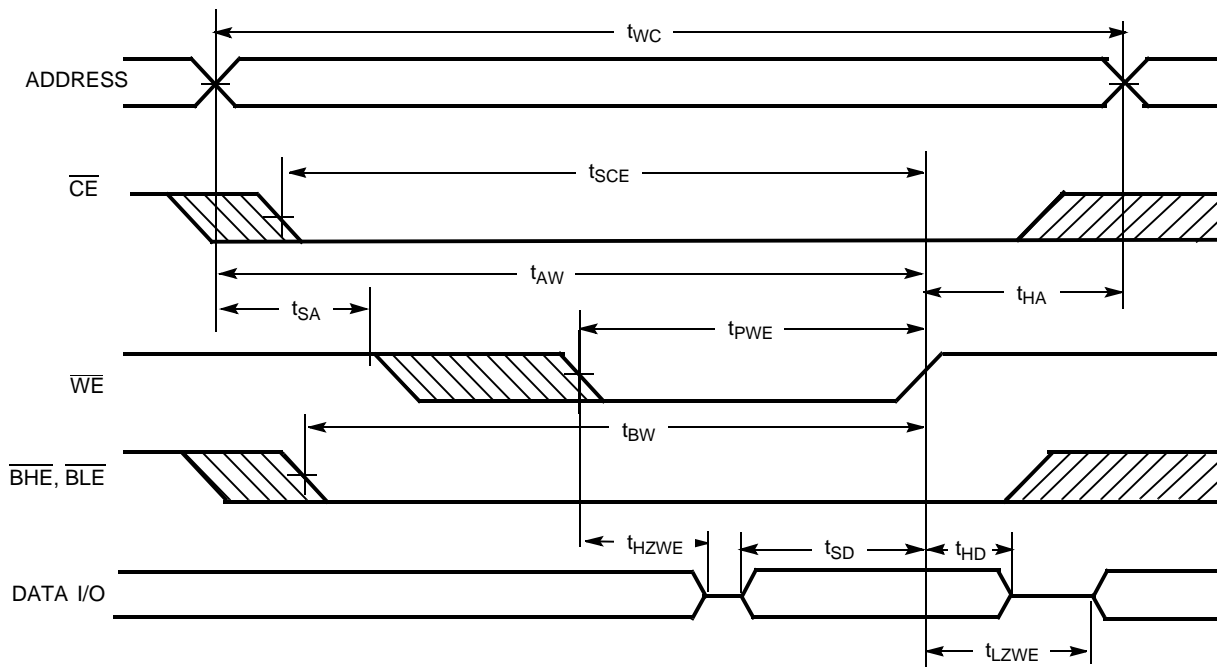
Notes:

- 14. Data I/O is high-impedance if  $\overline{\text{OE}}$  or  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{IH}$ .
- 15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.



Switching Waveforms (continued)

Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)



Truth Table

CE	OE	WE	BLE	BHE	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby ( $I_{SB}$ )
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active ( $I_{CC}$ )
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active ( $I_{CC}$ )
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active ( $I_{CC}$ )
L	X	L	L	L	Data In	Data In	Write All Bits	Active ( $I_{CC}$ )
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active ( $I_{CC}$ )
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active ( $I_{CC}$ )
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

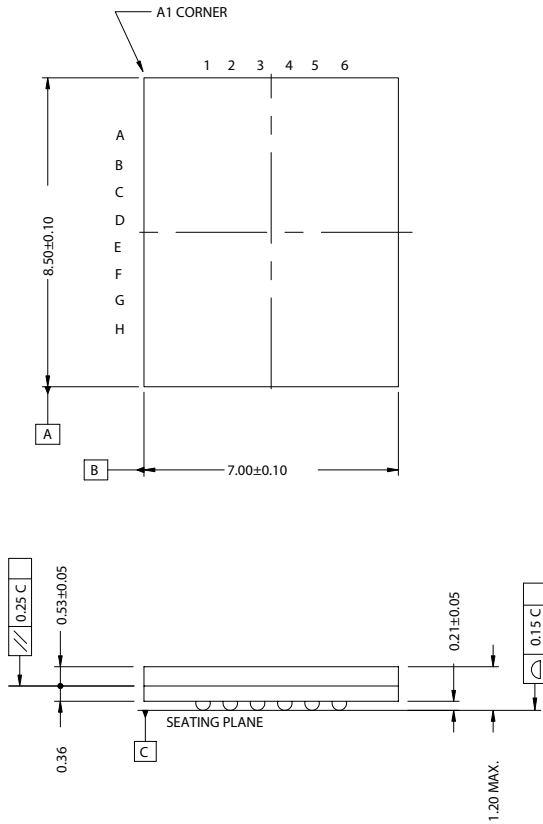
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range		
10	CY7C1041CV33-10BAC	51-85106	48-ball Fine Pitch BGA	Commercial		
	CY7C1041CV33-10BAXC		48-ball Fine Pitch BGA (Pb-Free)			
	CY7C1041CV33-10VC	51-85082	44-lead (400-mil) Molded SOJ		Industrial	
	CY7C1041CV33-10VXC		44-lead (400-mil) Molded SOJ (Pb-Free)			
	CY7C1041CV33-10ZC	51-85087	44-pin TSOP II			Automotive-A
	CY7C1041CV33-10ZXC		44-pin TSOP II (Pb-Free)			
	CY7C1041CV33-10BAI	51-85106	48-ball Fine Pitch BGA	Automotive-A		
	CY7C1041CV33-10BAXI		48-ball Fine Pitch BGA (Pb-Free)			
	CY7C1041CV33-10ZI	51-85087	44-pin TSOP II		Automotive-A	
	CY7C1041CV33-10ZXI		44-pin TSOP II (Pb-Free)			
	CY7C1041CV33-10ZSXA	51-85106	44-pin TSOP II (Pb-Free)			Automotive-A
	CY7C1041CV33-10BAXA		48-ball Fine Pitch BGA (Pb-Free)			
12	CY7C1041CV33-12VC	51-85082	44-lead (400-mil) Molded SOJ	Commercial		
	CY7C1041CV33-12VXC		44-lead (400-mil) Molded SOJ (Pb-Free)			
	CY7C1041CV33-12ZC	51-85087	44-pin TSOP II		Industrial	
	CY7C1041CV33-12ZXC		44-pin TSOP II (Pb-Free)			
	CY7C1041CV33-12VXI	51-85082	44-lead (400-mil) Molded SOJ (Pb-Free)	Industrial		
	CY7C1041CV33-12ZI	51-85087	44-pin TSOP II			
	CY7C1041CV33-12ZXI		44-pin TSOP II (Pb-Free)			
15	CY7C1041CV33-15VC	51-85082	44-lead (400-mil) Molded SOJ	Commercial		
	CY7C1041CV33-15VXC		44-lead (400-mil) Molded SOJ (Pb-Free)			
	CY7C1041CV33-15ZC	51-85087	44-pin TSOP II		Industrial	
	CY7C1041CV33-15ZXC		44-pin TSOP II (Pb-Free)			
	CY7C1041CV33-15VI	51-85082	44-lead (400-mil) Molded SOJ	Industrial		
	CY7C1041CV33-15VXI		44-lead (400-mil) Molded SOJ (Pb-Free)			
	CY7C1041CV33-15ZI	51-85087	44-pin TSOP II			
	CY7C1041CV33-15ZXI		44-pin TSOP II (Pb-Free)			
20	CY7C1041CV33-20ZC	51-85087	44-pin TSOP II			Commercial
	CY7C1041CV33-20ZXC		44-pin TSOP II (Pb-Free)			
	CY7C1041CV33-20ZSXA		44-pin TSOP II (Pb-Free)			
	CY7C1041CV33-20VE	51-85082	44-lead (400-mil) Molded SOJ		Automotive-E	
	CY7C1041CV33-20VXE		44-lead (400-mil) Molded SOJ (Pb-Free)			
	CY7C1041CV33-20ZE	51-85087	44-pin TSOP II	Automotive-E		
	CY7C1041CV33-20ZSXE		44-pin TSOP II (Pb-Free)			

Please contact your local Cypress sales representative for availability of these parts

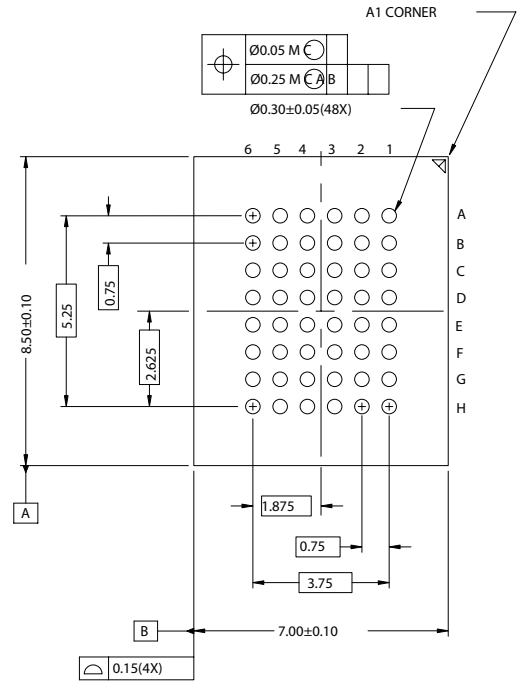
**Package Diagrams**

**48-Ball (7.00 mm x 8.50 mm x 1.2 mm) FBGA (51-85106)**

TOP VIEW



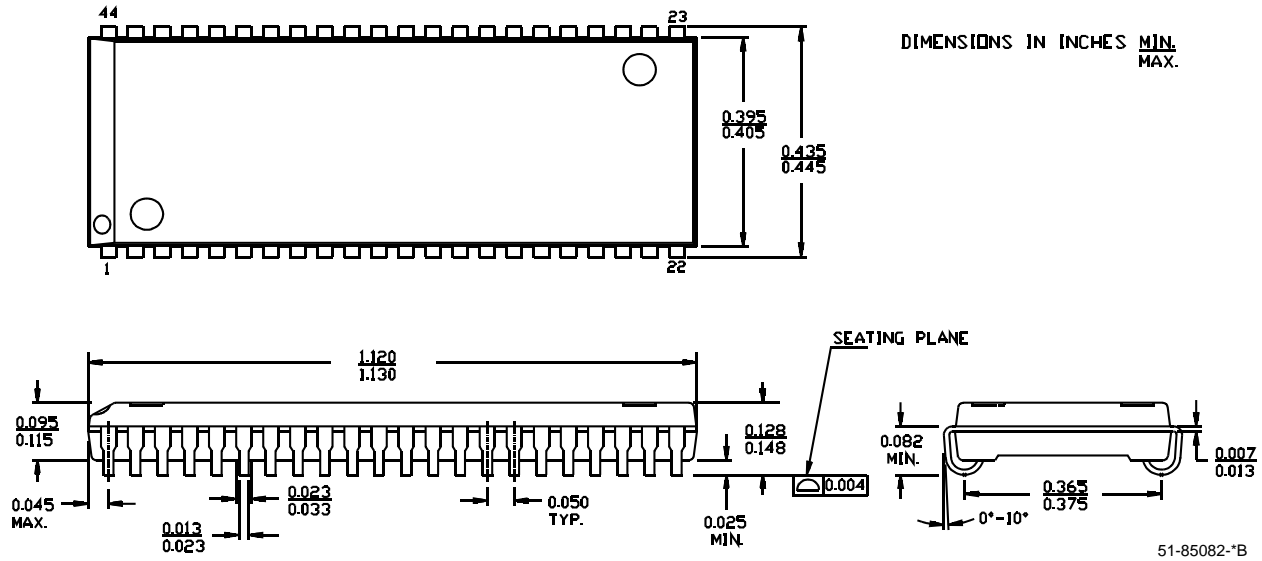
BOTTOM VIEW



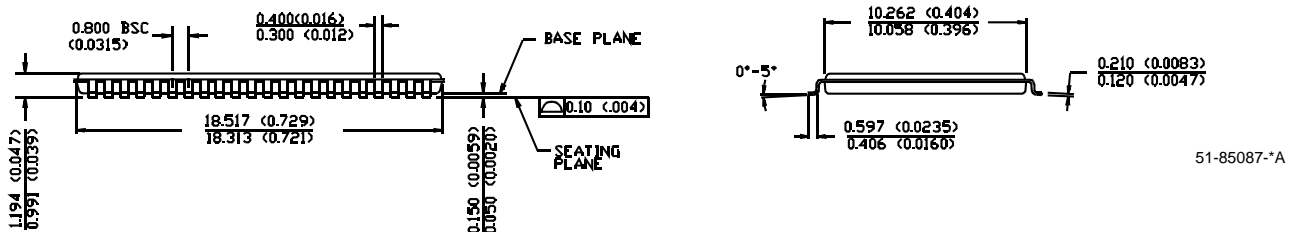
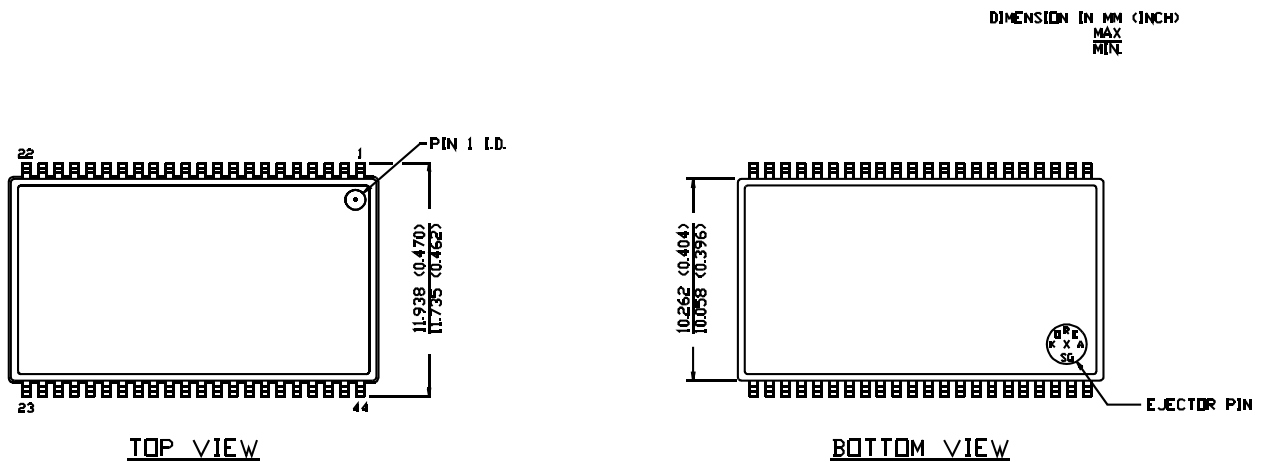
51-85106-\*E

Package Diagrams (continued)

44-lead (400-mil) Molded SOJ (51-85082)



44-pin TSOP II (51-85087)



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**Document History Page**

Document Title: CY7C1041CV33 4-Mbit (256K x 16) Static RAM				
Document Number: 38-05134				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109513	12/13/01	HGK	New Data Sheet
*A	112440	12/20/01	BSS	Updated 51-85106 from revision *A to *C
*B	112859	03/25/02	DFP	Added CY7C1042CV33 in BGA package Removed 1042 BGA option pin ACC Final Data Sheet
*C	116477	09/16/02	CEA	Add applications foot note to data sheet
*D	119797	10/21/02	DFP	Added 20-ns speed bin
*E	262949	See ECN	RKF	1) Added Lead (Pb)-Free parts in the Ordering info (Page #9) 2) Added Automotive Specs to Datasheet
*F	361795	See ECN	SYT	Added Pb-Free offerings in the Ordering Information
*G	435387	See ECN	NXR	Removed -8 Speed bin from Product offering. Corrected typo in description for BHE/BLE in pin definitions table on Page# 3 corrected ther Pin name from OE2 to OE. Included the Maximum Ratings for Static Discharge Voltage and Latch up Current. Changed the description of I <sub>IX</sub> current from Input Load Current to Input Leakage Current Added note# 4 on page# 4 Updated the Ordering Information table
*H	499153	See ECN	NXR	Added Automotive-A Operating Range Changed t <sub>power</sub> value from 1 μs to 100 μs Updated Ordering Information table