Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FAIRCHILD
SEMICONDUCTOR™

September 2001
Revised August 2003

FIN1048
3.3V LVDS 4-Bit Flow-Through High Speed Differential Receiver

General Description

This quad receiver is designed for high speed interconnect utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100mV, to LVTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1048 can be paired with its companion driver, the FIN1047, or any other LVDS driver.

Features

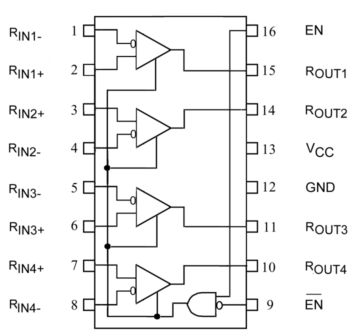
- Greater than 400Mbs data rate
- Flow-through pinout simplifies PCB layout
- 3.3V power supply operation
- 0.4ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Fail safe protection for open-circuit, shorted and terminated conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and LVPECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1048M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1048MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering code.

Connection Diagram



Pin Descriptions

Pin Name	Description
R_{OUT1}, R_{OUT2}, R_{OUT3}, R_{OUT4}	LVTTL Data Outputs
R_{IN1+}, R_{IN2+}, R_{IN3+}, R_{IN4+}	Non-Inverting LVDS Inputs
R_{IN1-}, R_{IN2-}, R_{IN3-}, R_{IN4-}	Inverting LVDS Inputs
EN	Driver Enable Pin
$\overline{EN}$	Inverting Driver Enable Pin
V_{CC}	Power Supply
GND	Ground

Function Table

Inputs				Outputs
EN	$\overline{EN}$	R_{IN+}	R_{OUT-}	R_{OUT}
H	L or Open	H	L	H
H	L or Open	L	H	L
H	L or Open	Fail Safe Condition		H
X	H	X	X	Z
L or Open	X	X	X	Z

H = HIGH Logic Level L = LOW Logic Level X = Don’t Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	–0.5V to +4.6V
DC Input Voltage (V_{IN})	–0.5V to +4.6V
DC Input Voltage (V_{OUT})	–0.5V to 6V
DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 10,000V
ESD (Machine Model)	≥ 450V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Magnitude of Differential Voltage	
($\|V_{ID}\|$)	100mV to V_{CC}
Common-Mode Input Voltage (V_{IC})	0.05V to 2.35V
Input Voltage (V_{IN})	0 to V_{CC}
Operating Temperature (T_A)	–40°C to +85°C

Note 1: The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1 and Table 1	–100			mV
I_{IN}	Input Current	V_{IN} = 0V or V_{CC}			±20	µA
$I_{I(OFF)}$	Power-Off Input Current	V_{CC} = 0V, V_{IN} = 0V or 3.6V			±20	µA
V_{IH}	Input High Voltage (EN or $\overline{EN}$)		2.0		V_{CC} + 1.0	V
V_{IL}	Input Low Voltage (EN or $\overline{EN}$)		GND		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –100 µA	V_{CC} –0.2			V
		I_{OH} = –8 mA	2.4			
V_{OL}	Output LOW Voltage	I_{OH} = 100 µA			0.2	V
		I_{OL} = 8 mA			0.5	
I_{OZ}	Disabled Output Leakage Current	EN = 0.8 and EN* = 2V, V_{OUT} = 3.6V or 0V			±20	µA
V_{IK}	Input Clamp Voltage	I_{IK} = –18 mA	–1.5			V
I_{CCZ}	Disabled Power Supply Current	Receiver Disabled			5	mA
I_{CC}	Power Supply Current	Receiver Enabled, (R_{IN+} = 1V and R_{IN-} = 1.4V) or (R_{IN+} = 1.4V and R_{IN-} = 1V)			15	mA
C_{IN}	Input Capacitance			3.5		pF
C_{OUT}	Output Capacitance			6		pF

Note 2: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

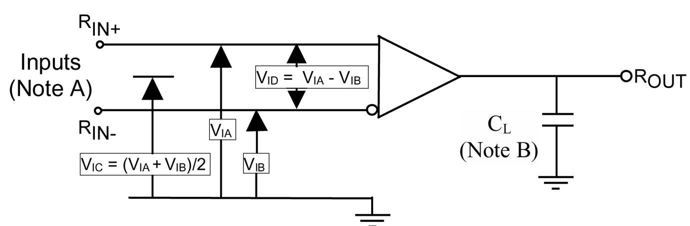
Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLH}	Propagation Delay LOW-to-HIGH	$\lvert V_{ID}\rvert$ = 400 mV, C_L = 10 pF, R_L = 1kΩ See Figure 1 and Figure 2	1.0		2.5	ns
t_{PHL}	Propagation Delay HIGH-to-LOW		1.0		2.5	ns
t_{TLH}	Output Rise Time (20% to 80%)			0.7	1.2	ns
t_{THL}	Output Fall Time (80% to 20%)			0.7	1.2	ns
$t_{SK(P)}$	Pulse Skew $\lvert t_{PLH} - t_{PHL}\rvert$				0.4	ns
$t_{SK(LH)}$ $t_{SK(HL)}$	Channel-to-Channel Skew (Note 4)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)				1.0	ns
f_{MAX}	Maximum Operating Frequency (Note 6)	R_L = 1kΩ, C_L = 10 pF, see Figure 1 and Figure 2	200	375		MHz
t_{ZH}	LVTTL Output Enable Time from Z to HIGH	R_L = 1kΩ, C_L = 10 pF, See Figure 3			6.0	ns
t_{ZL}	LVTTL Output Enable Time from Z to LOW				6.0	ns
t_{HZ}	LVTTL Output Disable Time from HIGH to Z				6.0	ns
t_{LZ}	LVTTL Output Disable Time from LOW to Z				6.0	ns

Note 3: All typical values are at T_A = 25°C and with V_{CC} = 3.3V.

Note 4: $t_{SK(LH)}$, $t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: f_{MAX} Criteria: Input $t_R = t_F$ < 1 ns, V_{ID} = 300 mV, (1.05V to 1.35V pp), 50% duty cycle; Output duty cycle 40% to 60%, V_{OL} < 0.5V, V_{OH} > 2.4V. All channels switching in phase.



Note A: All differential input pulses have frequency = 10MHz, t_R or t_F = 1ns

Note B: C_L includes all probe and jig capacitances

FIGURE 1. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mA)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

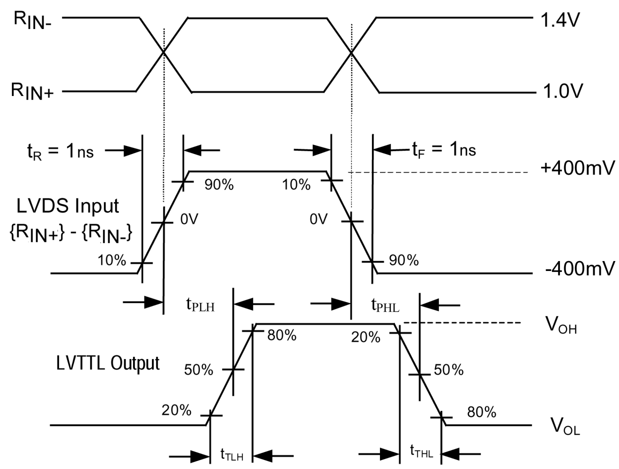
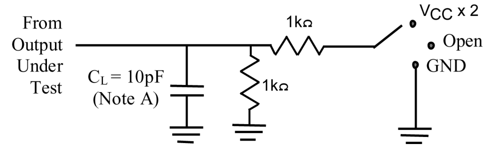


FIGURE 2. LVDS Input to LVTTL Output AC Waveforms

Test Circuit for LVTTL Outputs



Test	Switch state
	Open
t_{PZL}/t_{PLZ}	V_{CC} x 2
t_{PHZ}/t_{PZH}	GND

Voltage Waveforms Enable and Disable Times

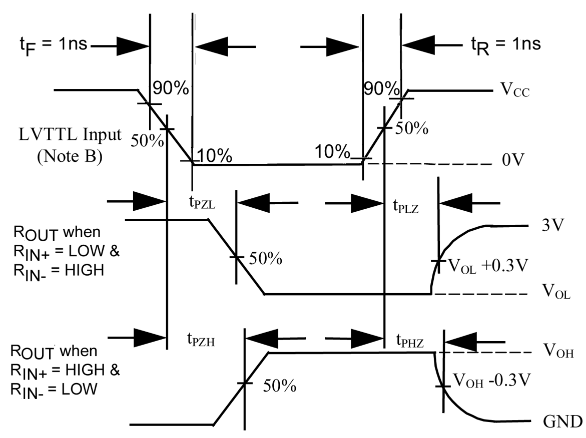
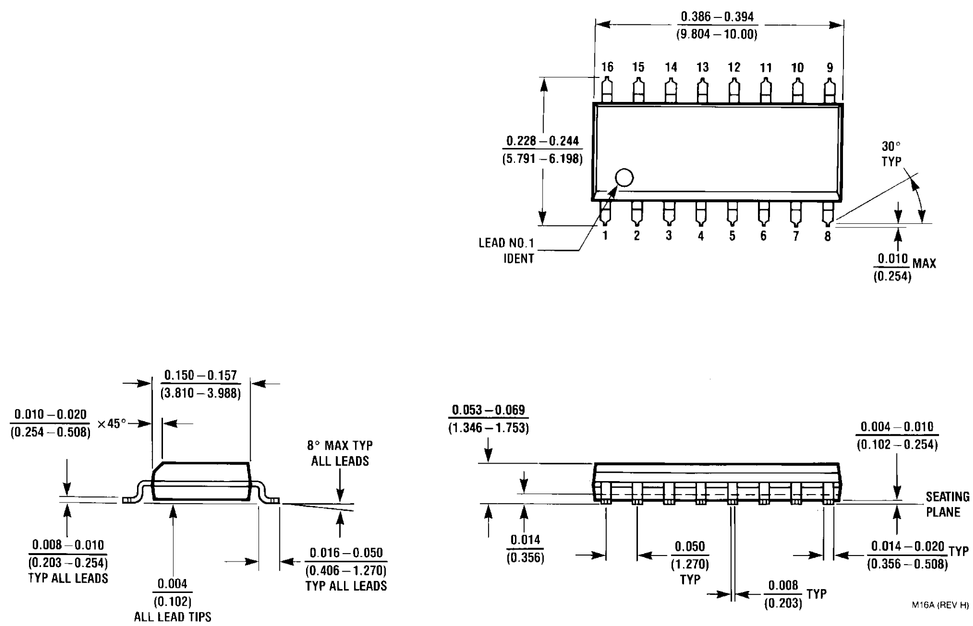


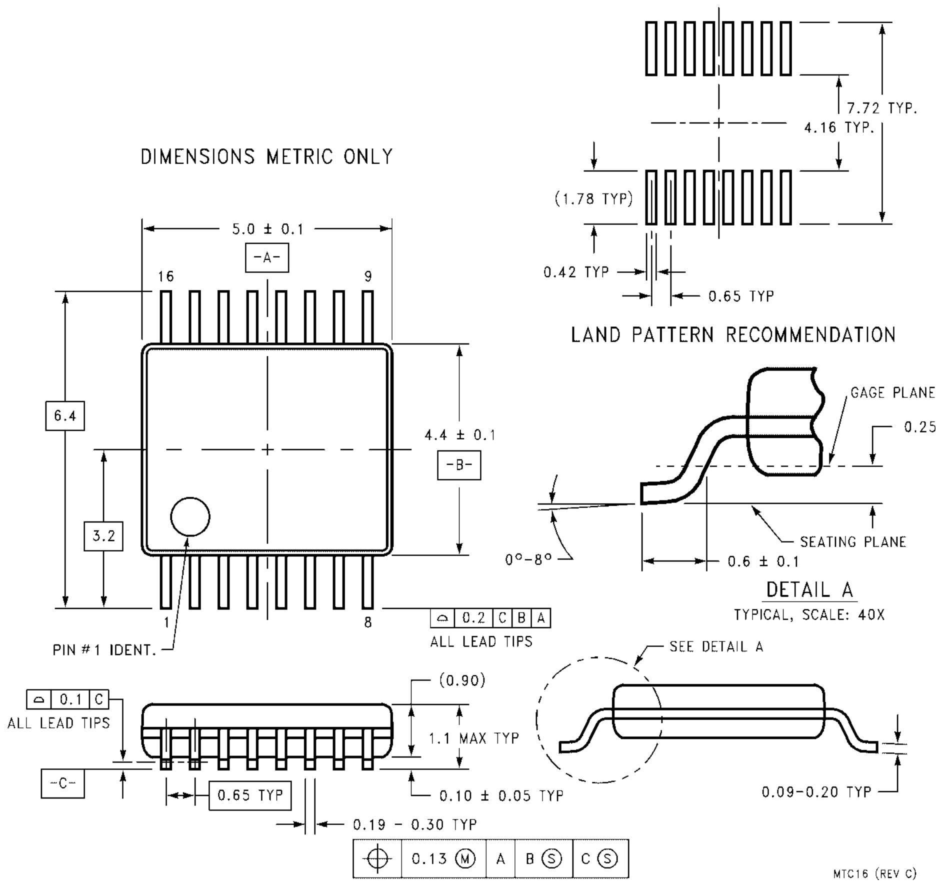
FIGURE 3. LVTTL Outputs Test Circuit and AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16